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Analysis and design of an analog control loop for digital input class D amplifiers

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Abstract—Analog input Class D Amplifiers are widely used in battery powered systems such as mobile phones to achieve high efficiency but it suffers from a complex DAC to convert the digital audio signal into an analog one. To increase the playback time, this paper presents digital input class D amplifiers using digital modulation. The proposed Class D amplifier is also controlled using an analog loop to achieve a good power supply immunity and low harmonic distortion. Usual AC analysis of this loop cannot be done due to its switching behavior. Very long transient simulation was the only solution to predict the dynamics performances of the control. To overcome this issue, the presented work includes a modeling method in order to study faster the control performances. The proposed modeling is then used to increase the audio quality reproduction of our digital input Class D amplifier. The complete audio path is implemented in CMOS 130nm process and characterized in order to validate the architecture, the modeling method and the integrated design.

I. INTRODUCTION

Due to their ideally perfect efficiency, class D amplifiers have become a very attractive solution to implement audio drivers in application with tight power consumption and low voltage requirements such as large electronics consumers systems (Smartphone, tablet, GPS, etc...). The basic class D topology and signal spectrum of each stage are shown on figure 1. It is composed by a modulation stage which transforms low frequency analog audio input signal in high frequency modulated bit stream. In this paper, only Pulse Width Modulation (PWM) is discussed because it is the most used modulation scheme. Then, a power stage translates the bit stream to power supply rails in order to feed the load. A low pass filter reduces high frequency components due to modulation to reconstitute the audio frequency signal. This basic topology, called “Open Loop analog Class D” suffers from major drawbacks which make it unsuitable for embedded audio amplifiers. Indeed, the errors introduced by the modulator, the power stage and the power supply are not corrected.

The presented work is then motivated by the requirement of effective control for audio class D amplifiers with high linearity, high power supply noise rejection and high efficiency.

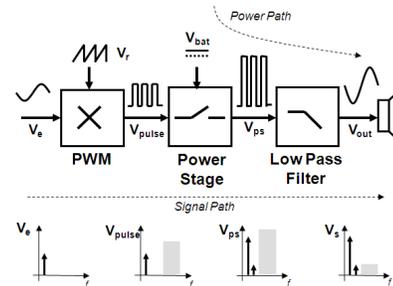


Figure 1. Open Loop Class D topology and spectrum of each stage

Depending of the application, the input of the power amplifier is analog or digital. Most of embedded systems as smart phone provide a digital signal from the main processor (called digital base band). Then two topologies are possible for the audio path as shown in figure 2. On the top, the audio input signal is first converted into an analog signal to drive the analog PWM based power amplifier (as presented in figure 1). The analog PWM is called Natural PWM (NPWM). On the bottom of figure 2, the digital audio signal is directly modulated into a pulse train using Uniform PWM (UPWM) [1].

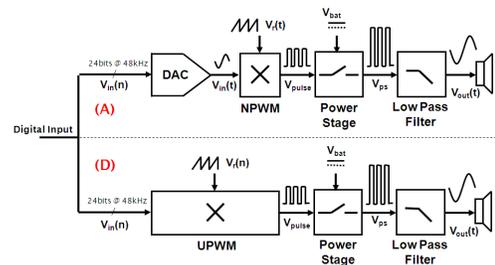


Figure 2. Analog and digital modulation for class D amplifiers.

The second topology does not require a high resolution DAC but needs digital input compatible class D amplifier. It is then more efficient and provides higher efficiency (and then increases playback time). In order to correct the power supply variation and the non linearity of the power stage, an analog control loop is used around the power stage. The proposed digital input Class D topology is shown on figure 3:

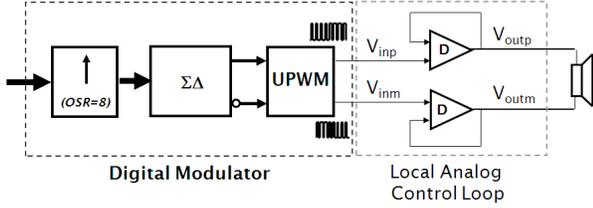


Figure 3. Digital input topology for class D amplifiers.

In a first section, the digital modulator and the local analog control loop are presented. In order to predict faster the performance of the proposed control, the linearization of the loop is then proposed, allowing AC analysis. The proposed modeling is then used to increase dynamics performances of the loop. A digital input class D amplifier based on the proposed loop is then integrated using CMOS 130nm process. The silicon measurements match analog class D state of the art performances with the benefit of the digital input compatibility.

II. DIGITAL AUDIO CLASS D AMPLIFIER

A. Digital Modulator

This section presents the digital modulator topology. As shown on the previous figure, there are three blocks in the proposed solution: Interpolation, Noise shaping ($\Sigma\Delta$) and Uniform PWM. A detailed analysis of the digital modulator is available in [1]. These three steps are needed since it is not possible to realize a direct UPWM from the input signal due to its high resolution ($n=24$ bits sampled at $f_s=48\text{kHz}$). Indeed, in this case, the required carrier frequency f_{UPWM} is defined by:

$$f_{\text{UPWM}} = 2^n \times f_s = 2^{24} \times 48\text{k} = 805.3 \text{ GHz} \quad (1)$$

As it is not possible to reduce f_s due to Nyquist criteria, the only effective way to decrease f_{UPWM} is to reduce the resolution n of the input signal of UPWM process. In order to keep the Signal to Noise Ratio (SNR) of the audio signal, the reduction of the resolution is done using a 4th order $\Sigma\Delta$ noise shaper. This system requires an interpolation process to increase the sampling frequency of input signal which increases the linearity of UPWM as well [1]. In the proposed solution, the interpolation has an OSR equal to 8 and the resolution of the signal after the noise shaping is $m=6$ bits. With this value, the UPWM process frequency becomes:

$$f_{\text{UPWM}} = 2^m \times \text{OSR} \times f_s = 2^6 \times 8 \times 48\text{k} = 24.576 \text{ MHz} \quad (2)$$

B. Analog Control Loop Description

The local analog control loop proposed is shown on the figure 4 [2]. As the digital and analog supplies could be different, the amplitude of the input bit stream is called V_{ana} whereas the amplitude of the output one is V_{bat} .

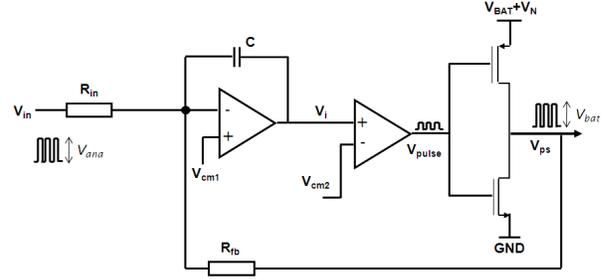


Figure 4. Analog Control loop topology

In steady state, signal V_{in} , V_{ps} and V_i are represented on figure 5.

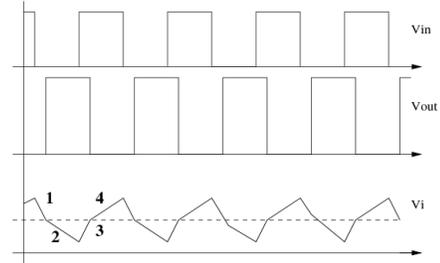


Figure 5. Input, output and control signals

To work properly, the evolution on V_i must not change when the output signal changes. Indeed, at the end of phase 1, V_{out} voltage goes from V_{bat} to ground, which obviously changes R_{fb} current source in a current sink. If this sink is higher than R_{in} current sources, evolution on V_i voltage switches and the loop falls into self commutation mode. The same issue is possible at the end of phase 3.

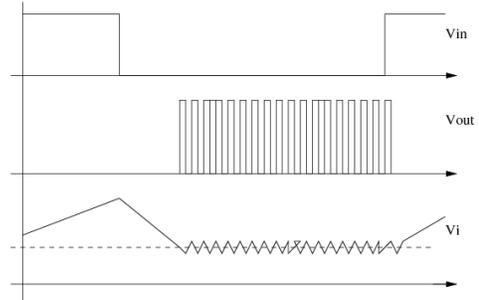


Figure 6. Inversion of V_i due to wrong ratio of current sources

To avoid this instability at the end of phases 1 and 3, the following condition must be respected:

$$\frac{R_{\text{fb}}}{R_{\text{in}}} \geq \frac{V_{\text{bat}}}{V_{\text{ana}}} \quad (3)$$

Where V_{bat} and V_{ana} are supply voltages of the power stage and the digital modulator. This condition will limit the AC performances as seen later in this paper.

In addition, to insure good linearity, phases 1/3 and 2/4 must be symmetrical. This condition gives the ideal value of reference voltage V_{cm1} :

$$V_{cm1} = \frac{1}{2}V_{bat} \frac{R_{in}}{R_{fb} + R_{in}} + \frac{1}{2}V_{ana} \frac{R_{fb}}{R_{fb} + R_{in}} \quad (4)$$

III. ANALOG CONTROL LOOP MODELING

In order to study dynamics performances of the proposed loop, an AC or ‘‘Small Signal’’ analysis must be done. For this, the linearization of the comparator and the power stage is required. In analog class D amplifier, a method consists in the calculation of an average model during one period of the carrier [3]. This method cannot be used here because there is not any carrier to synchronize the loop since the commutation occurs from the input signal. Another method of linearization is presented in [4] based on transient evolution of signal. It can be used here too because V_i signal is not differentiable (see fig. 5).

The proposed modelisation is then based on the creation of a virtual carrier using input signal characteristic in order to allow the use of the first presented method. Indeed, the analog input class D amplifier basic topology (fig. 7) is very close to the proposed analog control loop (fig. 4).

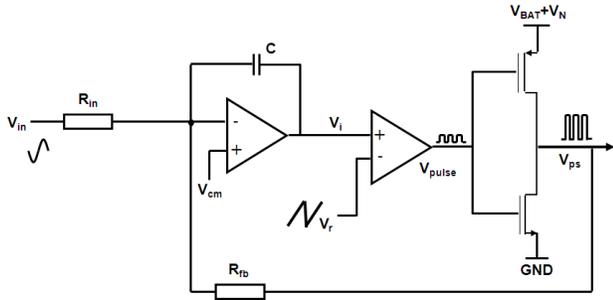


Figure 7. Basic analog input class D amplifiers

To understand how this virtual carrier is created, let's consider the four steps of equivalence between classic analog class D amplifiers (fig. 8 - E1) and the proposed solution (fig. 8 - E4).

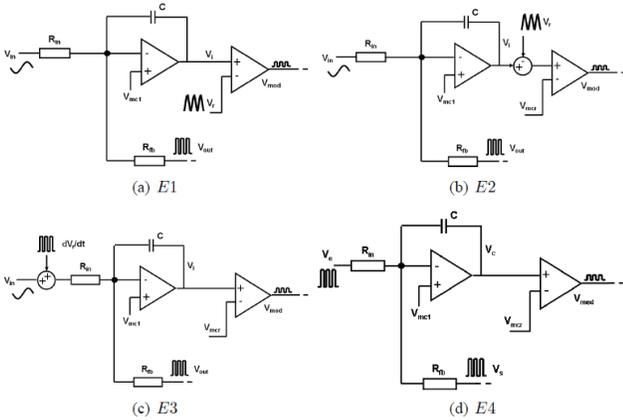


Figure 8. The four steps of equivalence

The step E2 is equivalent to E1 since the test $a(t) > b(t)$ is equivalent to the test $a(t) - b(t) > 0$. The sawtooth signal V_r in E2 is the result of the integration of a square wave in E3. The last equivalence is based of a decomposition of the input signal of the proposed loop V_{in} as shown on the following figure:

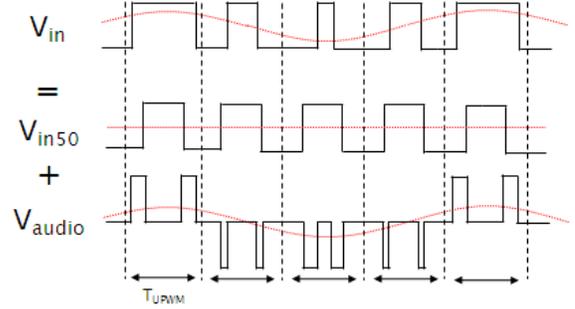


Figure 9. Decomposition of input signal V_{in}

The result of this equivalence leads to the following representation, where G stands for non linear elements:

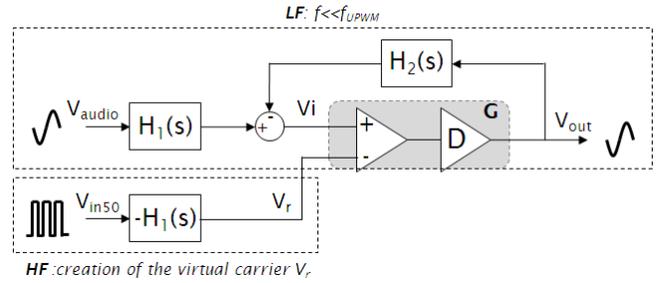


Figure 10. AC representation : LF and HF paths

There are two parts: the low frequency (LF – audio) one and the high frequency (HF) one. The LF part is valid only for frequencies f very low compared to f_{UPWM} . As the loop is synchronized on the input square wave (representing input common mode), it is now possible to average the behavior of non linear bloc (representing by the G bloc on fig. 10). In the figure 10, assuming ideal opamp, H_1 and H_2 are defined by:

$$H_1(s) = -\frac{1}{R_{in}Cs} \quad \& \quad H_2(s) = \frac{1}{R_{fb}Cs} \quad (5)$$

The amplitude V_r of the virtual carrier, created from H_1 in the HF path is then equal to:

$$V_r = \frac{V_{ana}}{2R_{in}C} \times \frac{T_{UPWM}}{2} = \frac{V_{ana}}{4f_{UPWM}R_{in}C} \quad (6)$$

An average model of G, noted \tilde{G} , can be calculated from the amplitude of the virtual carrier using a classic result in PWM modulation [3]:

$$\tilde{G} = \frac{V_{bat}}{V_r} = 4 \frac{V_{bat}}{V_{ana}} f_{UPWM} R_{in} C \quad (7)$$

The signal transfer function of the proposed system, $STF(s)$, and the noise rejection, $NTF(s)$ are then expressed as:

$$STF(s) = -H_1(s) \frac{\tilde{G}}{1 + \tilde{G}H_2(s)} = \frac{R_{fb}}{\frac{R_{in}}{G_{DC}} + 1 + \frac{R_{fb}C}{\tilde{G}}s} \quad (8)$$

$$NTF(s) = \frac{1}{1 + \tilde{G}H_2(s)} = \frac{\tau s}{1 + \tau s} \quad (9)$$

The presented solution has then a first order noise rejection, which limits the Power Supply Rejection (PSR) performances. The system is then unconditionally stable regarding its phase margin (as first order loop). To increase the PSR, which is a key performance in embedded systems using battery, a second order loop is then proposed. The schematic of the solution is given on figure 11. A HF zero must be inserted to avoid AC instability due to loop delays by increasing open loop phase in HF.

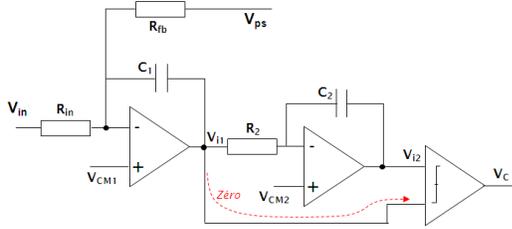


Figure 11. 2nd order loop schematic

Despite of the loop configuration has changed from figure 10 to the one represented on the figure 12, the average model \tilde{G} of non linear element is the same since the virtual carrier is still created by a first order integrator: $H_1(s)$.

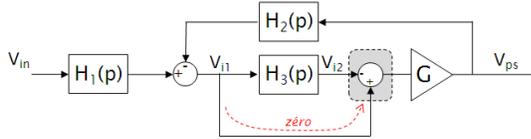


Figure 12. Updated AC representation

IV. DESIGN

The proposed solution, including the digital modulator, the analog control loop and the power stage, has been integrated in single die with CMOS 130nm process. The digital modulator size is around 2k gates [1]. For the analog control loop, the choice of pole/zero frequencies was done considering the tradeoff between the dynamic performances and large signal behavior. Figure 13 shows the layout of the realized chip.

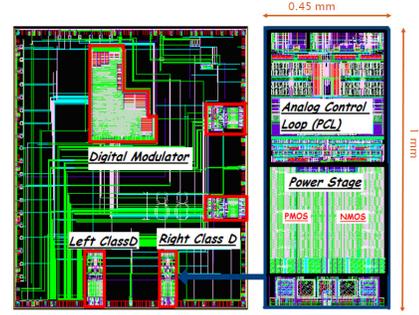


Figure 13. 2nd order loop schematic

The analog loop size is 0.45mm², including the power stage. Figure 14 shows the leveled THD+N (Total Harmonics Distortion plus Noise) of the proposed solution under 3.6V power supply. The THD+N is equal to -75 dB (0.02 %). Yellow curve is mono measurement whereas green is stereo. Complete measurement can be found in [1].

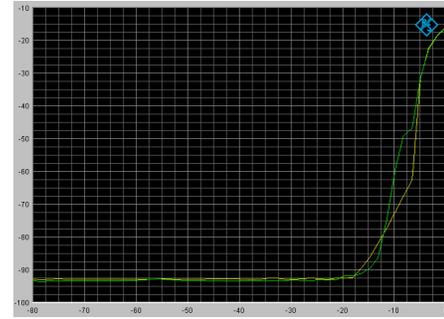


Figure 14. THD+N @ 1kHz vs output power

V. CONCLUSION

This paper has described a digital input class D amplifier a 1-bit digital modulator and an analog controlled class D to reduce the power consumption. The proposed modeling method makes possible AC simulation of the control loop. This better understanding of the dynamic behavior associated with large signal conditions allows the design of an optimal controller.

The digital modulator, the analog control loop and the power stage are integrated in CMOS 130 nm process on a single chip. The proposed solution offers a good combination of low idle power consumption, high power efficiency, and audio performances (@ -20dBFS shows THD 0.01%, SNR 93 dB and PSRR > 70 dB).

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