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Gaël Pillonnet, N Abouchi, R Cellier, A Nagari. A 0.01%THD, 70dB PSRR Single Ended Class D using variable hysteresis control for headphone amplifiers. IEEE International Symposium on Circuits and Systems, IEEE, May 2009, Taipei, Taiwan. pp.4, 10.1109/ISCAS.2009.5117972 . hal-01103722

**HAL Id: hal-01103722**

**<https://hal.science/hal-01103722>**

Submitted on 15 Jan 2015

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# A 0.01%THD, 70dB PSRR Single Ended Class D using Variable Hysteresis Control for Headphone Amplifiers

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**Abstract** — Switching audio amplifiers are widely used in H-Bridge topology thanks to their high efficiency; however low audio performances in single ended power stage topology is a strong weakness leading to not be used for headset applications. This paper explains the importance of efficient error correction in Single Ended Class-D audio amplifier. A hysteresis control for Class-D amplifier with a variable window is also presented. The analyses are verified by simulations and measurements. The proposed solution was fabricated in 0.13 $\mu\text{m}$  CMOS technology with an active area of 0.2mm<sup>2</sup>. It could be used in single ended output configuration fully compatible with common headset connectors. The proposed Class-D amplifier achieves a harmonic distortion of 0.01% and a power supply rejection of 70dB with a quite low static current consumption.

## I. INTRODUCTION

H-Bridge Class-D amplifiers are widely used in loudspeaker mobile application due to their high efficiency. However the major drawback of switching amplifier is linked to non linear behavior limiting the audio performances [1-3]. Recent design, using efficient close-loop topology to alleviate this problem, can achieved around 0.01% THD+N for H-bridge power stage configuration: those architectures show control based on Sigma Delta Modulator [4], Controlled Oscillated Modulator (COM) architecture [5], PWM feedback [6], digital feedback [7], hysteresis control [8,9], and sliding mode [10]. Performances differ significantly according to selected modulator topology. The loop is shaped by considering the following important parameters: a consistent loop gain at all audio frequencies, high PSRR especially at lower frequencies to lower the demands of GSM burst rejection and a wide open-loop bandwidth to obtain a good transient response.

In today's systems, Class-AB amplifier solutions are still used for headset application in mobile phones in order to reach high audio performance specifications. Class-D amplifier is not the preferred candidate because it provides a poor audio

quality and a low power supply rejection with single ended power stage topology (imposed by headset connector) [11]. Recent objectives of Class-D research activities are aimed to find an efficient controller to minimize the error introduced by single ended power stage and prove the Class-D capability for headset solution. In such way, mobile phone market demand of up to 100 hour listening autonomy for headset application can be easily reached thanks to Class-D solution.

This paper presents novel controller architecture for single ended audio Class-D amplifiers using a variable hysteresis window. We prove in [12] that this solution is efficient for H-Bridge output stage. Here, the target of this paper, is to prove the performances of this structure (patent pending) for headset mobile application at low output power (<10mW).

The proposed control offers a state of the art combination of low idle power consumption, high power efficiency and excellent audio performance: 70dB PSRR, 0.01% THD at 10mW, and 98dB Dynamic Range (DR).

## II. PROPOSED TOPOLOGY

### A. Principle

The proposed architecture is presented in figure 1. The feedback signal is the output taken from the power stage before the passive low pass filter as for most solutions [4-10]. The control function integrates the difference between the output voltage and the reference audio signal  $V_{in}$ . The hysteresis block generates the differential PWM signal  $V_i$  in binary modulation.

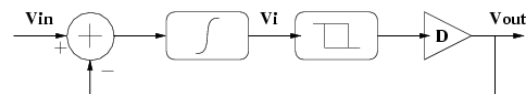


Figure 1: Block diagram of single end Class-D using hysteresis windows

The operating principle of this technique is the hysteresis control of the error signal  $V_i$ , given by:

$$V_i = -\frac{1}{\tau} \int_0^t (V_{in} - V_{out}) dt \quad (1)$$

To achieve the required feedback-loop condition for good Class-D behavior the error signal frequency must be higher than audio bandwidth.

### B. Modeling

Traditionally, Class-D amplifier designs use linear controllers combined with non linear architectures like pulse width modulation. The models used for this controller design are a result of subsequent simplifications including averaging the behavior of the system over time in order to avoid the modeling of the switching part.

However, standard linear analysis techniques cannot be used for our proposed architecture due to its non linear nature. In order to understand the behavior of this system, an ideal PSpice model has been developed. Following sessions will explain how all non linear components have been introduced into the model.

### C. Constant hysteresis control windows

The power supply rejection ratio is one of the most relevant characteristics for an audio amplifier in mobile phone [13]. As a matter of fact, its power supply is directly connected to the battery of the mobile devices that often contains system dependent noise. Most of consumers ask for a very high rejection for such kind of noise, most common specification is: PSRR>70dB@217Hz.

The prior works using the hysteresis topology integrate a constant hysteresis window. The bang-bang controller is realized based on usual Schmitt trigger (an op-amp with positive and negative feedbacks). Figure 2 shows the variation of hysteresis windows when the power supply voltage moves.

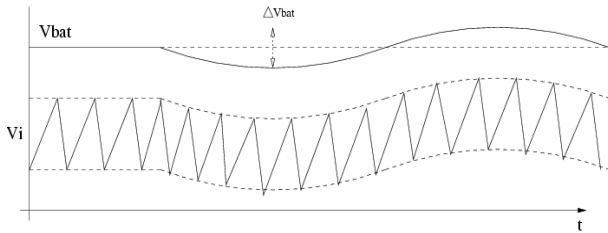


Fig. 2. Sliding surface and hysteresis windows when power supply varies

The integrated voltage  $V_i$  varies between the lower and upper windows at high frequency and follows also the frequency of power supply variation. The signal  $V_i$  can be simplify in two terms:

$$V_i = \bar{V}_i + \Delta V_i$$

In which  $\Delta V_i$  represents the HF variation and  $\bar{V}_i$  the variation in audio band due to the hysteresis common mode U.

For such reason this structure is not efficient to obtain a high PSRR.

### D. Variable hysteresis control windows

To solve this problem, the proposed method introduces a variable hysteresis window to improve power supply rejection. The boundaries of hysteresis window  $V_{min}$ ,  $V_{max}$  are centered on reference voltage  $V_{ref}$ :

$$V_{max} = V_{ref} + \alpha V_{bat} \quad \& \quad V_{min} = V_{ref} - \alpha V_{bat} \quad (2)$$

This approach avoids that error signal follows the supply ripple because of a constant common mode on hysteresis windows.

### E. Switching frequency

The switching frequency varies accordingly to modulation index mainly due to integration of a variable error, this result in a flatter slope. The switching frequency of Class-D based on presented hysteresis control, with variable windows width, is given by:

$$f_s = \frac{1 - M^2}{4 \cdot 2\alpha\tau} \quad (3)$$

In (3),  $M = V_{in}/V_{bat}$  is the modulation index (assuming  $V_{bat}$  as power supply),  $2\alpha$  is width of hysteresis windows and  $\tau$  is the integration time constant.

The effect of modulation index on Class-D switching frequency implies that audio signal level should be limited to a proper value in order to keep the switching frequency variation into allowed range [12]. This proposed approach has the advantage of spreading out of band energy (reducing EMI) due to the varying switching frequency. This leads also to improved power efficiency at high output levels. On the contrary, in case of stereo applications, the switching frequency difference between both channels can generate folding noise into audio band. Such effect can be greatly reduced with careful layout and substrate isolation.

### F. Performance of hysteresis control

The hysteresis control technique has several advantages compared to linear one (i.e. PWM architecture). Most important point is that's not suffering from bandwidth limitation. As a matter of fact, the loop bandwidth is equal to the switching frequency because the system has one cycle control time response. This means a theoretical infinite PSRR at DC; in reality, due to mismatch and finite opamp's GBW, a good supply rejection is achieved, making this solution very robust towards perturbations such as 217Hz burst noise in the GSM mobile phone.

Another advantage of the proposed solution is that doesn't need any carrier generators as required by PWM control. This is an effective improvement for system definition and current consumption.

Moreover, hysteresis control is stable by nature because the hysteresis window limits the error signal. All external circuitry variation and spreads have no impact in the stability.

### III. IMPLEMENTATION

The amplifier has been implemented in 0.13 $\mu\text{m}$  CMOS process (with high voltage transistors), and can be easily portable in other technology. The device operates with a single supply voltage range from 2.3V to 4.8V. The figure 3 shows the electrical schematic.

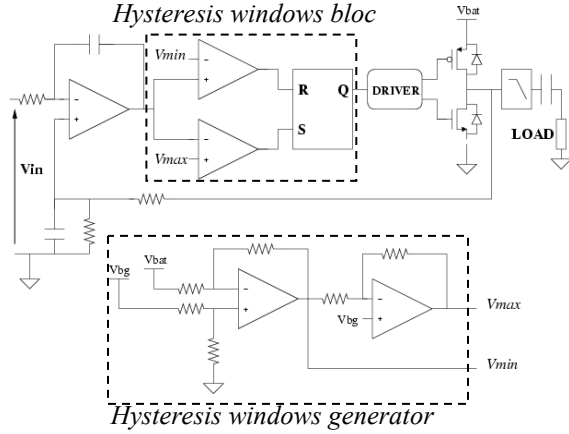


Figure 3: Electrical schematic of proposed solution

The hysteresis controller has to ensure a high PSRR performance, for such reason classical positive feedback solution has not been selected. In this design, the upper and lower hysteresis threshold voltages are created by the windows generation block: it's composed by two operational amplifiers and well matched resistors in order to provide a constant common mode window. Into hysteresis block, both comparators must be designed in order to obtain the fastest transient response: 10ns of switching delay at 20 $\mu\text{A}$  of static consumption as been achieved. RS latch is used to lock state after switching.

The width of hysteresis is process and temperature independent. The only remaining spread is due to resistor matching of hysteresis windows block.

The die micrograph of figure 4 shows the layout of one single ended amplifier with H-bridge output stage. The core area is 0.2mm<sup>2</sup>.

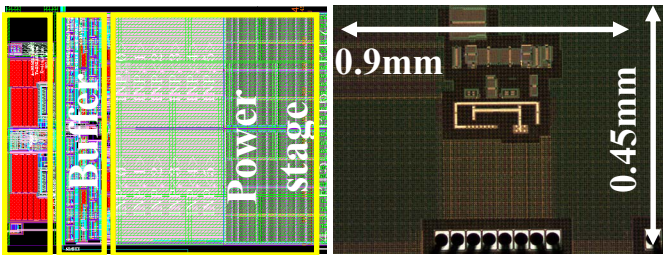


Figure 4: Layout & die micrograph

### IV. EXPERIMENTAL RESULTS

All measurements have been done with a single ended configuration (half of the H-bridge is not used and left intentionally OFF). The performance of Class-D prototype amplifier has been measured with 32 $\Omega$  load. The power supply used for most measurements is 3.6V. In order to

minimize the external component size, a small size inductor and capacitor is used. The inductance value is 2 $\mu\text{H}$ . All measurements have been done on Audio bandwidth: 20 Hz to 20 kHz at ambient temperature of approximately is 25 $^{\circ}\text{C}$ .

#### A. Harmonics distortion and noise

The THD+N is plotted versus output voltage level in fig. 5; the input frequency is 1kHz. All distortion from the power stage is suppressed by the feedback.

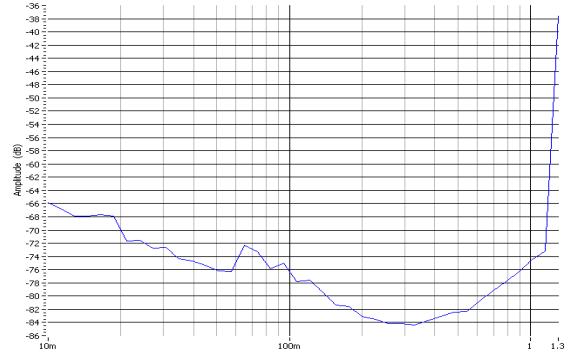


Figure 5: THD+N versus output level

Figure 6 shows THD versus frequency of input tone. Circuit achieves 0.01% THD at 6 kHz input signal frequency.

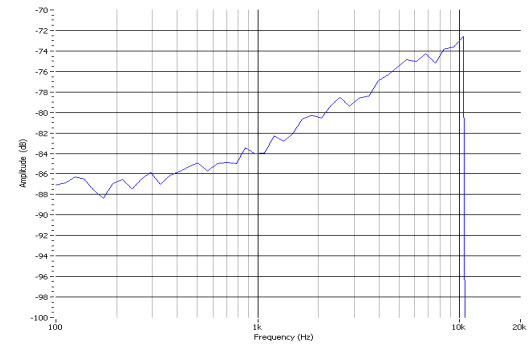


Figure 6: THD+N versus input frequency at 300mV<sub>rms</sub>

#### B. Power Supply Rejection for GSM burst

The power supply rejection is measured with a square wave of 600mV<sub>pp</sub> at 217 Hz, which stand for standard GSM emission perturbation, when a signal is present. The amplitude of input signal is 1V<sub>rms</sub> at 1 kHz. In this case, as shown on output spectrum in figure 7, PSRR is above 70dB (the highest component is below 90dB for a power perturbation of 20dB).

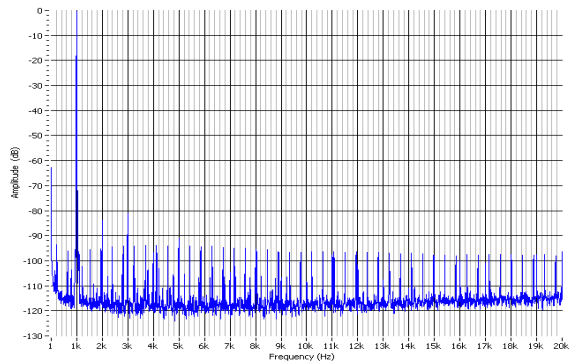


Figure 7: Output spectrum with GSM burst

Figure 7 measure shows how the main benefit of the proposed controller is the high PSRR due to loop bandwidth equal to switching frequency, even if the binary modulation is used (Single End configuration). In audio band, the distribution of the PSRR is the same as in a second order feedback control.

### C. Efficiency

The measured efficiency is 90% at full output power (500mW). At a low output power (average of 1mW for headphone), the power efficiency depends on the size of power stage ( $R_{on}$  and parasitic gate capacitance ratio) and the static current. The static consumption current of controller is smaller than 500 $\mu$ A. This previous characteristics increases battery life time for playback use cases in most mobile phones. However, the power stage in our proposed circuit is not optimized for 1mW power level ( $R_{on}=0.1m\Omega$ ).

### D. Performance Summary

A comparison of the performance of this audio amplifier with the ICs leading the market reveals that this design can be a serious alternative for headset application requiring high efficiency (table I). The main disadvantage of the class D solution is that extra filter components are needed at the output to decrease EMI.

In addition, thanks to high power supply rejection ratio and low current consumption (<500 $\mu$ A), the proposed circuit is suitable for portable devices with battery operations. Table 6 resumes performances of amplifier.

TABLE I. PERFORMANCE SUMMARY

Power Supply	2.3 to 4.8 V	
THD+N	P=1mW, R=32 $\Omega$	0.001%
	P=10mW, R=32 $\Omega$	0.01%
PSRR	100mV <sub>pp</sub> , 217Hz	70dB
	100mV <sub>pp</sub> , 10kHz	50dB
Dynamic Range	A Weighted	96dB
Controller consumption	V <sub>cc</sub> =3.6V, T=25°C	500 $\mu$ A
Switching Frequency	Average	450kHz
	[F <sub>min</sub> , F <sub>max</sub> ]	[350,700] kHz
Die Size	CMOS 0.13 $\mu$ m	0.2mm <sup>2</sup>

## V. CONCLUSION

In this paper a new hysteresis control with a variable window has been proposed to correct efficiently a single ended power stage non linearity. Key factors of this work are:

low voltage and low power functionality, a quite good PSRR (70 dB), high linearity (0,001%) and SNR (97 dB) with low current consumption. The next objective of Class-D research is to supply the circuit with symmetrical power supply to avoid coupling capacitor for the load.

## ACKNOWLEDGMENT

The authors gratefully acknowledge STMicroelectronics and Lyon Institute of Nanotechnology (INL) that sponsored this work. We would also like to acknowledge the design team of Advanced Audio IP's: E. Allier, F. Amiard, V. Binet, P. Marguery.

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