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A FULLY DIFFERENTIAL DIGITAL INPUT CLASS D WITH EMI SPREADING METHOD FOR MOBILE APPLICATION

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Class D audio amplifiers are widely used in embedded system to achieve high efficiency. Digital class D accepts bit stream as input signal to drive loudspeaker. Major drawbacks of such systems are the non linearity due to the switched behavior and EMI radiations issued from the output low pass filter. This paper presents a digital class D amplifier with a local analog feedback loop to improve performances of the power stage and digital method to spread output spectrum in order to reduce EMI radiation. The amplifier, including digital modulator and analog power stage, was integrated in a single chip in 0.13 μm CMOS technology. The silicon results confirm the validity of the theoretical analysis.

INTRODUCTION

Digital input class D (DD) amplifiers do not require any high end digital to analog conversion before the power stage, which improved the total efficiency of the amplifier (Fig. 1). Unlike Analog Class D (AD) where Pulse Width Modulation (PWM) is done inside the analog power loop, the input of DD is already modulated by digital PWM. This approach removes the generation of high frequency analog carrier which introduced non linearity and increase distortion of AD [1-2]. In DD, there are also non linearity introduced by digital PWM, but digital solutions are possible to reduce them.

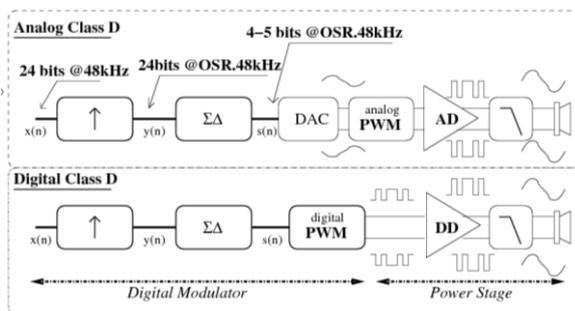


Figure 1: Analog and Digital class D

The other major drawback of class D amplifiers is Electro Magnetic Interferences (EMI) due to radiation of high frequency component of the output signal

spectrum through the low pass filter self. AD and DD both have high frequency components at modulation signal frequency. In order to reduce EMI, a solution to spread the EMI is also presented in this paper.

1 DIGITAL MODULATION

In mobile application, the audio input signal comes from the digital base band or a digital codec (voice, mp3 decoding ...) and its resolution is usually 24 bits sampled at 48 kHz. This signal can be directly modulated in a bit stream to drive the DD. This solution, named direct PWM, as majors flaws as explained in the next subsection.

1.1 Limitations of the direct PWM solution

1.1.1 Limited frequency of PWM reference

As shown on Fig. 2, direct PWM involved the use of digital saw tooth signal as reference in order to create a bit stream from the digital input.

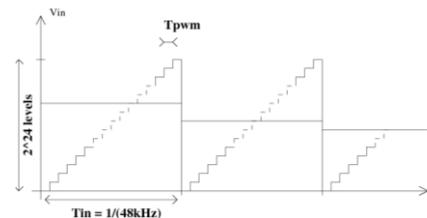


Figure 2: Digital PWM frequency limitation

The quantum generation frequency of the saw tooth signal can be expressed as:

$$F_{pwm} = 2^n \cdot F_s \quad (1)$$

Where n is the resolution of audio input signal and F_s is its sample frequency. In standard mobile application, as seen before, the resolution is 24 bits and sample frequency is equal to 48 kHz. These values drive to a frequency of 805 GHz.

Obviously, such value of frequency is unreachable in standard CMOS technologies.

1.1.2 Linearity of digital PWM

Due to sampled nature of audio signal, the digital PWM (called UPWM – Uniform PWM) introduced error in comparison with the analog PWM (called NPWM – Natural PWM) (Fig. 3) [2]. The more the sample frequency of audio signal is high, the less the error is important. NPWM is like UPWM with infinite sample rate.

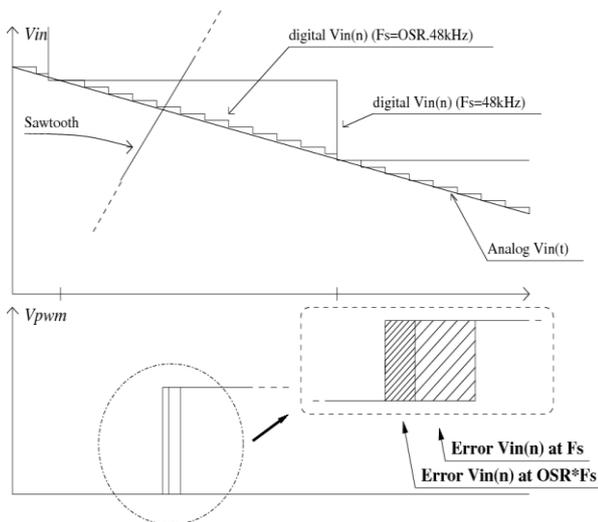


Figure 3: Effect of OSR on error in digital PWM

The digital audio signal can be over sampled by Over Sampling Ratio (OSR) to improve linearity of UPWM.

In case of differential digital modulation, which means that V_{in} is divided in two channel, the error done by one channel is corrected by the other channel.

1.2 Increasing linearity and SNR of modulation using $\Sigma\Delta$ modulation

These flaws of direct PWM are corrected by using a $\Sigma\Delta$ modulation before the digital PWM. The $\Sigma\Delta$ modulation consequences are:

- The over sampling of the digital signal, which increase linearity of UPWM as seen before.

- The reduction of signal resolution from 24 bits to m bits (generally, m value is between 1 and 5), which makes the quantum of PWM saw tooth reachable (for example, if output of the $\Sigma\Delta$ modulator is coded with 5 bits, which is actually worst case, $F_{pwm} = 2^5 \cdot 48k = 1.5MHz$).
- The shaping of the $\Sigma\Delta$ quantification noise over the audio band.

Choice of OSR, output resolution m , order k and structure (simple, pipe line, MASH, CRFB...) of the $\Sigma\Delta$ modulator is depending on performance and Noise Transfer Function (NTF) needed by the application. Tradeoffs between performances and complexity (stability issue and global consumption) have to be found.

The $\Sigma\Delta$ modulator used in this design is a 4th order MASH 2-2 5 bits structure, with OSR = 48 (Fig. 4). Its coefficients are computing [3] from the desired NTF.

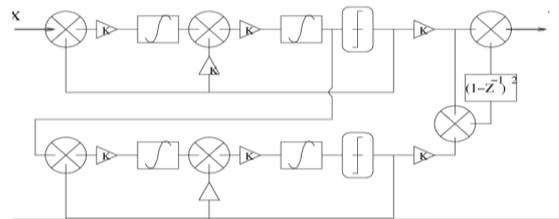


Figure 4: Structure of MASH 2-2 $\Sigma\Delta$ modulator

The output of this circuit can be written as (2).

$$Y(z) = X(z) \cdot z^{-4} + g_1 \cdot E_2(z) (1 - z^{-1})^4 \quad (2)$$

Where $X(z)$ and $E_2(z)$ are z transform representations of input signal and second quantiser error respectively. g_1 is a digital multiplier which compensates for the scaling factors. NTF of this $\Sigma\Delta$ modulator is shown on Fig. 5. The Curve (A) is the original one whereas curve (B) is corrected NTF to reduce HF gain.

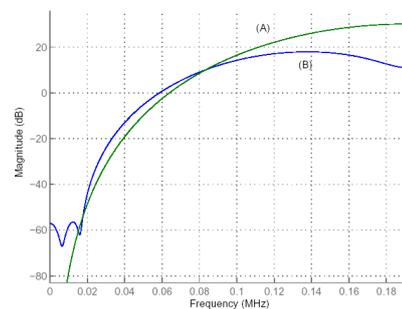


Figure 5: NTF of MASH 2-2 4th order 5 bit $\Sigma\Delta$ modulator

2 DIGITAL POWER AMPLIFIER

2.1 Limitations of open loop power stage

The modulated bit stream is able to drive directly the loudspeaker through a CMOS power stage (Fig. 6). This configuration, called *open loop digital class D*, has unacceptable issues with Power Supply Rejection (PSR) and linearity. Indeed, the perturbation presents on supply rail feed directly the load as output node is not controlled. In addition, to avoid crossover in CMOS power stage between plus supply to minus supply during switching time, a no overlapping delay is introduced and decreases linearity of amplifier.

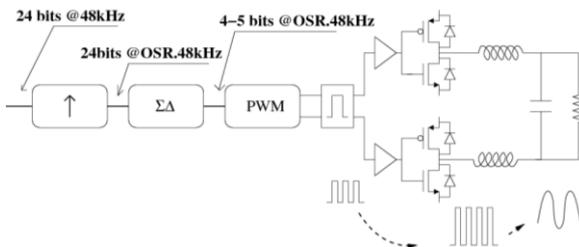


Figure 6: Open Loop digital class D amplifier structure

The power stage errors have to be corrected by an efficient control loop.

2.2 Control loop for digital class D

2.2.1 State of the art

To achieve good PSR and increase linearity of power stage, a local feedback loop can be used. In [4], a solution with an algorithm which compares input and output bit stream and feed a corrector is proposed. Another solution, described in [5], consist in a $\Sigma\Delta$ modulation of supply variation introduced in UPWM modulation of audio signal to increase PSR. This solution reach to good PSRR (PSR Ratio), but there is not correction of linearity, and THD is not good enough for high end mobile application. In [6-7], a mixed correction, both analog and digital, is proposed. This solution achieves good performances in high power amplifier, but it's not suitable for low power amplifier due to high static consumption of control loop.

2.2.2 Local analog loop for digital class D

The control of the power stage is done with a PowerDAC [8] solution. The basic analog loop, called Phase Control Loop (PCL) is shown on Fig. 7.

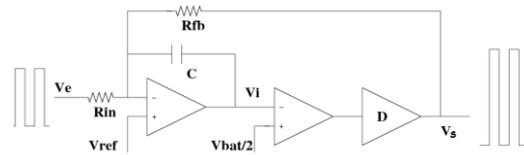


Figure 7: Phase Control Loop schematic

In steady state, the signals V_{in} , V_{out} and V_i are represented on Fig. 8.

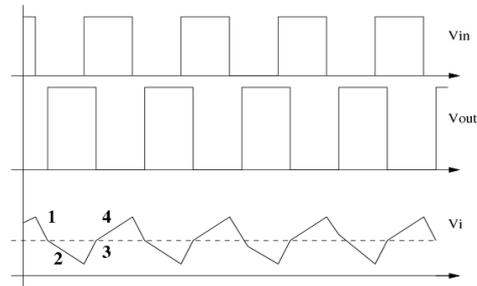


Figure 8: Main Signal of PCL

The behavior of such loop can be studied in four distinct phases, due to pseudo digital nature of signals V_{in} and V_{out} . During a single phase, V_{in} and V_{out} are constant voltages so R_{in} and R_{fb} are like constant current sources which charge or discharge C . Depending of the phase (1 to 4 – see Fig. 8), R_{in} and R_{fb} are current sources or sinks. For example, in phase 1, both R_{in} and R_{fb} are current sources, so U_C is increasing linearly and V_i is decreasing linearly too as $U_C = V_{ref} - V_i$.

Phase 1 and 3 are called *working phases* because the output voltage is different of input voltage, whereas phases 2 and 4 are called *waiting phases* because the loop is waiting for a new input event.

To work correctly, evolution on V_i must not changes when output signal changes. Indeed, at the end of phase 1, V_{out} voltage goes from V_{bat} to Gnd , which obviously changes R_{fb} current source in current sink. If this sink is higher than R_{in} current sources, evolution on V_i voltage switches and the loop, instead of going in *waiting phase*, switched again (Fig. 9). The same issue is possible at the end of phase 3.

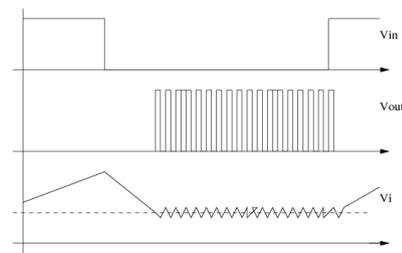


Figure 9: Instability on V_i due to wrong balance of current sources

To avoid large signal instability at the end of phase 1 and 3, the following relation must be respected:

$$\frac{R_{fb}}{R_{in}} \geq \frac{V_{bat}}{V_{ana}} \quad (3)$$

Where V_{bat} is the power stage supply and V_{ana} is the digital modulator supply. The ratio R_{fb}/R_{in} is the gain of the analog loop and in most of the case, power supply is higher than logic supply.

Theses conditions involve that the analog loop must have a minimum gain which is the ration of supplies to be stable.

In addition, to insure good linearity, phases 1/3 and 2/4 must be as symmetrical as possible. This condition gives ideal value of reference voltage V_{ref} :

$$V_{ref} = \frac{1}{2}V_{bat} \frac{R_{in}}{R_{fb} + R_{in}} + \frac{1}{2}V_{ana} \frac{R_{fb}}{R_{fb} + R_{in}} \quad (4)$$

The mathematic calculus of the condition of linearity drives to a result which is logical. Indeed, the common mode of input amplifier is the pondering average of input common mode ($V_{ana}/2$) and output common mode ($V_{bat}/2$).

Small signals model of this loop, with modeling power stage and commutation stage by a single gain [9] allow understanding of how the loop gain affects PSRR and linearity. In order to increase audio performances, the simple pole is replaced by a double pole, which increases the gain in low frequency, such as audio band and do not change anything in high frequency.

Two solutions of double pole structure are possible: a single amplifier with two pole feedback loop (Fig. 10) or two cascaded amplifiers with each one a single pole feedback loop (Fig. 11).

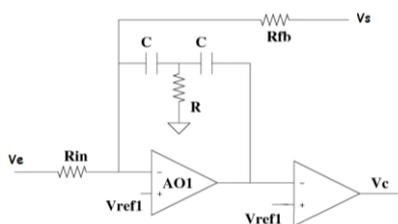


Figure 10: PCL with one amplifier - double pole schematic

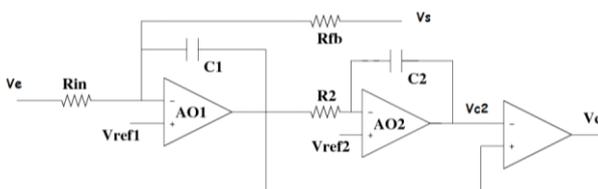


Figure 11: PCL with two amplifiers – two single poles schematic

Hence, output voltage of integrator has as expression in both cases:

$$V_{C1}(p) = -\frac{1+2RCp}{R_{in}RC^2p^2}V_{in}(p) - \frac{1+2RCp}{R_{fb}RC^2p^2}V_{out}(p) \quad (5)$$

$$V_{C2}(p) = -\frac{1+2RCp}{R_{in}R_2C_1C_2p^2}V_{in}(p) - \frac{1+2RCp}{R_{fb}R_2C_1C_2p^2}V_{out}(p)$$

If $C_2=C$, $R_2=2R$ and $C_1=C/2$, the two approaches have the same small signals behavior. The second solution reduces bandwidth constraints and is not sensible to the noise from AO1, but needs two amplifiers.

3 EMI SPREADING

In BTL configuration, when three levels modulation is used, there is two ways to have a null output voltage: both channels output are '1' or '0' as shown on figure 12.

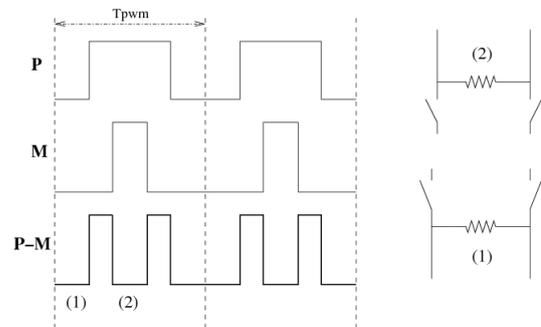


Figure 13: BTL - Three level modulation output

In order to spread HF spectrum of output, the states (1) and (2) are randomly swap, which add distortion on each single channel but do not change in any way the differential signal (P-M) which drives the load (figure 13). The decision of swapping the two channels is chosen by a single bit every half saw tooth period.

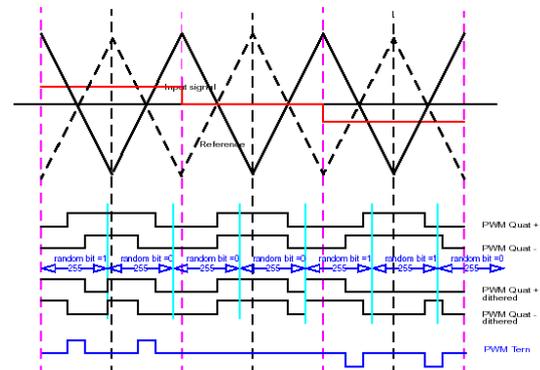


Figure 13: BTL - Three level modulation output with EMI reduction

The spectrums of each signal are shown on figure 14, 15, 16 and 17. There is no variation on the BTL signal (16), but each channel's HF spectrum is spread (14 and 15). Thus, the electro magnetic radiation from low pass filter's self are decreased. The global amount

of energy present in HF modulation stays the same in the two cases, but the frequency distribution of this energy is quite different.

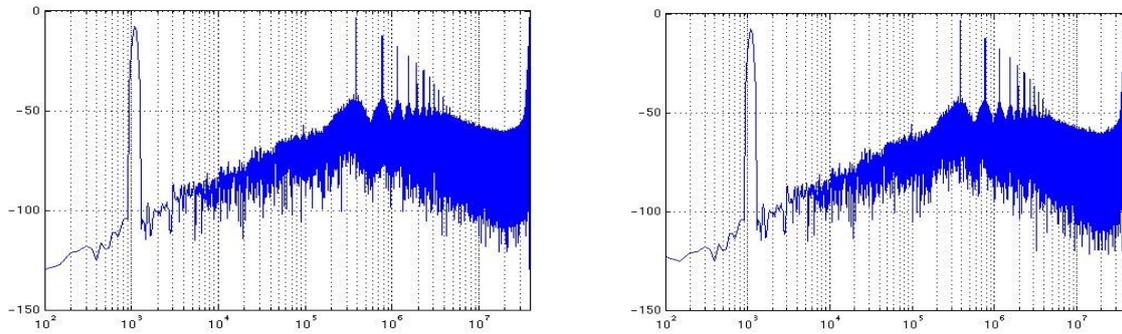


Figure 14: Simulated spectrum of N and P channel output without swapping

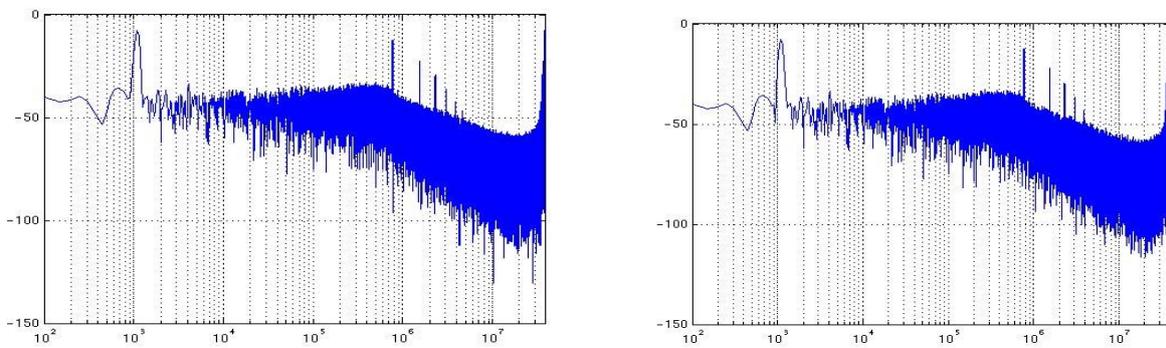


Figure 15: Simulated spectrum of N and P channel output with swapping

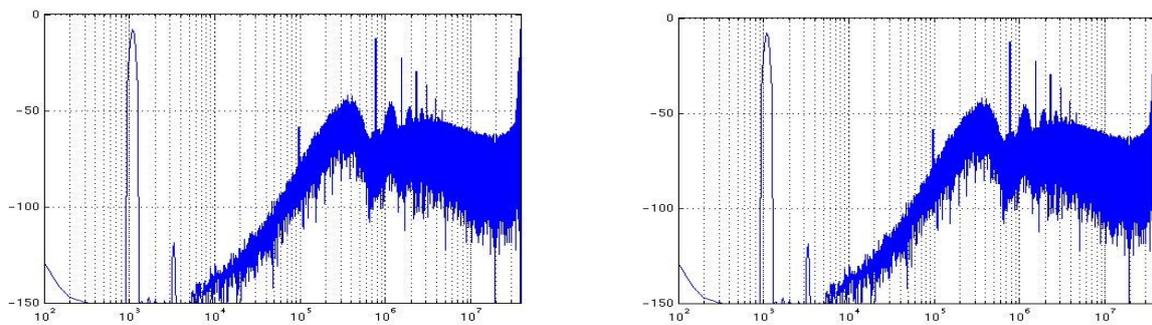


Figure 16: Simulated spectrum of differential output with and without swapping

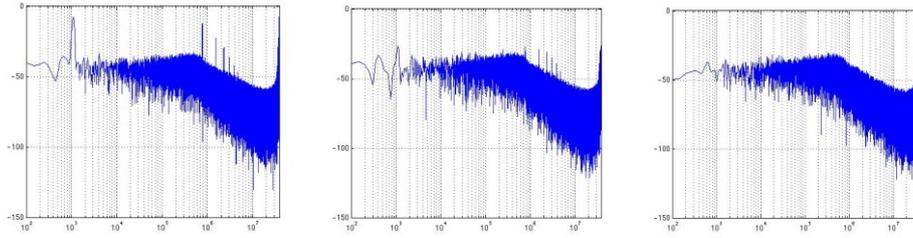


Figure 17: Simulated spectrum of P output with swapping at different input level (-4, -24 and -64dB)

Figure 17 shows that swapping method benefits are much more evident at low input level which is the main application of such an amplifier.

This solution increases the switching frequency of each power stage, and so decreases the global efficiency of the class D amplifier. The power lost during switching can be expressed as [10]:

$$P_{LOST} = 2 \times \left(C_{eq} V_{bat}^2 F_{PWM} + \frac{V_{bat}^2 (t_f + t_r)}{R} F_{PWM} \right) \quad (6)$$

Where C_{eq} is the equivalent gate capacitance of power stage transistors, V_{bat} is the power supply, R is the resistive load, t_f and t_r are the fall and rise time of transistor and F_{PWM} is the switching frequency. In embedded application [11], $C_{eq} = 100\text{pF}$, $V_{bat} = 3.6\text{V}$, $R = 8\Omega$, $t_f = t_r = 2\text{ns}$ and $F_{PWM} = 400\text{kHz}$, which give $P_{LOST} \approx 2\text{mW}$. With the spreading proposed method, F_{PWM} could be at maximum twice higher than previous case, which could double P_{LOST} . The output power of our application is about 700mW, so the global efficiency is theoretically decreases by 0.5%.

In order to reduce EMI radiation, another solution consists in reducing the rise and fall time of the power stage [11], but this approach reduces efficiency more drastically than the previous method and the cross conduction current can be an issue.

4 DESIGN OF DIGITAL CLASS D

Figure 18 shows layout of digital class D. The digital modulator has a size of 2.3 mm². Each channel power stage size is 0.5 mm².

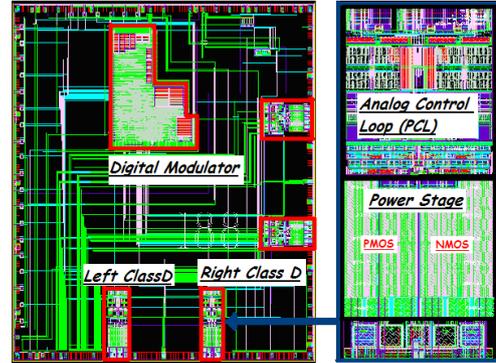


Figure 18: Layout of Digital Class D: Full chip (Left) & Zoom on PCL + Power Stage (Right)

5 PRACTICAL CHARACTERISATION

The performances of class D prototype amplifier were measured using audio analyzer (UPD). Unless otherwise noted, assume the following measurement conditions:

- 8 Ω load and {L,C}={20μH, 20nF} in LC filter
- THD and noise measurement at load
- 20Hz to 20kHz measurement bandwidth
- Ambient temperature at 25°C approximately

Figure 19 shows the output's FFT in response to 1 kHz sine wave input with amplitude of -20dB and power supply of 3.6V. In this case, THD is equal to 75 dB (0.02 %). With A-weighted filters, which stand for ears sensibility, THD became superior to 80 dB.

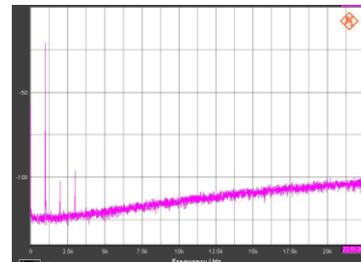


Figure 19: FFT of output signal @1kHz FS

Figure 20 shows how leveled THD+N (THD including noise) varies with input level at 1kHz. Just

before saturation (i.e. $V_{in} > V_{bat} = 3.6V$), at Full Scale, THD is equal to 75 dB. SNR can be measured at -60dB FS ($V_{in}=3.6mV$) and value is 86 dB.

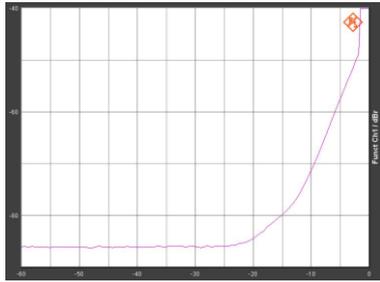


Figure 20: Levelled THD+N versus Vin (dBFS)

PSRR is measured with square wave of $300mV_{pp}$ (i.e. -20dB FS) at 217 Hz, which stand for GSM emission perturbation. In this case, as shown on figure 21, PSRR is above 60 dB.

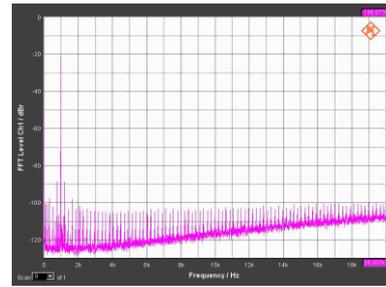


Figure 21: FFT of output signal @ 1 kHz + 217 Hz power supply variation

Figure 22 shows HF output spectrum of one (P) channel with and without EMI spreading method. The swapping method add distortion on each single channel, as shown on the right spectrum, but minimize the harmonic on saw tooth frequency.

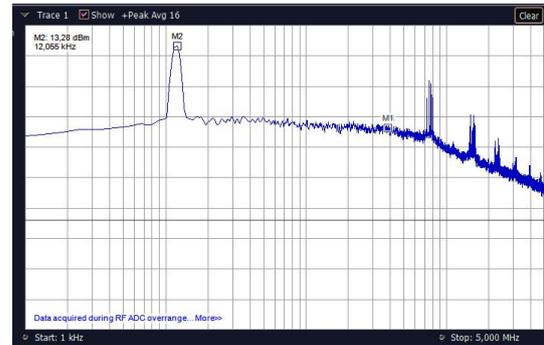
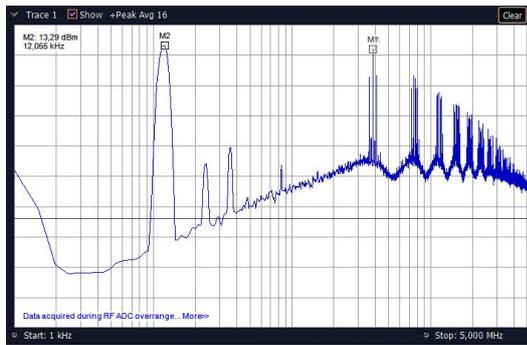


Figure 22: HF P channel output signal spectrum without and with swapping

Figure 23 shows efficiency with (full line) and without (dashed line) spreading method. As supposed, the efficiency is not significantly impacted by the spread of EMI.

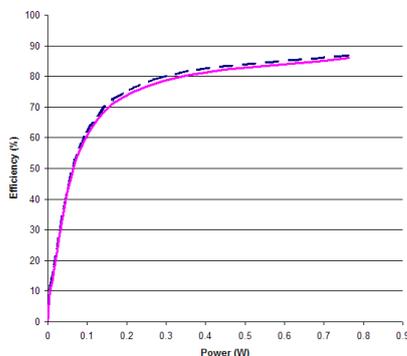


Figure 23: Efficiency vs Output Power

For a typical music crest factor, which is -12dBVrms or -24dB from full output power, the efficiency is decrease from 54% to 53.4%.

Figure 24 shows output intermodulation between two sine wave input : 200 Hz and 2kHz, both FS. From this measurement, IMD factor can be calculated as the ratio of magnitude of the sum and difference signals to the original input signal [12].

$$IMD = \frac{\sqrt{\sum_{k=-\infty}^{\infty} V_{f_2+kf_1}^2}}{V_{f_2}} \quad (7)$$

Where V_{f_2} is the voltage at the input frequency f_2 , etc...

The measured IMD factor value is here, with $f_2 = 2kHz$ and $k=\{-2;2\}$, is 0.015%.

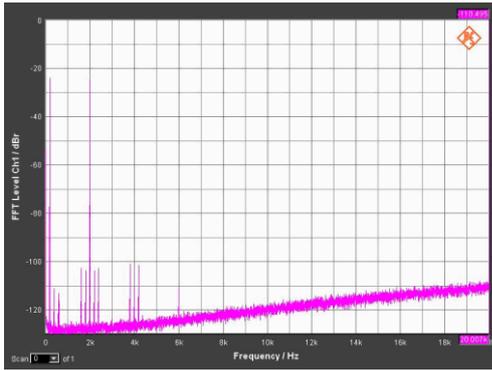


Figure 24: FFT of output signal @200Hz+2kHz FS

6 CONCLUSION

This paper has described a digital class D amplifier with digital $\Sigma\Delta$ PWM modulator and analog local feedback loop. The digital modulator and the analog drivers both are integrated in CMOS 0.13 μ m on a single chip. A random digital noise is added in the modulator in order to spread the EMI of the output signal. The method to spread EMI is useful in case of electromagnetic sensibility of the amplifier's environment, such as in mobile phone power management chip.

The audio performances of our amplifier are in line with actual state of the art (THD < 0.05%, SNR > 80 dB and PSRR > 60 dB).

The stability condition was studied for the local analog control loop of the power stage and a condition between the audio gain and the supply was found.

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