Current-mirror based PID controller

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***Abstract*—in this paper, the architecture of the Proportional-Integration-Derivative (PID) controller, based on the current-difference amplifier, is presented. This architecture allows to integrate the controller, employing only four active MOS transistors. It also allows obtaining interesting features, such as the low power-consumption, and high bandwidth, in spite of the low DC accuracy. In this paper, design equations for the DC operation point setting, transfer function, and the MOS transistor sizing are provided. The performances are demonstrated by a simulation of the circuit designed in 40nm CMOS, employed to stabilize the feedback-loop of switched DC/DC buck converter.**

I. Introduction

In the design of continuous-time PID-like controllers, various structures based on the active elements can be used. For instance, [1] presents the overview of the voltage mode (voltage input/output) PID controllers, based on the operation amplifier, OTA, and CCII. Alternatively, current mode controllers recently emerged in literature, based *e.g.* on the CCII, CDTA or grounded synthetic inductance (see [2 - 4] for instance). The common factors of merit of a controller are the power-consumption, frequency bandwidth, offset, and DC gain.

In this paper, the circuit reaching interesting power consumption vs. frequency bandwidth trade-off is presented. The structure is based on the current-difference amplifier (CDA) which can be implemented by only two simple current mirrors [2]. The circuit does not require the frequency compensation, which allows to extend the frequency bandwidth. This might be advantageous compared to the operation amplifier based counterparts [1]. On the contrary, the structure exhibits inherently higher DC offset, due to the lower current mirrors accuracy (mismatch). On this account, the controller is intended mainly for devices requiring a high-quality (fast) regulation, while admitting a DC offset in the order of tens of milivolts. Developed application concerns the power-supply chain of the audio and RF power amplifiers.

This article is organized in four parts. In *section II*, the concept of controller based on the ideal CDA is presented. In *section III*, the AC and DC analyses of the current-mirror based PID controller are provided. *Section IV* relates the transistor sizing to the DC controller gain, and the last section provides an example of the controller designed in 40nm CMOS, applied to the switching step-down DC/DC converter.

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II. Basic Concept of the Controller

The current-difference amplifier CDA provides the difference of input currents I_1 and I_2 in such a way that $I_{OUT} = F(I_1 - I_2)$, where F is usually set to unity. However, while using the CDA as the voltage-mode PID controller, the conversion of the input/output voltages to the currents with appropriate dynamics (PID) is required. This can be obtained by the circuit shown in *Fig. 1*, where the input (reference) and feedback currents I_{REF} and I_{FB} are generated by means of R_{REF} and Z_1. The output voltage occurs across the impedance Z_2.

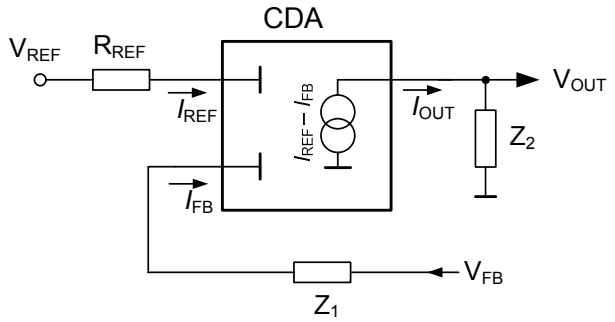

Figure 1. Idealized schematics of the controller.

The values of reference and feedback currents I_{REF} and I_{FB} in *Fig. 1* controller circuit can be expressed as:

$$I_{REF} = \frac{V_{REF}}{R_{REF}} \quad \text{and} \quad I_{FB} = \frac{V_{FB}}{Z_1} \tag{1}$$

where V_{FB} refers to the regulated (feedback) voltage. Since the output current results from the current difference $I_{REF} - I_{FB}$, the output voltage of the controller can be revealed as:

$$V_{OUT} = \left(I_{REF} - I_{FB}\right) \cdot Z_2 = \left(\frac{V_{REF}}{R_{REF}} - \frac{V_{FB}}{Z_1}\right) \cdot Z_2 \tag{2}$$

We can therefore express the condition of steady-state regulation:

$$I_{REF} - I_{FB} = 0 \tag{3}$$

The manner to design the impedances Z_1, Z_2 then allows to attain the control regulation condition with the appropriate dynamics of the controller: PD, PI, PID or derivative filtered PID, see [1, 3].

III. CURRENT-MIRROR BASED CONTROLLER

The circuit representing the controller based on two-current mirrors CDA [2] is shown in *Fig. 2*. Compared to *Fig. 1*, the CDA from *Fig. 2* has to be considered as non-ideal, due to the nonzero input impedances $1/g_m$ and $1/g'_m$ of the current inputs.

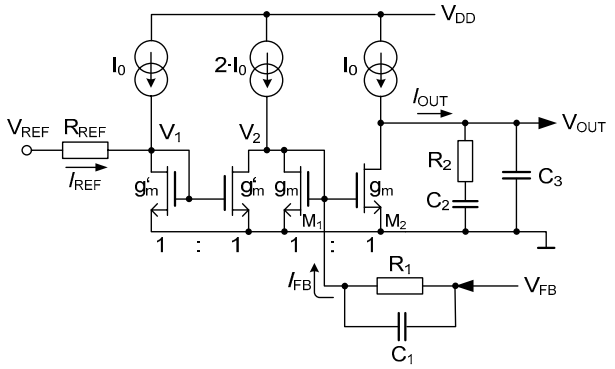

Figure 2. PID (type-3) controller based on two-current mirrors CDA. In the following, we consider all transistor W/Ls identicall.

In this idealized schematic, we distinguish two mentioned current mirrors, reference current source resistance $R_{REF}+g'_m$ impedance Z_1 containing R_1, C_1, g_m, and impedance Z_2 composed of R_2, C_2, and C_3. The current sources are designed in order to provide the zero output current I_{OUT} in the steady-state (3).

A. Transfer Function, Components Values

The transfer function of the PID controller can be expressed *e.g.* in the general zero-pole form [1]:

$$C(s)=K\frac{(s/z_1+1)(s/z_2+1)}{s\cdot(s/p_1+1)(s/p_2+1)} \tag{4}$$

where z_n refers to the real controller zeros, and p_n to the real pole frequencies (all in rad/s). An alternative type of controller (PI, PID, and derivative filtered PID) can be obtained by the appropriate selection of z_n and p_n (see [1], [3] for more details).

The small-signal analysis of the circuit shown in *Fig. 2* reveals the transfer function V_{OUT}/V_{FB} in the following zero – pole form:

$$\frac{V_{OUT}}{V_{FB}}=\frac{-g_m(1+sC_2R_2)(1+sC_1\cdot R_1)}{s\cdot(1+R_1g_m)(C_2+C_3)\left(1+sR_2\frac{C_2C_3}{C_2+C_3}\right)\left(1+s\frac{C_1R_1}{R_1g_m+1}\right)} \tag{5}$$

where g_m is the transconductance of transistor M_1:

$$g_{m(M1)}=\sqrt{2KP(W/L)I_0} \tag{6}$$

The values of the passive components from *Fig. 2* circuit can be found by solving the set of linear equations obtained by comparing the coefficients of transfer functions (4) and (5):

$$R_1=r_1 \quad R_2=\frac{KR_1p_1p_2}{z_2(p_1-z_1)(p_2-z_2)} \quad C_3=\frac{z_2(p_1-z_1)}{KR_1p_1p_2}$$
$$C_1=\frac{1}{z_1R_1} \quad C_2=\frac{(p_1-z_1)(p_2-z_2)}{KR_1p_1p_2} \quad g_m=\frac{p_1-z_1}{z_1R_1} \tag{7}$$

where r_1 is an arbitrary selected value related to the impedance level. In this choice of r_1, we focus namely on the:

- value of I_{REF}: minimize, in order to reduce the current from V_{REF}. Its low value also increase the tracking capability,
- minimization of g_m (results from (7) and is related to the transistor size and power consumption, see *Eq*. (6))
- realistic value of C_3.

Notice: As for an controller PID based on the OTA [1], the transfer function V_{OUT}/V_{REF} differs from (5):

$$\frac{V_{OUT}}{V_{REF}}=\frac{g_m(C_2R_2s+1)}{s\left(sR_2\frac{C_2C_3}{C_2+C_3}+1\right)(C_2+C_3)(1+R_{REF}g_m)} \tag{8}$$

The transfer function (8) has to be considered in some specific regulation schemes, namely when the fast tracking capabilities are required by the system.

B. DC Transfer Function

The value of R_{REF} can be found by applying the steady-state regulation condition $I_{REF}=I_{FB}$ (3). Due to the non-constant tracking gain V_{FB}/V_{REF}, R_{REF} is to be determined for each single reference voltage V_{REF}. In practice, R_{REF} can be found by the iterative DC simulation. In this paragraph, we point to the complicated, but closely linear relationship between R_{REF} and tracking gain V_{FB}/V_{REF}. In order to determine the steady-state currents I_{REF} and I_{FB}, we refer to the 1st order quadratic equation of an MOS [2]:

$$I_D=\frac{\beta}{2}\left(V_{GS}-|V_{TH}|\right)^2 \tag{9}$$

where I_D is the drain current, $\beta=KP\cdot W/L$ is the transistor gain, V_{TH} the threshold voltage, and V_{GS} the gate-to-source voltage. Condition $I_{REF}=I_{FB}$ can be then expressed in terms circuits' components values of *Fig. 2*:

$$\frac{V_{REF}-V_1}{R_{REF}}=\frac{V_{FB}-V_2}{R_1} \tag{10}$$

As the steady-state drain current of M_1 is I_0, the nodal voltages V_1 and V_2 result from (9):

$$V_1=\sqrt{\frac{2(I_{REF}+I_0)}{\beta}}+V_{TH}\ ; \quad V_2=\sqrt{\frac{2I_0}{\beta}}+V_{TH} \tag{11}$$

and the value of current I_{REF} results from (11) as:

$$I_{REF}=\frac{1}{R_1}\left(V_{FB}-\sqrt{\frac{2I_0}{\beta}}-V_{TH}\right) \tag{12}$$

These equations yield the following value of R_{REF}:

$$R_{REF}=\frac{R_1\sqrt{\frac{\beta}{2}}(V_{TH}-V_{REF})+\sqrt{R_1\left(V_{FB}-V_{TH}-\sqrt{\frac{2I_0}{\beta}}+I_0R_1\right)}}{\sqrt{\frac{\beta}{2}}(V_{TH}-V_{FB})+\sqrt{I_0}} \tag{13}$$

From this equation, the nonlinear tracking gain V_{FB}/V_{REF} can be evaluated. A curve presenting the example of the tracking gain of the controller presented in *section V* is shown in *Fig. 3.*

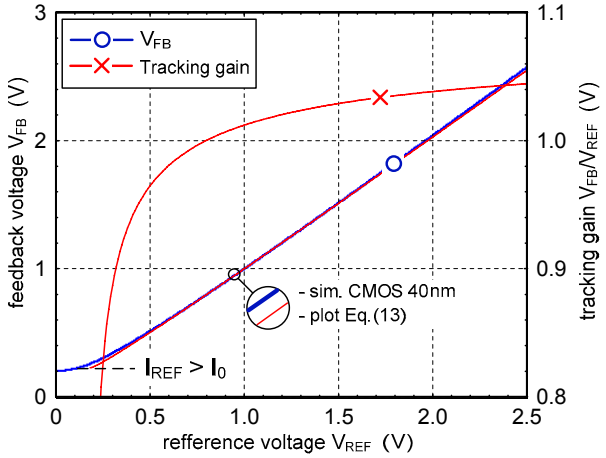

Figure 3. Simulated and calculated tracking characteristic and tracking gain, provided on the design example from *section V*.

IV. DC Gain and Transistor Sizing

In reality, the ideal infinite gain of the controller G_{DC} is reduced by the drain conductances of M_2 and I_0 current sources g_{dso} and $g_{dso,P}$. This maximal gain is comparable *e.g.* to OTA controller PID, being in order of 40dB. The value of the controller gain is related to the regulation accuracy of the closed loop [3] (see *section V*).

In order to evaluate the value of G_{DC}, we can build the small signal scheme of the controller shown in *Fig. 4*.

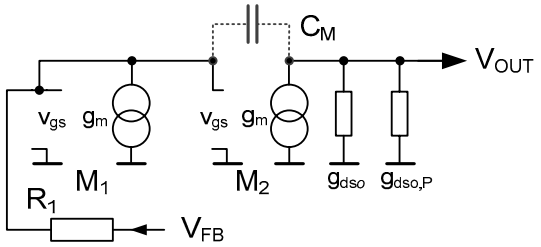

Figure 4. Simplified small signal model of the controller.

The analysis of the linearised circuit allows to obtain the value of G_{DC} as the function of g_m and g_{dso}:

$$G_{DC} = \frac{\partial V_{OUT}}{\partial V_{FB}} = \frac{-g_m}{(g_{dso} + g_{dso,P})(R_1 g_m + 1)} \qquad (14)$$

where $g_{dso} \approx \lambda_0 I_0/(L \cdot V_{DS})$ (λ_0 refers to the channel length modulation of the output transistors, [2]). The (14) can be rewritten in terms of the parameters of the transistor (we neglect the influence of the current source conductance $g_{dso,P}$:

$$G_{DC} = -\frac{\sqrt{2KP_N \frac{W}{L}}}{\frac{\lambda_{0n}\sqrt{I_D}}{V_{OUT} L}\left(R_1\sqrt{2KP_N \frac{W}{L} I_0} + 1\right)} \qquad (15)$$

This expression can be used to evaluate the trade-off between G_{DC}, $L_{(M1)}$, and I_0. Example of this dependency is plotted in *Fig. 5* (see also example in *section V*).

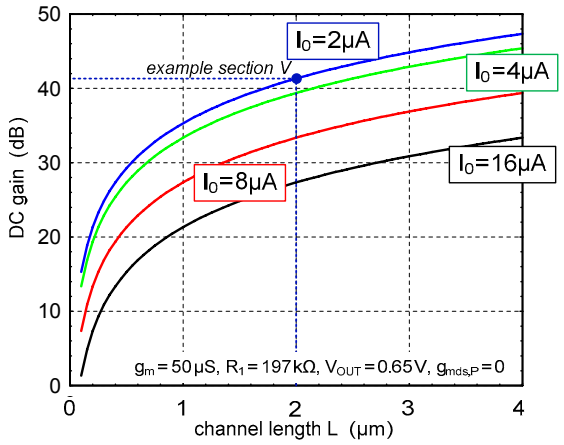

Figure 5. Impact of I_0 and transistor channel scaling to DC gain.

From this figure, we notice the impact of the bias current I_0 on the G_{DC}. The lowest value of I_0 is limited by the required transistor operating regime (saturation), and also has an important impact to the maximal frequency bandwidth as well as the positive slew-rate of the controller.

V. Design Example

Performances of the circuit are demonstrated by the example of design in 40nm CMOS (2.5V). The design aims to stabilize the feedback loop of the switched-mode step-down (buck) DC/DC converter. In the 1st order approximation, the step-down DC/DC converter can be modeled as the linear dynamic system, composed of the controller, LC filter, and constant gain G, shared between PWM modulator and output stage (see block scheme in [4]). For our design example, we consider the following parameters of the converter: $L = 0.47\mu H$, $C = 10\mu F$, $R_L = 150m\Omega$, $R_{ESR} = 20m\Omega$, $G = 4$ and we require the operating point $V_{REF} = V_{FB} = 1V$. The process parameters for the design were obtained by the least-squares approximation of the transistor I/V characteristics [8] as: $KP_N = 134\mu V/A^2$, $V_{THN} = 0.542V$ and $\lambda_{0n} = 32mV \cdot \mu m^{-1}$.

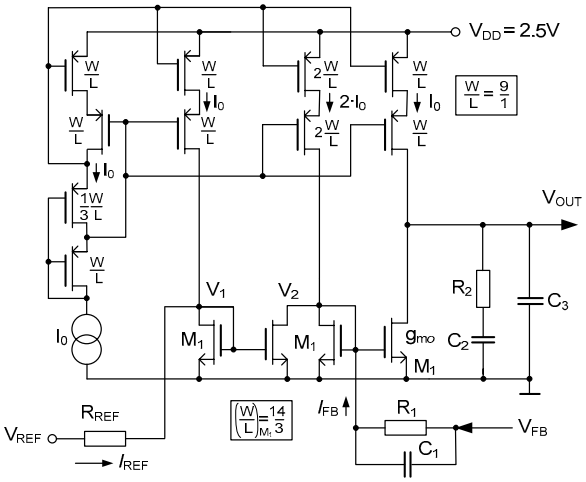

Figure 6. Schematic diagram of the controller using the high-voltage swing cascade [9] allowing to increase DC gain and voltage dynamic range.

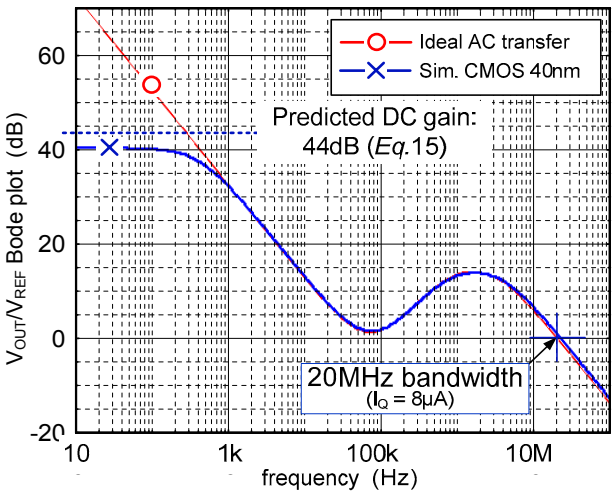

Figure 7. Ideal and simulated frequency characteristic (CMOS 40nm).

The transfer function of the controller was obtained using the procedure from [7], requiring peak of the load transient response of 55mV per ampere of load current step, and bandwidth of 20MHz. The transfer function can be expressed in the pole-zero form (4) as:

$$C(s) = \underbrace{\frac{1}{4}}_{gain\ G} \frac{2.67\cdot 10^6 \left(s/4.61\cdot 10^5 +1\right)\left(s/4.61\cdot 10^5 +1\right)}{s\left(s/2.05\cdot 10^7 +1\right)\left(s/5\cdot 10^6 +1\right)} \quad (16)$$

which, by using (7) allows to obtain a set of component values: R_1 = 197kΩ, R_2 = 128kΩ, C_1 = 11pF, C_2 = 16.9pF, C_3 = 0.39pF, g_m = 50μS. From *Fig. 5*, we select the transistor parameters I_0 = 2μA, and L = 3μm, which allows to estimate the controller gain G_{DC} = 43dB (V_{OUT} in (15) = 0.65V). The corresponding transistor width results from (6) as W = 14μm (g_m = 50μS). The value of R_{REF} is computed from (13) as 180.1kΩ, and can be adjusted by the accurate DC simulation (computed voltage V_{FB} is shifted by 9mV). The main circuit of the controller is shown in *Fig. 6*. Here, we make use of the high voltage swing Sooch cascode [9] for reducing the impact of $g_{dso,P}$ in (14) and obtaining high V_{OUT} dynamics.

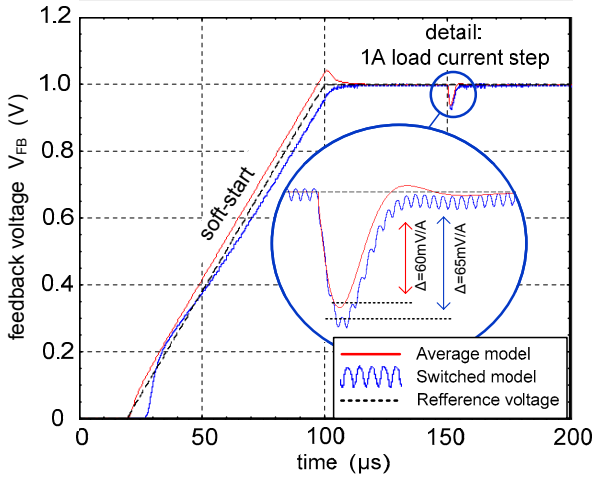

Figure 8. Transient analysis of the buck converter provided by the ideal (average), and complex (real) switched model of the converter.

The simulated AC characteristic of the controller shown in Fig. 7 corresponds with reference transfer function (16). Obtained DC gain 41dB causes the steady-state regulation error lower than 1mV per ampere of load current. As shown in *Fig. 8*, this controller allows to provide the transient response undershoot of the buck DC/DC converter, which is close to the required value 55mV/A.

As previously mentioned, the controller exhibits non-negligible DC offset due to the transistor mismatch. This effect is demonstrated by the Monte-Carlo simulation of the output voltage (V_{FB}) dispersion, shown in *Fig. 9*. The obtained dispersion is in order of ± 30mV and would require a post-fabrication trimming or the additional circuit calibration.

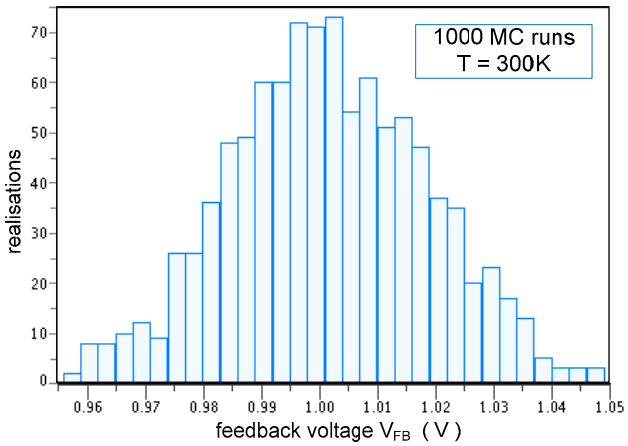

Figure 9. Monte-Carlo simulation of the output voltage V_{OUT} dispersion.

Conclusion

In this paper, PID controller circuit was presented, based on the current-difference amplifier. It was shown that the presented circuit allows to obtain interesting frequency range vs. power consumption trade-off. The detailed design equations and analysis of the circuit was presented and demonstrated on the designed circuits, where 20MHz of the frequency bandwidth was obtained with only 8μA of the static bias current.

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