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► **To cite this version:**

Frédéric Drillet, Mohamad Hamieh, Lounis Zerioul, Alexandre Brière, Eren Unlu, et al.. Flexible Radio Interface for NoC RF-Interconnect. Digital System Design (DSD), 2014 17th Euromicro Conference on, Aug 2014, Verona, Italy. pp.36-41, <10.1109/DSD.2014.59>. <hal-01084993>

HAL Id: hal-01084993

<https://hal.science/hal-01084993v1>

Submitted on 20 Nov 2014

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Flexible Radio Interface for NoC RF-Interconnect

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Abstract — This paper introduces flexible radio techniques inside integrated circuits in order to tackle the interconnect issue for many-core chips. We propose to take benefits from OFDMA for a RF-interconnect associated to a carrier allocation policy and adaptive modulation. A 20 GHz bandwidth is shared between 32 tilesets made of 32 tiles of 4 cores each, for a 4096 cores chip. We adopt a cognitive radio approach in order to dynamically share 1024 carriers, which avoids inter-cluster communication contention and decreases latency compared to conventional static approaches.

I. INTRODUCTION

Flexible radio has been a hot topic for 40 years now. As usual, it started in the military domain. B. Fette, in [1], reminds the roots of SDR (Software Defined Radio) in late 80's with the Integrated Communications, Navigation, and Identification architecture (ICNIA) of the US Air Force, followed by SPEAKeasy programs in the 90's. Civil and non military research of flexible radio started then first at MIT, for GSM base-station [2]. Now SDR, and its evolution towards radio self adaptation, namely cognitive radio [3], is invading all radio domains. Cognitive radio aims indeed at using more efficiently the radio frequency spectrum based on the analysis of its instantaneous state. It is foreseen for 5G, but also for shorter term potential uses such as TV White Spaces (TVWS) or 4G bands extension [4]. Maybe the last place where cognitive radio has not already been used so far is inside chips, but time has come since communications became crucial as the number of processing elements inside a chip greatly increases. This paper deals with many-core architectures which are planned to integrate several thousands of cores in the medium term. In this paper, we aim to demonstrate the feasibility of a generic wideband RF-transceiver and a transmission line with multiple accesses implementation. A wideband front-end is needed as we need to dynamically allocate the available communications between clusters of cores, the whole bandwidth needs to be emitted and received. The paper is organized as follows. Section II describes the architecture of the CMP with an OFDMA RF-

Interconnect. Section III gives some primary results on the implementation features corresponding to these specifications. Finally section IV draws some conclusion.

II. FLEXIBLE OFDMA SCHEME FOR RF-INTERCONNECT

A. Many-core Interconnect Challenges

The continual increase in the integration density of systems on chips was the basis for the emergence of new interconnections structures between the different blocks of the system. Indeed, the limitations caused by conventional interconnects are no longer compatible with the new requirements and constraints imposed by emerging technologies in terms of latency, flow rate and power consumption. Some technologies have already been investigated to solve intra-chip communication problem (as it can be seen in ITRS'09 report [5]) such as the 3D integration [6], optical interconnections [7][8], Radio Frequency [9][10][11] or hybrid solution [8][11]. These designs generally involve hierarchical communication schemes based on a global serpentine waveguide for inter-cluster communication and a local network on chip for the intra-cluster communication. While optical interconnects provide high bandwidth density, low latency and a distance-independent power consumption, they suffer from static power consumption [12], full CMOS compatibility and limited on-demand band allocation (only one single wavelength per emitter can be allocated at any given time). Current RF interconnects combine the advantages to provide low latency, compatibility with silicon technologies (in future CMOS and BiCMOS silicon technologies with frequencies up to 300 GHz are expected) and to be usable in near future for communication in 3D structure. On the other hand, they have some limitations as they provide a low bandwidth density and only offer a limited dynamic allocation (TDMA and FDMA [13]). Feasibility of intra-chip RF communication has already been proposed with CMOS technology [10][12], but these solutions do not directly address deadlock issues that are

likely to occur in a Network on Chip (NOC). In addition, communication latency is non-deterministic and system performance is degraded.

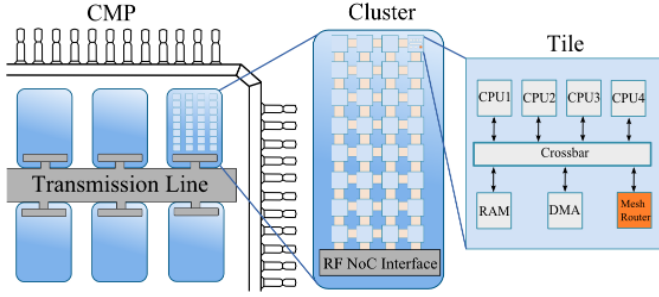


Fig. 1. Architecture of the hierarchical CMP considered with RF-Interconnect

We assume in this work a serpentine waveguide that travels among clusters, creating a fully connected crossbar, like in [8]-[13]. This design is illustrated in Fig. 1.

In this specific example, 32 clusters, each containing 32 tiles of four cores, create a 4096 cores CMP. Each cluster features an RF NoC Interface, as shown in Fig. 2, in order to communicate on the serpentine waveguide which forms the RF-interconnect (RF-NoC can also be found in the literature). The RF transceiver of each cluster is connected to a specific node in its cluster 2D-mesh network with a router.

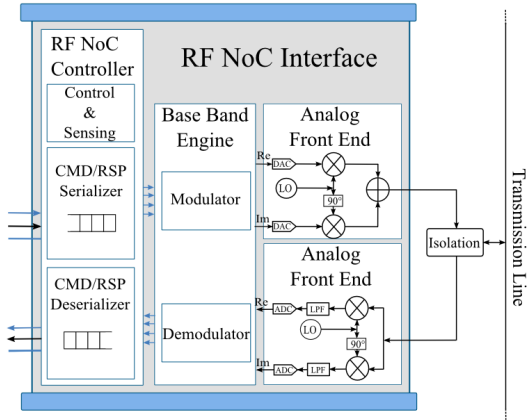


Fig. 2. RF-NoC Interface

B. OFDMA for RF Resource Allocation

As number of cores in a multi-processor rapidly increases, the designers have shifted towards hierarchical memory architectures (cores, tiles and clusters) to provide communication scalability. As shown in Fig. 1, we consider 3 levels of communication organization in our approach. Each level of the architecture has its own interconnect. In a tile, cores (CPU) communicate via a crossbar. Tiles are aggregated in clusters and communicate using a standard synchronous or asynchronous 2D-mesh NoC. Each router of the NoC has 5 ports (N, S, E, W and local) that are linked to neighbouring tiles. Finally, the communication between clusters is managed

by the RF-interconnect. The crossbar and the mesh descriptions are out of the scope of this paper that focuses only on the RF-Interconnect.

On the RF-Interconnect, simultaneous communication between clusters on orthogonal channels seems to be a promising technique for optical and RF interconnect [14][15], in order to improve their global performance, by providing services to adapt the bandwidth allocation to the data rate. However, state-of-the-art multiband interconnects require large number of redundant components to implement orthogonal channels, i.e. local oscillators and filters for RF, resonant modulators and detectors for optical interconnects. Since a node RF front-end has to include the components for each desired frequency band (for transmission and reception), an efficient multiband communication is not scalable. In order to overcome all these aforementioned challenges, we evaluate the feasibility of OFDMA (Orthogonal Frequency Domain Access) as a modulation scheme for on-chip RF-interconnects. This solution presents certain advantages such as reducing the number of RF components to re-distribute channels based on instantaneous traffic with no extra components and computation. This also provides efficient broadcast capabilities, which is of major importance in distributed-memory NoCs architectures.

OFDMA is an OFDM based multiple access (MAC) scheme, where each user gets a certain number among the 1024 subcarriers, i.e. a certain part of the bandwidth. This is performed for each user by simply padding zeros on the non-used subcarriers, before the IFFT (Inverse Fast Fourier Transformation) phase. Therefore, dynamic bandwidth arbitration between users in OFDMA is a non-complex procedure. In the context of this work, users are clusters. With recent technological developments on computational power, OFDMA is already evaluated as a possible candidate for an intra-data centre interconnect [14][15].

As it can be seen from Fig. 3, an OFDMA interconnect can be modified to create a SWMR (Single Write Multi Read) crossbar, where each node is allocated to a certain number of subcarriers (typically a resource block - RB - of 32 carriers by default) to transmit their data.

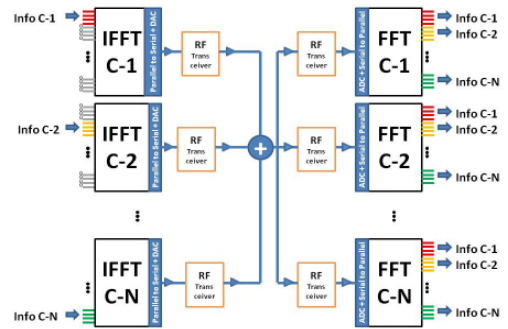


Fig. 3. OFDMA allocation scheme with intrinsic broadcast capabilities

Note that this allocation of subcarriers may be updated dynamically for each OFDM symbol thanks to cognitive radio features of this interconnect. Every user decodes all carriers but only consider data destined to them while decoding the header of each RB, thus introducing a “broadcast and select” scheme. Furthermore, they can also receive common information to all users such as broadcast or control messages. This procedure is non-complex for OFDMA, compared to existing conventional multiband architectures, as a cluster only needs to encode its information on its allocated subcarriers for that symbol. This provides fast and effective reconfiguration capabilities.

C. OFDMA transceiver

In our design, for each cluster, two cores are dedicated to the FFT and IFFT. Moreover each of them features a RF transceiver to access the transmission line. In a currently realistic implementation perspective, we propose to use a 20 GHz bandwidth RF front-end, made of a direct I/Q conversion with a fixed 30 GHz local oscillator for each cluster which gives a band between 20 GHz and 40 GHz. Contrary to a FDMA (Frequency Division Multiple Access) scheme [11], the proposed solution allows a reconfigurable allocation (rate, transmission band) without any changes in the RF part of the transceiver, thus analog reconfiguration is avoided and replaced by a digital processing, thanks to FFT/IFFT’s reconfiguration flexibility.

FFT/IFFT blocks feasibility has been demonstrated up to 50 Gbit/s computation. Assuming a power dissipation of 3.3mW/MHz by the FFT/IFFT implementation [16] and sharing the whole band between the 32 clusters for bidirectional communication, the symbol rate is 19.53 MHz. Therefore, an overall power dissipation of 4.12W is expected. ADC/DAC blocks which are able to operate at 20 Gsample/s and 22 Gsample/s respectively. In addition, authors of [15] are currently developing a 10 Gbit/s Ultra Wideband (UWB) optical OFDM system. Considering these innovative technologies, in this work we assume a 1024 subcarriers system spanning a 20 GHz bandwidth. One of the tiles (e.g. 4 processors) of each cluster is allocated to the task of radio resource management, so that any arbitrary subcarrier arbitration or modulation policy could be embedded according to future requirements. Cognitive radio approaches may be softly applied for instance, for sensing, learning and decision making purposes [16]. Application specific massive CMPs and SoCs are on the horizon, which show distant traffic characteristics and require different QoS requirements; hence this approach makes sure to be able to employ the optimal policy. It is out of the scope of this paper to deal with the resource management. However we can consider that subcarriers may be dynamically re-allocated depending on each cluster requirements in terms of transmission throughput or delay. Previous studies have shown that a 3.5x lower average latency can be achieved with this approach in comparison to static allocation scheme [18].

III. RF NOC INTERCONNECT INTERFACE

A. Analog Transmitter Front End

In order to avoid analog reconfiguration and to take benefit from advantages of OFDMA, a generic wideband front end is needed. Knowing that, in 250 nm SiGe BiCMOS technology, the maximum reachable frequency allowing gain is about 40 GHz, we design therefore a 20 GHz bandwidth analog transceiver. E. Socher, et al [10] presented a T_x/R_x in a RF NoC, design in a 0.18 μ m silicon technology. Unlike our work, they used FDMA and needed several local oscillator frequencies for their mixers. In SiGe technology, E. Laskin, et al [19], proposed a wideband transceiver in the 80 and 160 GHz band and a 140 GHz amplifier, which demonstrates the feasibility of SiGe BiCMOS technology for systems in the 100-160 GHz range. As power consumption is an important constraint in the RF NoCs, passive components are privileged when possible, for instance for the mixers. F. Ellinger, et al [20] proposed a drain-pumped passive mixer in the 30-40 GHz range. None of these works perfectly fit our needs. We have adapted the features of these systems on our case.

We focus in this paper on the mixers, adders, subtractor and filter. The DACs, ADCs, splitters, PLL and phase shifters are considered ideal, their performance and surface are taken in the literature. At the transmission side, I/Q digital signals are converted to analog in the DAC. Then they enter the mixers, which are the first stage of the transmitter as shown in Fig. 4. The up-conversion mixers combine the baseband signal with the local oscillator (LO) signal. Mixing occurs in a MOSFET whose gate and drain are fed by the local oscillator and the baseband signal respectively. A higher frequency output is recovered in the MOSFET source. A drawback of such a device is the weak LO/RF isolation [19]. It leads to a high power LO carrier in the output spectrum. As the local oscillator frequency is 30 GHz, which is the middle of our 20 GHz bandwidth, it needs to be removed. Thanks to the differential outputs of the DAC, two IQ-Modulators can work together to do so. Besides avoiding interference caused by image frequencies, they can reduce the LO level in the output. As we use the same local oscillator for both of IQ-modulators and opposite I-Q signals, the IQ-Modulators outputs are subtracted in a differential amplifier [22][23] in order to perform this suppression. In addition to the 20 GHz bandwidth, our transceiver has two important specifications: surface and power consumption.

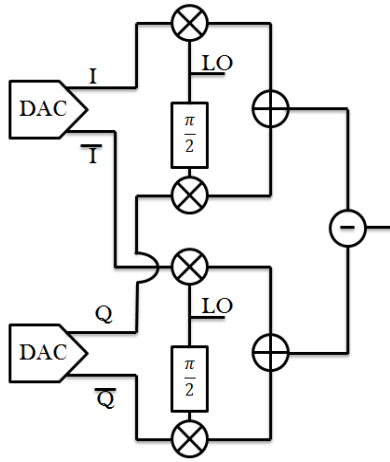


Fig. 4. Transmitter architecture

As it is integrated on a network on chip, the transceiver power and area consumption must be sufficiently small compared to the whole system one. The mixers are designed with non-polarized MOSFETs [20][21]. Thus, there is no power consumption in the mixers. We can have an estimation of the occupied surface by the transmitters including DACs and phase shifters if they were implemented on such a device. Tables I and II summarize the simulated transmitter performance. Table II considers the complete chip design with 32 transmitters, one per cluster. In Table II the power consumption and area values for are obtained considering the sum of all individual powers given, there are four mixers, two adders, one differential amplifier, two DACs, two phase shifters, and one PLL in a transmitter.

Table I - Performance of simulated transmitter block and those found in the literature

	Gain/Loss (dB)		Power Consumption (mW)	Area (mm ²)
	Max	Min		
Mixer	-7.6	-10	Passive	0.17
State of the art Mixer [20]			Passive	0.235
Adder	-1.1	-1.4	3.2	0.089
Diff. Amplifier	15.8	6	6.4	0.1
State of the art Diff. Amp. [23]			90	0.37
DAC [25]	/	/	3.8	0.0086
Phase shifter [27]	/	/	Passive	0.08
PLL [27]	/	/	57	0.87

Table II - Performance of 1 and 32 transmitters

	Power Consumption (mW)	Area (mm ²)
1 Transmitter	77.4	1.9
32 Transmitters	2477	61

B. Analog receiver Front End

In the receiver of Fig. 5 an IQ-demodulator is used to retrieve the I/Q outputs. The splitter [29] separates the RF-input into 2 paths which are mixed with a LO signal in a down-conversion mixer. As we use the same topology for the up and down-mixers, a LO signal is retrieved in the output of the mixer. Unlike the up-conversion, the LO signal can be filtered by a low-pass filter. The bandwidth is indeed 0-10 GHz in the receiver output.

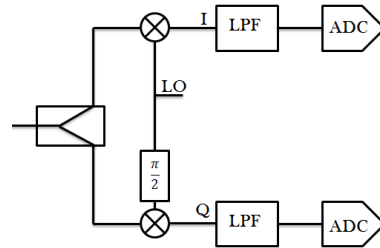


Fig. 5. Receiver architecture

Then ADC converts the analog data into digital domain. Tables III and IV summarize the simulated receiver performance for one receiver and 32 receivers for RF-interconnect inside the chip.

Table III - Performance of each simulated receiver block

	Gain/Loss (dB)		Power Consumption (mW)	Area (mm ²)
	Max	Min		
Mixer	-7.6	-10	Passive	0.17
ADC [25]	/	/	3.8	0.013
Phase shifter [27]	/	/	Passive	0.08
PLL [27]	/	/	57	0.87
Splitter [27]	-3.8	-3.8	Passive	0.93

Table IV - Performance of the simulated LPF

	Passband attenuation (dB)	Power Consumption (mW)	Attenuation (dB)	Area (mm ²)
LPF	-1	Passive	-60	0.044

Table V - Performance of 1 and 32 receivers

	Power Consumption (mW)	Area (mm ²)
1 Receiver	64.6	2.33
32 Receivers	2067	74.7

The whole 32 transceiver power consumption is around 8.66W, which is 24% of the one of a 256 cores NoC (36W). R.Das et al [28] proposed a 256 cores NoC power consumption about 20W. In that case, our system is about 43.3% of the whole power consumption. If we extrapolate to a 4096 cores system, the whole transceivers power consumption would remain the same but an exponential increase of the power consumption of the mesh NoC is expected.

As we use a transmission line for the RF communications, another remaining issue is to consider the access to the transmission line.

C. Transmission Line Access

The state of the art presents two kinds of RF interconnects corresponding to transport information either by radio [29], or by a waveguide used as a transmission medium. But, the interest of using radio signals is decreased by the problems of electromagnetic compatibility (EMC). Therefore we focus our work to the case of the transmission provided through a waveguide.

The access methods to the transmission line can be classified into two categories. The first one considers the "direct coupling", for which the modelling of multi-connection ports shows a degradation of the transmission line properties, while increasing the number of T_x/R_x . The second category considers an "indirect coupling" such as capacitive coupling [9], inductive coupling [13], etc. As in the inductive access method, the presence of inductors take a large area, it is not presented in our study.

In order to minimize the length of the radio-frequency transmission line, we consider that each transceiver T_x (transmitter) and R_x (receiver) elements are placed on one side of the line. The distance between two T_x/R_x is 8 mm. So, for 32 T_x/R_x , the total length of the line is 120 mm.

The presence of multiple T_x/R_x , as shown in Fig. 6, affects the characteristics of the transmission line, where multiple reflections appears along the line at the interconnect points. To overcome these problems, we used the capacitive coupling to access the line [29][30]. This method consists in transmitting a signal between two conductors, without any physical link. Right hand side Fig. 6 shows a typical scheme for this access method: the gap between the T_x/R_x and the line represents the coupling capacitance. Using this access, the use of several T_x/R_x does not influence the characteristics of the transmission line and therefore generates less reflection.

In order to minimize the metal loss, we use a transmission line (coplanar line) whose impedance characteristics are equal to 30 Ω : the linear attenuation ranges from 0.4 to 0.6 dB/mm in the 20-40 GHz frequency band. In order to illustrate the transmission performance of the capacitive access method, we compare it to the direct access one where the T_x/R_x are directly connected to the RF transmission line as shown in left

hand side of Fig. 6. Fig. 7 shows the variation of the transmission coefficients (S_{ji}) in the frequency band 20-40 GHz for the furthest T_x and R_x (T_{x1} and R_{x32}).

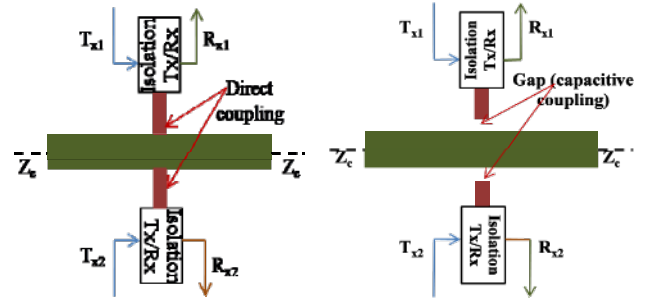


Fig. 6. Typical scheme of direct and capacitive access methods

As shown in Fig. 7, the capacitive access method has a lowest attenuation compared to direct access and it is less fluctuant in the 20-40 GHz frequency band; it can be explained by less reflexions of the signal along the RF transmission line.

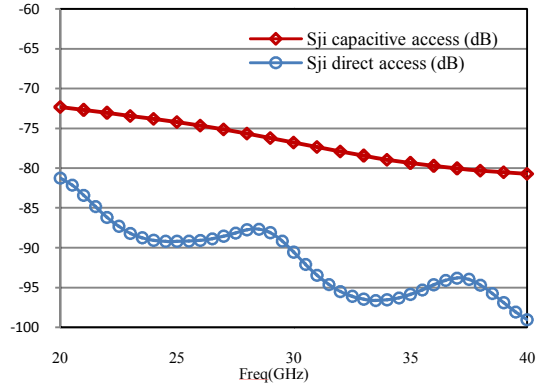


Fig. 7. Transmission coefficients S_{ji} between the T_{x1} and R_{x32}

IV. CONCLUSION

In this paper, we tackle the communication scalability problem of future massive CMPs. We present an innovative and flexible OFDMA RF-interconnect. Our architecture provides a broadcast capable and highly adaptable infrastructure, while avoiding the state-of-the-art models necessity of employing numerous amounts of CMOS elements and analog reconfiguration. Also, the system allows the designers to use any kind of radio resource allocation policy based on the specifications and QoS requirements. This will be the scope of future papers. We target for our current prototype a frequency domain between 20 and 40 GHz, limited by the technology. If such a system were implemented on a NoC indeed, it should be in a higher frequency range that will be available in the future, namely, at least a few hundred of GHz. Taking into account these technological advancements, we can hope to divide the passive components surface by 6. We are also currently working on a new wired transmission line access which causes less power loss and we

plan to evaluate in a future work the performances of a wireless transmission type.

ACKNOWLEDGEMENTS

This work is supported by the 2012 INS program of the French National Research Agency: ANR-GUI-AAP-05.

We would like to thank NXP Semiconductors for providing us their technology.

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