Safe design method of embedded control systems. Case study

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Résumé— **This paper proposes an approach for safe design of hardware embedded control systems. The approach is based on a combination of formal verification and discrete controller synthesis techniques. Formal verification is solicited to detect design errors and provide counterexamples, while the Discrete Controller Synthesis technique is used to correct those error since it attempts to enforce previously verified specifications which do not hold. It automatically produces control code, which is assembled to the erroneous component in order to provide a system correct by construction with respect to the specification to enforce. We illustrate the approach on a train controller subsystem taken from "Bomabardier Transport" company.**

Mots-clés— **COTS, Vrification formelle, synthse du contrleur discret, systme evenements discrets, proprit de sret, proprit de vivacit, composant correct par conception.**

I. Introduction

Design errors have serious consequences when they appear in critical control systems, such as robotized plants, energy production plants, or transport systems. Such errors may cost human lives, or at best, a large amount of money to redesign the system. Such systems are often modeled as synchronous reactive systems, by using communicating finite state machines. They call for safe design methods and techniques, ensuring functional correctness against a set of specifications. Besides simulation, the model checking (formal verification) technique [7], [8] is unavoidable for discovering subtle bugs, usually known as corner-case configurations, which are very difficult to uncover by simulation. The model checking technique was used in the industrial domain to detect design errors of avionic systems [5] and [14]. However, the designer must correct these errors manually, which is an error-prone process in general. It is usual that by attempting to manually correct an error, another error is introduced, which creates a vicious circle situation.

However, this design process allows the progressive creation of reusable building blocks considered as certified: enough time has been spent in design/verification, without finding any more significant errors. Such re-usable blocks can be managed internally, or acquired from vendors; they are known generically as Commercial off-the-shelf (COTS) components. A COTS encompasses both a behavior, and a set of specifications. COTS can be assembled according to their specifications, in order to create new behaviors, satisfying more complex specifications, and gain a lot of time through code reuse. However, even though each of them has been individually and thoroughly verified, they are rarely designed to perfectly operate together. Design errors can appear by simply assembling a collection of correct COTS and their manual correction is likely to be error-prone and time-consuming. Thus, COTS integration can remain an expensive task.

The Discrete Controller Synthesis (DCS) technique is an emerging solution able to build correct-by-construction designs, by automatically generating a controller. It was first proposed by Ramadge and Wonham [17] in 1989, to generate controllers for manufacturing plants. DCS seems a promising approach for automatically producing correct designs, or correcting design errors. In this paper, we propose a component-based design approach for safe design of COTS-based hardware systems. This approach uses model checking in synergy with discrete controller synthesis. We demonstrate the validity of this approach on an railway control system. The discrete controller synthesis has been suggested to synthesize some temporal properties over toy robot [1], and to solve mismatches between interacting protocols [18]. An optimization over the DCS method has been proposed in [11].

The rest of the paper is organized as follows: In section 2 we define the notion of COTS. Section 3 briefly recalls the model checking basic concepts. Section 4 explains the discrete controller synthesis technique. Section 5 introduces our safe design method for component-based hardware systems. Section 6 illustrates the method on a train control system, it presents an application of the proposed method and the results obtained. Section 7 concludes the article.

II. Definition

A control COTS can be found in a generic COTS library. It is characterized by four elements: (1) COTS interface (I). (2) environment assumptions, or sometimes named preconditions (A). (3) behavioral guarantees, or sometimes named post-conditions (G). (4) COTS functional behavior (M). Given C, a control component in a hardware embedded system, with (n) input and (m) output, we define its elements as follows: a COTS interface (I) is the list of inputs and outputs though which the component is connected to the physical environment.

Many hardware COTS have a discrete event behavior which can be described as a discrete event system DES, it can be modeled as a set of synchronous Finite State Machines *(FSM)* with outputs. A *FSM* is defined as a tuple $M = \{q_0, X, Q, \delta, PROP, \lambda\}$ where:

- q_0 is the initial state;
- Q is a finite set of Binary state variables;
- X is the set of Binary input variables;
- $X = X_c \cup X_{uc}$, the sets on controllable uncontrollable inputs respectively;

- $PROP$ is set of Binary output propositions;
- δ is the translation relation

$\delta : B^{|s|} \times B^{|x_c|} \times B^{|x_{uc}|} \times B^{|s|} \rightarrow B^{|PROP|}$

- λ is the output function:

$\lambda : B^{|s|} \times B^{|x_c|} \times B^{|x_{uc}|} \rightarrow B^{|PROP|}$

$\lambda : B^{|s|} \rightarrow B^{|PROP|}$

III. The model checking technique

This technique checks the behavior of a design against a formal specification written in temporal logic [13]. The design is modeled by a set of communicating finite state machines. The verification algorithm performs a symbolic exhaustive search inside the state space of the studied model, and returns the set of states satisfying the specification.

Model checking is more powerful than simulation since it verifies the system against all its possible input values instead of only selected scenario. In addition, it is able to provide a diagnostic counterexample in case a specification is violated. This counterexample contains all the system inputs that are involved in the property violation and chains of their values, starting from the system initial state till the error state. However, its performance decreases dramatically with the size of the design under verification because of its exponential complexity in the number of design variables. Model checking is suitable for verifying small/medium-sized designs, in order to find corner-case errors [reference]. Although it can find all the design errors, but it leaves a harder mission which is correcting these errors to the designer.

IV. Discrete controller synthesis

Given *(M)* a *FSM* modeling a system, *(P)* a formal specification expressing safety (possibly in temporal logic), the *DCS* technique attempts to build a supervisor SUP, which, once composed with M, guarantees the invariance of P. The satisfaction of P is considered within a game, where the supervisor, if it exists, plays against the environment; at each moment is able to implement a non-losing strategy, preventing M to reach a state where P does not hold. The input set of M is divided into two disjoint subsets: controllable (X_c) and uncontrollable (X_{uc}) inputs. Controllable inputs are driven by the supervisor, whereas the uncontrollable inputs are driven by the environment. The *DCS* technique operates in two steps. First, an Invariant Under Control set IUC is built; as long as M stays inside IUC, the game cannot be lost: states not satisfying P cannot be reached. This is performed by selecting controllable values which always lead to IUC, whatever the uncontrollable values provided by the environment. The second step constructs the supervisor SUP, as the set of all transitions leading to IUC. We integrate this technique in the design method to correct automatically the design errors detected in the model checking techniques.

$IUC_0 = \{q \mid \text{P holds in } q\}$.

$IUC_{i+1} = \{q \in IUC_i \mid \forall x_{uc} \exists x_c : \delta(q, x_c, x_{uc}) \rightarrow q' : q' \in IUC_i\}$. A supervisor does not exist if IUC is empty or does not contain q_0. The supervisor is the set of transitions denoted as follows:

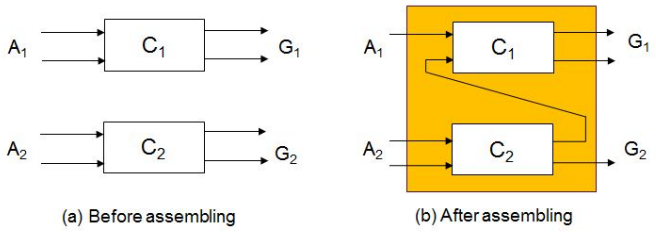
$SUP = \{(q, x_c, x_{uc}, q') \mid \forall x_{uc} \exists x_c : q' \in IUC\}$

The solution SUP obtained above is a relation, represented as a characteristic equation. A final step implements the supervisor SUP by transforming it into a set of control functions, one for each x_c, according to the technique described in [10]. The DCS technique has been suggested to synthesis some temporal properties over toy robot [1], and to solve mismatches between interacting protocols [18].

V. Component-based design flow

As mentioned above, each COTS has its local environment assumptions (A) and local guarantees (G). The fact of connecting COTS to each other can entail incorrect global behavior of the assembly, because some local assumptions of a COTS conflict some guarantees of another COTS and vice versa. For example, if *G2* conflicts *A1* in figure 1 a global design errors appear when assembling the COTS despite the correct local behavior of each individual COTS.

Fig. 1. COTS assembly



Designing a safe system based on COTS means assembling the components and ensuring that the assembly operates correctly, i.e, the assembly satisfies certain defined global properties and preserves the local guarantees of each individual component. Figure 2 presents our design flow. The design method is semi-automatic method which had two main goals. The first one is to provide formal COTS library which contains not only the executable model of the component with a textual documentation, but also a formal representation of the component's functional requirements. The second goal is to construct hardware control systems based on prebuilt COTS components. The first step in the design method is selecting the needed component(s) and formalizing the environment assumptions, the behavioral guarantees and additional new properties. Two or more COTS can be composed together, according to some new specifications to satisfy. This task amounts to a synchronous composition between FSMs in the cases where the final system will be implemented on chips like FPGA or ASIC. In the second step the composite design is formally verified against a specification *spec* in order to detect the design errors. If the verification passes, the newly obtained design can be inserted in the COTS library as a new reusable component with its formal documentation for the environment assumptions, behavioral guarantees and additional properties. Otherwise, the model checking tool produces a counterexample which means a property under verification is violated. If the detected error is related to a liveness property the designer must correct this error manually. Whereas, if the error is related to a safety property, the designer passes to an automatic correction step based on the DCS method. As said before the DCS tool needs two sets of inputs (controllable, uncontrollable inputs). As this tool is still a research demonstration tool, the set of controllable inputs is chosen by the researchers

through random testing of different inputs and choose the set that fits better the synthesis process, i.e, the set with which the DCS tool can provide a correcting solution (no specific strategy is used for choosing the controllable inputs). In hardware control systems, the designer cannot impose the controllabily of the system inputs, since he is working with a real system and some inputs can be impossibly controlled like sensors. In our method we suggest to use the counterexample provided by the model checking tool to find the set of controllable inputs. As the counter example, provides a set of only and all the signals responsible of the property violation, it can direct the designer to choose the signals candidate to be controllable. The model checking tool "Cadence SMV" [16] that we use for this study categorizes the counterexample signals' variables in (Input variables, state variables). To construct the set of controllable signals X_c, the designer should select the set of input and internal variables in the counterexample list and remove some of those signals which are impossible to be controlled. The designer should respect some rules when removing the signal variables :

- X_c initial = the complete set of signals provided by the counterexample.
- remove from X_c every variable of a sensor signal;
- remove from X_c every variable of data signal;
- remove from X_c every variable of an alert or alarm signal;
- remove from X_c every state variable;

Those rules can be applied for the hardware systems which contain the above types of signals. The DCS step attempts to build a supervisor which enforces *spec* by controlling the variables previously chosen. If a supervisor exists, it is implemented as a set of control functions f and assembled to the original executable model of the components. Otherwise, the designer concludes that *spec* cannot be satisfied by this system. Sometimes, the DCS produces very restrictive supervisors which ensures *spec* by disabling most interesting behaviors. We propose to verify some key Liveness properties after the synthesis step to ensure that the system still achieves certain behavior. We also verify the controller passiveness, i.e, the controller do not invent events to the system, it only delays or prevents some events. Finally, we call a simulation step order to dynamically validate the newly obtained control solution. In the following, this design method is illustrated on an example of building a train controller subsystem over COTS.

VI. Case study : Passengers' access system

The design method proposed above is illustrated on the subsystem (Door / filling-gap). The objective of this case study is to show how the controller synthesis automatically generates a control component correct by construction, in order to save time and correction guaranties compared to manual coding. Our case study is obtained from the project FerroCOTS [6]. The system consists of three components (the open authorization component, the door controller ($Manage\_open\_close$) and the filling-gap controller (Manage_FG)) which are separately prebuilt.

COTS Manage_open_close illustrated in figure 3 handles the control of the door, in accordance with a request for the opening/closing ($Demand\_open, Demand\_close$) respectively and the state of physical sensors (Sns_φ_d).

Fig. 2. Design Method of Control Embedded Systems

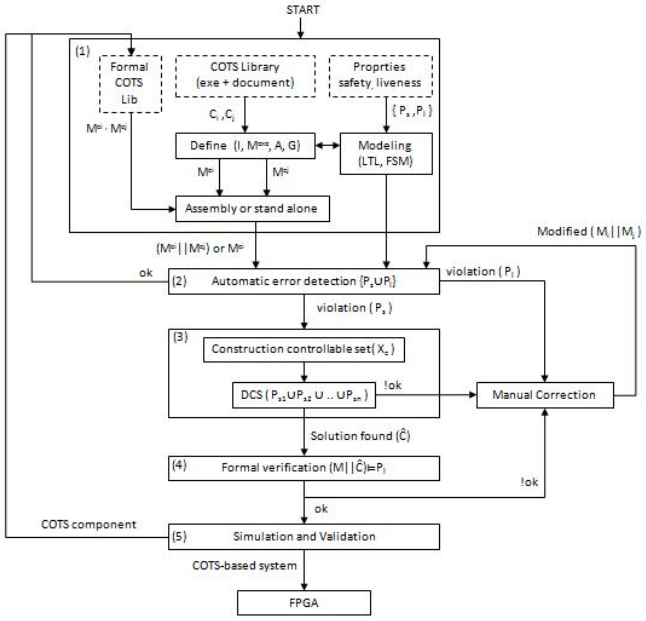
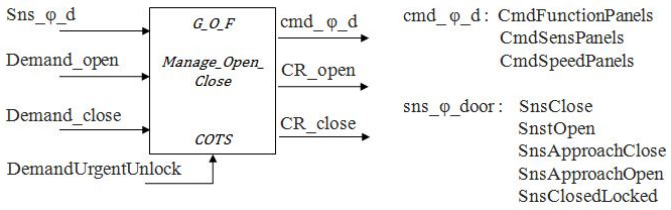
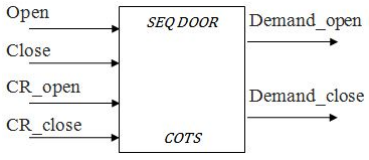


Fig. 3. Manage_open_close COTS



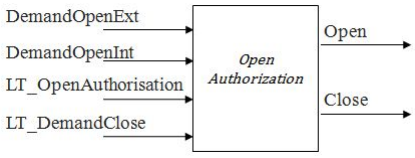
Some specific functional constraints related to the train context are not part of the COTS Manage_open_close. For example, at the time of closing, wait (1s) between the close request and the order of the panels' command. This period corresponds to a sound (ringing) signal. It is an operational constraint which is integrated in the assembly of COTS in form of a new component modeling this behavior named SEQ_PORTE shown in figure 4.

Fig. 4. Operational constraint SEQ_DOOR



The Open-authorization component shown in figure 5 provides the COTS Manage_open_close with the open and close requests.

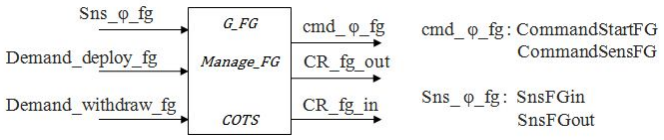
Fig. 5. Open authorization component



The filling-gap control component Manage_FG is shown in figure VI, it controls the deploying (opening) and with-

drawing (closing) of the physical filling gap. It receives a deploy or a withdraw request from the train driver $(Deploy, Withdraw)$ respectively, it reads the values of sensors CR_fg_out, CR_fg_in which indicate the full opening and the full closing states of the physical filling-gap.

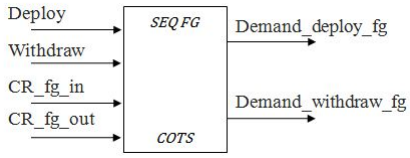
Fig. 6. Manage_FG COTS



We suppose that the internal functionality of each component is correct and no local errors occur. The global behavior of the component's assembly has to obey a global safety temporal property which is: the door must not start opening before the full opening of the filling-gap.

The component SEQ_FG component shown in figure 7 allows to model an operational constraint of Manage_FG component.

Fig. 7. Operational constraint SEQ_FG



A. Behavioral description of COTS

While the train is in mode "stop in the station", the train driver send requests to the door and the filling-gap to open/close. Manage_open_close component controls the panels and speed, according to the information sent by the physical sensors. It sends commands to the physical environment $(CmdFunctionPanels, CmdSensPanels, CmdSpeedPanels)$ regarding the driver requests. $CmdFonctionPanels$ commands the panels of the door to function, $CmdSensPanels$ commands the direction of the door panels (opening direction / closing direction), $CmdSpeedPanels$ commands the speed of the panels movement (quick / slow movement).

Manage_FG component controls the movement of the filling-gap and its direction, basing on information received from physical sensors. It returns signals at the end of the operation CR_fg_in, CR_fg_out. Authorization opening component produces a control opening and closing of applications sent by the driver. The exact behavior of the COTS is purely combinatorial.

- Open = (DemandOpenExt or demandOpenInt) and LT_OpenAuthorisation and not LT_DemandClose;
- Close = LT_DemandClose.

In order to preserve safe behavior of the system, the door must not start opening before a full opening of the filling-gap. To ensure such a safe behavior a global safety property must be synthesized over the assembly of the components.

B. Safe design of the system

We build the system following the steps of the method. First, we formalize the door, the filling-gap and the open authorization components as follows: $M^d = \{I^d, M^{exe}, A^d, G^d\}$ where:

- $I^d = \{SnsClose, SnsOpen, SnsApproachClose, SnsApproachOpen, SnsClosedLocked, Demand\_open, Demand\_close, CmdFunctionPanels, CmdSensPanels, CmdSpeedPanels\}$;
- $A^d = \{F(CmdFunctionPanels \wedge CmdSensPanels \wedge CmdSpeedPanels), F(CmdFunctionPanels \wedge CmdSensPanels \wedge \neg CmdSpeedPanels)\}$;
- $G^d = \{F(Demand\_open \rightarrow (CmdFunctionPanels \wedge CmdSensPanels \wedge CmdSpeedPanels)), G(Demand\_close \rightarrow (CmdFunctionPanels \wedge CmdSensPanels \wedge \neg CmdSpeedPanels))\}$.

The filling-gap is modeled as follows: $M^{fg} = \{I^{fg}, M^{exe}, A^{fg}, D^{fg}\}$ where:

- $I^{fg} = \{(SnsFGin, SnsFGout, Demand\_deploy\_fg, Demand\_withdraw\_fg, CommandStartFG, CommandSensFG, CR\_fg\_out, CR\_fg\_in\}$;
- $A^{fg} = \{F(Demand\_deploy\_fg), F(Demand\_withdraw\_fg)\}$;
- $G^{fg} = \{G(Demand\_deploy\_fg \rightarrow CommandStartFG \wedge CommandSensFG), F(Demand\_withdraw\_fg \rightarrow CommandStartFG \wedge \neg CommandSensFG)\}$.

The open authorization component is modeled as follows: $M^{O\_AUT} = \{I^{O\_AUT}, M^{exe}, A^{O\_AUT}, D^{O\_AUT}\}$ where:

- $I^{O\_AUT} = \{DemendOpenExt, DemandOpenInt, LT\_OpenAuthorization, LT\_DemandClose, Open, Close\}$;
- $A^{O\_AUT} = \{F(DemendOpenExt \vee DemandOpenInt), F(LT\_close)\}$;
- $G^{O\_AUT} = \{G(DemendOpenExt \vee DemandOpenInt \rightarrow F(Open)), G(LT\_close \rightarrow Close)\}$.

The models of all the components are generated and assembled in VHDL form in order to synthesize the safety global property.

The assembly of the original components is shown in figure 8.

The assembly model is $M^{sys} = \{I^{sys}, M^{exe}, A^{sys}, G^{sys}\}$ where:

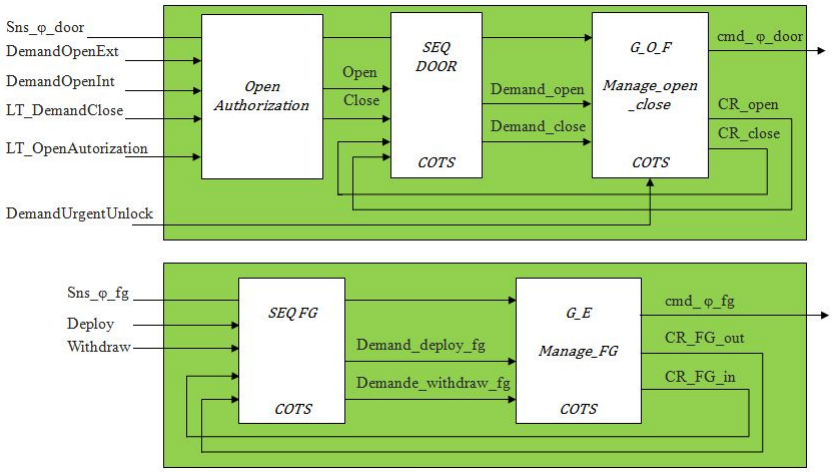
- $I^{sys} = \{I^d \cup I^{fg} \cup I^{O\_AUT}\}$;
- $A^d = \{A^d \cup A^{fg} \cup A^{O\_AUT}\}$;
- $G^d = \{G^d \cup G^{fg} \cup G^{O\_AUT}\}$.

The global safety property is modeled in LTL logic as :

$p = G\neg(CR\_open \wedge CR\_fg\_in)$ In the second step of the method, p is firstly verified over the assembly model M^{sys} using a model checking tool Cadance SMV, a counterexample is obtained. It contained the set of the system inputs and outputs which caused the property violation. This set represents the initial list of controllable variables $X_c^{init} = \{SnsClose, SnsOpen, SnsApproachClose, SnsApproachOpen, SnsClosedLocked, Demand\_open, Demand\_close, CmdFonctionPanels, CmdSensPanels, CmdSpeedPanels, SnsFGin, SnsFGout, Demand\_deploy\_fg, Demand\_withdraw\_fg, CommandStartFG, CommandSensFG, CR\_fg\_out, CR\_fg\_in, DemendOpenExt, DemandOpenInt, LT\_OpenAuthorization, LT\_DemandClose, Open, Close\}$.

We notice that the set contains all the assembly inputs and outputs, this result is expected since the example is relatively small, so all its signals are involved

Fig. 8. Original COTS assembly



in the property violation. To build the final set of controllable variables, we remove all the variables of the sensors since they represent information which cannot be neither delayed, nor ignored. We remove the variables of the commands since they are outputs of the control components. The final set of controllable variables is $X_c = \{DemandOpenExt, DemandeOpenInt, LT\_DemandClose, Deploy, Withdraw\}$ All remaining variables are considered uncontrollable variables

In the third step in the design method, a controller is automatically generated using the DCS to synthesis the safety property *(p)* over the assembly model. We use for this study the tool *Sigali* [4]

The controller generates the values of $(DemandOpenExt, DemandeOpenInt, LT\_DemandClose, Deploy, Withdraw)$. If the value received from the environment is the expected value, the controller let it pass to the component, otherwise, it change it, in order to keep the behavior of the system safe. An extract of the real controller of the door-filling-gap system can be seen as follows: if $(SnsOpen \vee SnsFGout)$ then $(Withdraw = 0)$ else $(Withdraw = 1)$; if $(SnsClose \vee SnsFGin)$ then $(DemandOpenExt, DemandeOpenInt = 0)$ else $(DemandOpenExt, DemandeOpenInt = 1)$;

We assemble the resulting controller to the system model in order to construct the controlled system as shown in figure 9. The dashed arrows represent the uncontrollable signals. The signals $(O\_DemandOpenExt, O\_DemandOpenInt, O\_LTDemandClose, O\_Deploy, O\_Withdraw)$ are the signals received by the controller from the environment, their values are modifiable by the controller i order to provide the corresponding signals $(DemandOpenExt, DemandOpenInt, LTDemandClose, Deploy, Withdraw)$ correct values which prevent the system of going to error states. The assembly obtained by the controller synthesis allows several possible implementations of the composite function door / Filling-gap. The presence of the controller allows the arrival of the opening and deployment requests in any order, with the guarantee of a correct sequence.

In the fourth step we verify the liveness of the controlled system and the passiveness of the controller. To do so we verify the assembly guarantees G^{asm}, and some passiveness properties :

- $passive_1 : G\neg(DemandOpenExt \wedge \neg O\_DemandOpenExt)$;
- $passive_2 : G\neg(DemandOpenInt \wedge \neg O\_DemandOpenInt)$;
- $passive_3 : G\neg(LT\_DemandClose \wedge \neg O\_LT\_DemandClose)$;
- $passive_4 : G\neg(Deploy \wedge \neg O\_Deploy)$;
- $passive_5 : G\neg(Withdraw \wedge \neg O\_Withdraw)$;

After calculating the controllers, a simulation step (the fifth step) allows the designer to visualize the behavior of the controlled assembly for certain scenarios in order to provide a final validation of the system before implementing it on the chip.

VII. Conclusion

In this article, we present a compositional, semi-formal safe design framework over prebuilt, reusable COTS components, it is an enhancement over a former work [12], here, we detail the formalization step and we manage to provide the simulation results. The method uses model checking in synergy with Discrete Controller Synthesis for automatically finding and automatically correcting design errors respectively. The method proposed is illustrated on a railway control system and the results obtained demonstrate the validity of the proposed method in producing correct by construction designs. Although the model checking and the discrete controller synthesis methods already exist in the literature, our method is considered the first cooperation between these two techniques, which takes advantages of each one and solves the problem of manual correction after the model checking and the problem of finding the controllable variables which is a basic input for the DCS technique. It is also the first application of the DCS technique on a real industrial system. Current investigations include possible performance to fully automatize the choice of controllable inputs of the *DCS* in order to reach a full-automatic safe design method starts by a system model and finishes by the implementation code.

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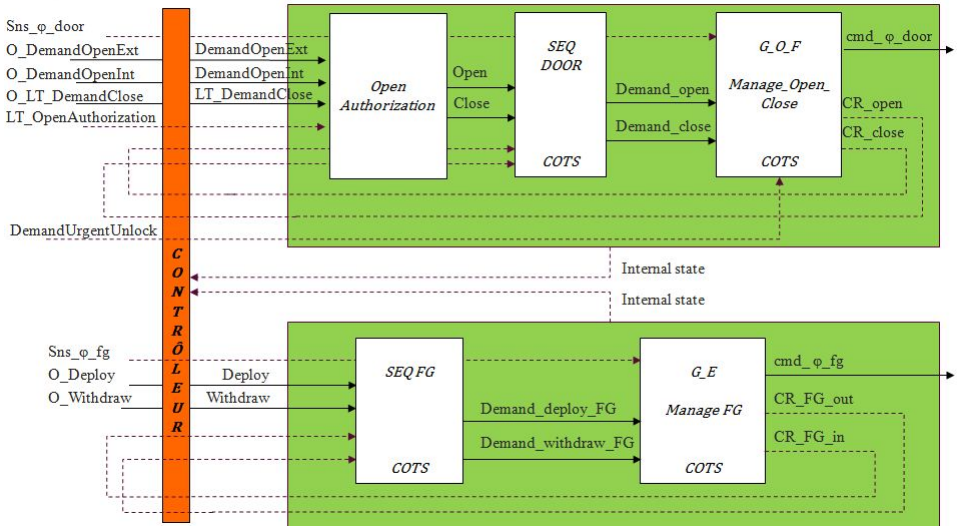
Fig. 9. The controlled system



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