A novel CAD framework for substrate modeling

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(Invited Paper)

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***Abstract*—This paper presents a novel Computer-Aided-Design (CAD) framework for 3D extraction of the substrate electrical network. The proposed CAD tool (framework) models efficiently the minority carrier propagation inside substrate network especially for smart power ICs. Today, the minority carrier propagation into the substrate is ignored in existing SPICE simulators. It can be simulated using finite element methods in TCAD. Generally, TCAD simulations are accurates but take long time. Thus, they become of limited help for large scale ICs involving hundreds of transistors. In the context of the FP7 AUTOMICS project, the extraction tool will take into consideration the minority carriers effects. It will allow the designer to predict the minority carrier propagation through the substrate. This can be useful in evaluation the efficiency of ESD protection and latchup faults due to this leackage current in the substrate specially in HV/HT applications. With the proposed substrate network, the three-dimensional layout parasitics are constructed and substrate noise is simulated before first silicon fabrication. A simple diode example is illustrated to demonstrate the principal idea of the extraction tool.**

I. Introduction

Smart Power ICs merge high-voltage and low-voltage devices on the same silicon chip [1]. This makes them highly demanded in automotive embedded systems, at a competitive cost. Merging standard low voltage architectures with high power devices on a single chip is a difficult task since these devices operate at different voltage levels. Switching of the power stage for many automotive high voltage applications (e.g. driving motor) cause the minority carrier injection to propagate into the substrate. The disturbances caused by minority carrier propagation may dramatically affect the functionality of low voltage devices existing on the same chip, even at long distances. [2].

To evaluate the noise coupling into the substrate, numerous investigations for substrate model extraction have been studied recently [3] [4] [7]. The boundary-element method and the interpolation method [5] [6] face the choice between a relatively large amount of memory use and less accurate extraction and computation, even when neglecting the minority carriers diffusion. A physically based TCAD simulators are available. They are accurate and considered as powerful tools to model the minority carriers diffusion [8]. For large-scale IC involving hundreds of high voltage devices, TCAD becomes very limited due to the amount of components, the time consuming FEM simulation, and the complexity of layout and placement of devices. All these limitations impact significantly the estimation of the circuit's ESD and latch-up behavior for a successful design in CMOS technology. Therefore, an accurate and even simple to use substrate extraction CAD tool is highly demanded.

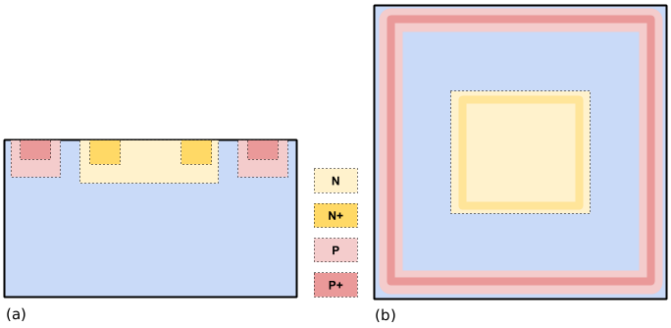


Fig. 1. Simple diode layout: (a) diode cross section view, (b) top side view.

In this paper, a fundamental extraction flow is illustrated. We present the modeling of the substrate by a three-dimensional extraction of enhanced resistors and diodes that has been presented in [12], [13]. Pattern based extraction strategies with intelligent computation algorithms are employed, for the purpose of delivering highly accurate, efficient and simple tool. This will facilitate the usage and dramatically reduce the cycle of development and verification of substrate noise before first-silicon fabrication.

This paper is organized as follows: in section II, we introduce a simple design diode as a case study, in section III, a general extraction flow is illustrated. Finally, the concluding remarks are in section IV.

II. Case study

We study the simple diode structure presented in figure 1. The diode consists of an N-well in the middle of the P-doped substrate and is surrounded by P+ doped diffusion area. All those layers are presented as two-dimensional shapes (rectangles and/or multi-paths) in the layout database in our design environment.

III. Proposed extraction flow

The diagram representing the proposed extraction flow is depicted in figure 2. The extraction tool is developed using OpenAccess [14] which is a common and open C++ database for integrated design tools and design methodologies. OpenAccess give access to shapes, geometries and the coordinates

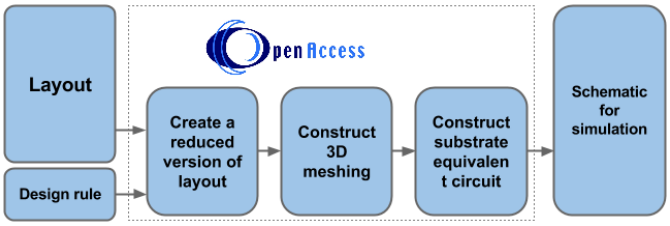


Fig. 2. The overall substrate extraction flow proposed.

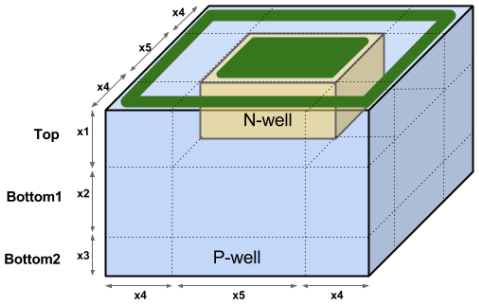


Fig. 3. Three-dimension view of reduced layers: the bigger light-blue cube representing the P-type area, the small gray cube representing the N-type area, and green shapes on the top for the diffusion area

of the physical layers. With this layout geometrical database, we are able to extract the substrate network and produce an OpenAccess schematic view that is ready for simulation.

Four main steps are involved in this extraction flow:

1) Design rules definition to define extraction rules to apply.
2) A version of layout which comprises only the layers contributing in the substrate parasitics (more details discussed in section III-B);
3) Three-dimensional meshing construction by using the developed reduced layout (more details in section III-C);
4) An equivalent three-dimensional substrate network extraction that produces the corresponding circuit netlist (more detail in section III-D).

A. Design rule definition

During the preprocessing stage, the substrate extraction rules are declared in a standard Extensible Markup Language (XML) database file. An example of extraction rules is presented below.

```
1  <Wells>
2    <well name="Top" depth="x1e-6"/>
3    <well name="Bottom1" depth="x2e-6"/>
4    <well name="Bottom2" depth="x3e-6"/>
5  </Wells>
6  <Bypass>
7    <layer name="MET1" preserve="true"/>
8    <layer name="VIA1"/>
9  </Bypass>
10 <Operations>
11   <merge name="DNTUB"/>
12   <contact diffusion="DIFF"/>
13   <setFilePath path="netlist/"/>
14 </Operations>
```

Three sections implementing extraction rules are shown:

1) Substrate well depths are given in the section with keyword “Wells”, between line 1 to 5;
2) “Bypass” section automatically removes the unused layer data, from line 6 to 9 (c.f. details given in the next subsection);
3) Customized extraction operations are used to customize the extraction results, with section keyword “Operations”, between line 10 to 14.

B. Reduced layout extraction

Traditionally, for a given layout, many layers are used and stored in layout database. Practically, only few of them will be reused for extraction strategy of substrate network. Metal Layers, such as METAL layers and VIA layers, etc will be ignored since they do not contribute to substrate noise. To define unneeded layers, we declare them inside the section “Bypass” in extraction rules file. Consequently, the extraction tool will keep only the desired layers data inside the layout database during the preprocessing stage. For example, lines 7 and 8 inform the extraction tool to ignore METAL1 and VIA1 layers during extraction.

Unfortunately, the obtained reduced layers may not completely satisfy the requirements of the meshing construction process, due to the complexity or repetitiveness of the drawn shapes. As an example from figure 1, the highly-doped N+ multi-part path shape forming the contacts is contained in the doped N rectangle shape. A simple “merge” operation applies for N doped layer could inform the extraction tool to ignore the path shape since it has been contained in a bounding rectangular shape. Moreover, other operations are defined such as:

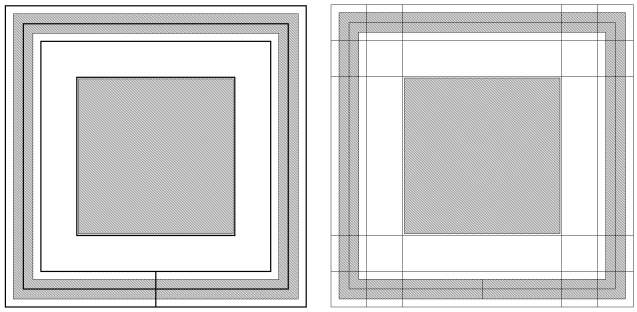
- “remove” to remove the target layer,
- “overlaps” to merge overlapped shapes,
- “setPath” to set produced file path

As a result of layout reduction, only diffusion, N-well and P-substrate shapes will be considered as shown in figure 3.

C. Three-dimensional Meshing construction

Commercially existing layout design tools draw the layers by using two-dimensional geometrical shapes, such as a rectangle, a path segment, a path, a polygon, etc. Firstly, we studied these two-dimensional geometrical shapes. Secondly, we implemented the extraction strategy by constructing a two-dimensional rectilinear meshing strategy. Construction strategies aims at constructing a highly accurate two-dimensional meshing network that fully emulates meshing in TCAD simulations. An example of a generated two-dimensional meshing matrix is shown in figure 4(b). Based on the original reduced layer in figure 4(a), it produce an 5x5 mesh cells. Each of these mesh cells represent four boundaries where minority carrier injected currents can be evaluated.

Applying the substrate extraction rules from the “Wells” section of the XML rules file, the substrate is subdivided into



(a) (b)

Fig. 4. Two-dimension view of: (a) reduced version of layers, (b) meshing network with diffusion (DIFF) layer.

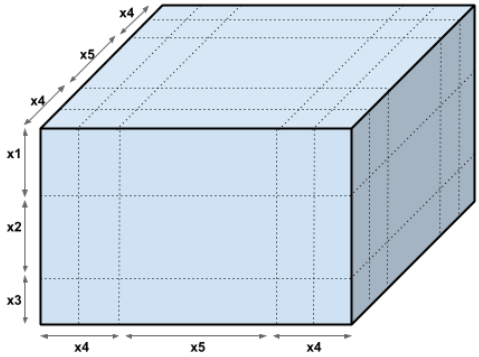


Fig. 5. Constructed 3D meshing network with 5x5x3 cuboids.

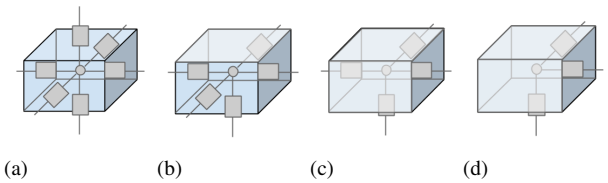
three conducting wells with different depths in the Z-direction. In our example, 5x5x3 cuboids shown in figure 5 will be generated using the depth value of each well. Each cuboid inside the 3D representation, stores *technological* information such as doping type, *geometrical* information (width, length and depth) and *algorithmic* information such as coordinate in the three-dimensional space.

D. Three-dimensional schematic extraction

Basically, the obtained three-dimensional meshing represents the whole substrate network. Therefore, the tasks for schematic extraction is to deal with these cuboids *technological*, *geometrical* and *algorithmic* information mentioned in the previous section.

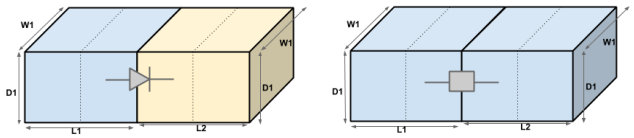
Algorithmically, each cuboid in the three-dimensional matrix directly defines the number of components to extract, as shown in figure 6. This figure illustrates a cuboid inside the 3D matrix and how it will generate substrate components in different cases:

(a) A cell in the middle of matrix will generate six components, four in horizontal plane and two in the vertical plane.
(b) A cell in the face of the 3D matrix will generate five components because no neighbouring cuboid exists on top of it.
(c) A cell in the edge of the 3D matrix will generate only four components,



(a) (b) (c) (d)

Fig. 6. Components extraction strategy for cuboid: 6(a) inside the substrate, 6(b) in the face, 6(c) in the edge, 6(d) in the vertex.



(a) (b)

Fig. 7. Component extraction strategy at neighbouring cells: (a) a diode is extracted if two neighbouring cells are doping type different, (b) a resistor is extracted if two neighbouring cells are the same doping type.

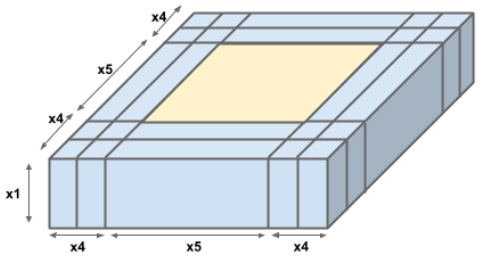


Fig. 8. Top layer of the substrate.

(d) A cell in the vertex of 3D matrix will generate only three of them.

Technologically, only three parasitic components can be extracted: the *EPFL enhanced diode* [12], [13], the *EPFL enhanced resistors* [12], [13] and the *homo-junction contacts* [9]. the type of component to extract is determined by the doping types of two neighbouring cuboids, as shown in figure 7, either to be a resistor (same doping type) or to be a diode (different doping type). Homo-junction contacts will be discussed below.

Geometrically, the size of each component is computed by examining neighbor cuboids in three-dimension, e.g. length(resistor)=L1/2+L2/2 for the resistor and length_AnodeP(diode)=L1/2, length_CathodeN(diode)=L2/2 for the diode P doping and N doping length respectively, both device areas equal to the cross-sectional area D1xW1 of the cuboid. Figure 7 illustrates these calculations.

E. Example of schematic extraction for one layer

According to the extraction method presented above, we illustrate the extraction results of the upper topmost layer of the diode in figures 9 and 10. A total number of 5x5 cuboids including one N-type cuboid in the middle of P-type cuboids, with the depth of "Top" layer equals X1 as shown in figure 8. After scanning all these cuboids, the extraction tool produces

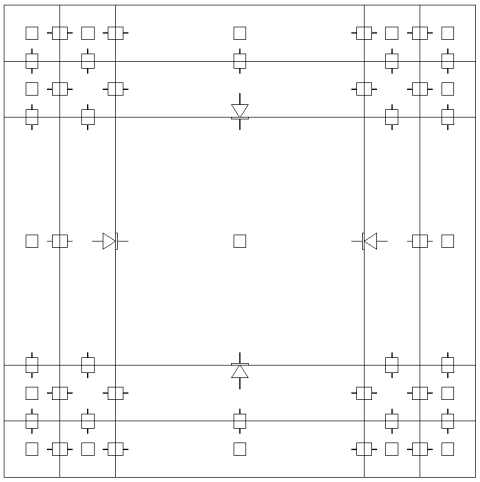
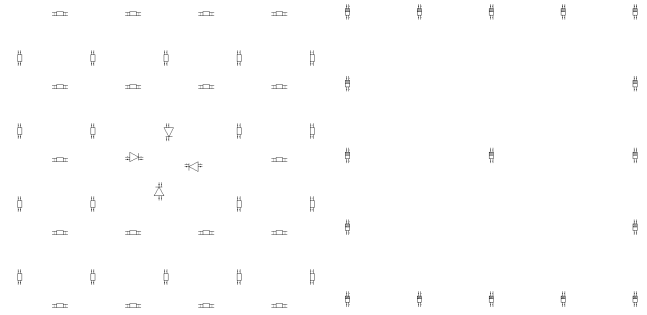


Fig. 9. Extracted view for the Top Layer.



(a) (b)

Fig. 10. Extracted netlist for Top layer: (a) horizontal contribution, (b) vertical contribution.

the substrate netlists into two separate files to distinguish the horizontal and vertical contributions to the substrate network. These contributions are shown in figures 10(a) and 10(b) respectively. In addition, each component is drawn in the individual layout view containing the meshing lines as shown in figure 9. We note that for the vertical contribution in figure 10(b), sixteen vertical homo-junction contacts [9] are generated: fifteen components generated by the cuboids in the edge of the substrate, plus one component generated at the center which is reduced into one center contact of N-contact.

IV. Conclusion

A novel Computer-Aided-Design (CAD) framework for substrate modeling is presented. The extraction steps of a simple diode illustrate the principal layout-to-netlist extraction flow. The substrate parasitic circuit can be directly back-annotated to the corresponding circuit for the purpose of simulation. In this way, the designer will be able to simulate substrate noise coupling before first-silicon fabrication. We have to mention that the simulation speed is shorter than that of the TCAD with an acceptable error. The next enhancement is to extend the extraction tool to deal with complete chips containing hundreds of devices. Consequently, the extraction tool will allow the designer to simulate and predict the circuit's ESD protection performance and latch-up immunity for automotive applications.

Acknowledgment

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