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Susceptibility Analysis of an Operational Amplifier Using On-Chip Measurement

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Abstract— This paper presents an electromagnetic immunity study of a simple operational amplifier by using the on-chip measurement. With the technology of on-chip non-invasive sensor, the internal inaccessible signal (voltage/current) can be obtained accurately in time domain. This approach grants a good insight in the internal transient response caused by the external electromagnetic interference. The validity of the on-chip measurement results is discussed comparing with the off-chip measurement and simulation.

Index Terms—integrated circuit, on-chip measurement, conducted susceptibility

I. INTRODUCTION

These last years, the susceptibility of integrated circuit (IC) has become an important issue for all circuit classes. To reduce the redesign time, the need for prediction of the risks of non-compliance during the design phase has become critical for IC manufacturers [1]. By using a circuit simulator with the available models of components (passive components, ICs, parasitic parts, transmission lines ...), the circuit functional failure caused by the electromagnetic interferences (EMI) could be predicted. From the simulation results, the design of circuit can be easily optimized. Although the simulation models are already very accurate, it's hard to consider and reconstruct all the elements of the real chips, especially the parasitic resistances, inductances and capacitances of interconnects, I/O pads, substrate or package. These elements play an important role in the filtering of high frequency interference. Several simulation results (e.g. I/O voltages) could be verified by off-chip measurements, like S parameters and probing testing [2]. However, verifying the exactness of the simulated voltage profiles of internal inaccessible circuit nodes requires on-chip measurement methods.

As a recent technology began in the early 2000s, the on-chip measurement has progressed a lot in the recent years [3] [4]. In [2], the authors have demonstrated the precise results of the on-chip measurement for high frequency signals in time domain, like crosstalk, delay, and supply bounce. These measurement results could be verified by the simulation. In [5], the first use of on-chip sensor for the characterization of the

coupling of external disturbances to IC power supply pin is presented. The comparison between the on-chip and off-chip measurements in [6] reveals the advantage of on-chip measurement in high frequency (more than 50 MHz). The differences between the two measurements is related to the power distribution network (PDN) which represents the physical interconnects of component, parasitic capacitances and the package pins.

As a common electronic block, failures of the operational amplifiers (OPA) caused by electromagnetic interference is widely discussed and analyzed by experimental measurement, simulation modeling and mathematical demonstrations [7] [8] [9]. The coupling of EMI on OPA inputs and power supply leads to a distortion of the output voltage, especially the generation of an offset. The origin of the problem lies in the distortion of the current which circulates in the differential pair. The characterization of these currents is essential to validate the exactness of a prediction model of the susceptibility to EMI, but this task remains difficult as the differential pairs are inaccessible.

This paper aims at presenting the susceptibility analysis of a simple operational amplifier based on the use of on-chip sensors. These sensors provide a precise time domain characterization of the voltage of internal nodes. It can help to understand the reaction of the amplifier to EMI, specially the currents of the differential pair, and to validate or improve the circuit model. Section II details the on-chip measurement method and the experimental set-up. Experimental results are presented and compared with the first simulation results in Section III. Finally, the conclusion and future work are provided in Section IV.

II. ON-CHIP SENSOR AND MEASUREMENT SETUP

A. On-chip sensor

The architecture and the principle of signal reconstruction of the on-chip sensor used in this test have been presented in [6] and are described in Fig. 1. An on-chip sample and hold (S/H) cell probes directly the voltage signal. The high input impedance of the probe ensures that the measurement is not

invasive. The sampling command is delayed by a delay cell. The delay is set according to the test frequency, in order to get a good time resolution of the reconstructed waveform.

With this method, a very high virtual sampling frequency can be achieved without the constraints of hardware bandwidth. According to [2], the bandwidth of sensor in our test (90 nm technique) is up to 14 GHz, which is sufficient for the measurements in this study (up to 2 GHz).

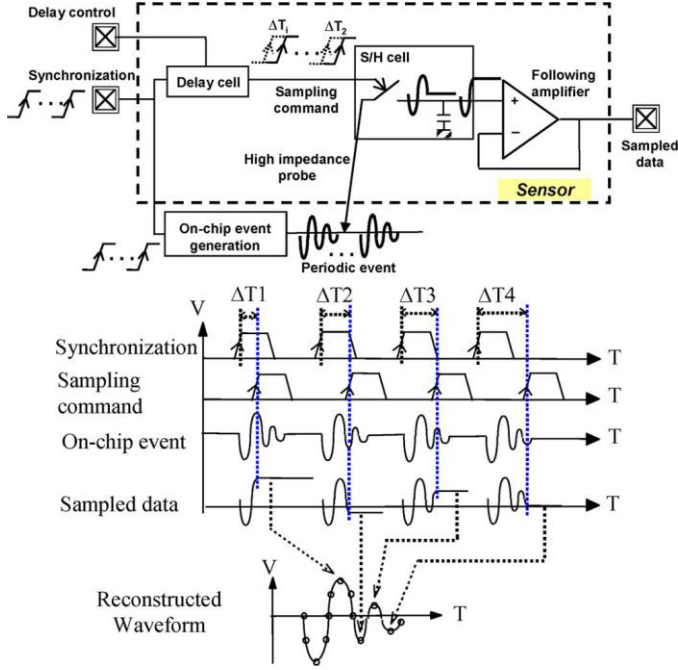


Figure 1. Architecture and the sequential equivalent-time sampling principle of the synchronous on-chip sensor [10]

B. Device under test

The amplifier under test is embedded in a test chip designed in Freescale[®] CMOS 90-nm process. It is a simple Miller operational amplifier with a P-channel input stage, in order to accept a common mode-voltage down to zero. As illustrated in Fig. 2, the input stage comprises 3 main parts: a differential pair of PMOS (M2 and M3), a bias current source of PMOS (M1) controlled by an external bias voltage (V_{bias}), and the active load (M4 and M5). The output terminal (V_{out}) is an amplified copy of the voltage difference between the two input terminals (V_+ and V_-).

Two 500 Ω current-sensing resistors are placed in both branches of the differential pair and four on-chip sensors are connected to the resistor terminals. The measurement of the voltages across each resistor provides the drain current of each transistor of the differential pair by using (1) and (2). The sensor measurements have to be synchronized to a same time references to ensure a correct extraction of the current.

$$i_m(t) = \frac{V_{im}(t) - V_{im2}(t)}{R_m} \quad (1)$$

$$i_p(t) = \frac{V_{ip}(t) - V_{ip2}(t)}{R_p} \quad (2)$$

The measurement repeatability of the on-chip sensor for low voltage (0 to 3.75V) is estimated to be ± 4 mV, adding with the accuracy of external equipment given as ± 3 mV, the accuracy of the low voltage sensor used in this device is ± 7 mV. Since two voltage sensors operate simultaneously for the current measurement, the accuracy of current i_m and i_p is evaluated to ± 28 μ A (± 7 mV * 2 / 500 Ω).

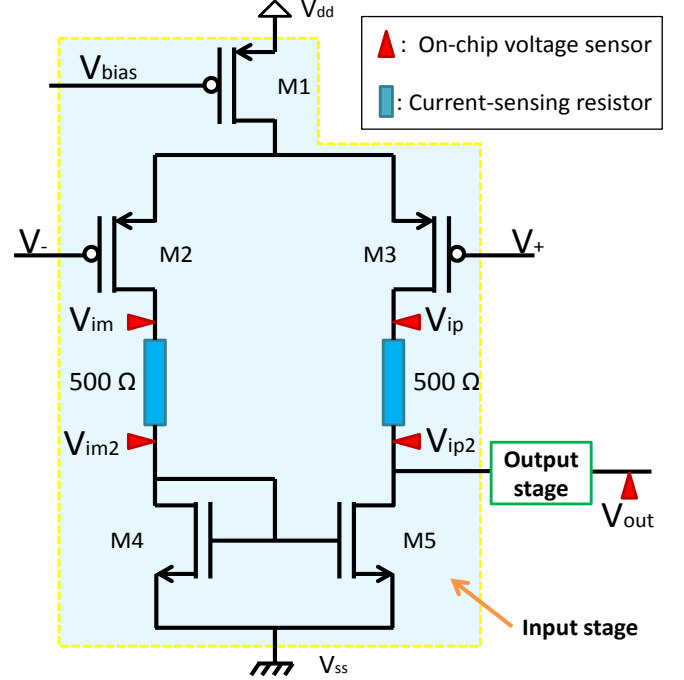


Figure 2. Operational amplifier structure and the positions of on-chip sensors

In this case study, the current of the differential pair is defined by the bias current, the addition of two current-sensing resistors has a little influence of the function of amplifier. That is why the 500 Ω resistors are chosen which we can get a good accuracy and a little voltage drop. If the value of the added current-sensing resistor is too important to modify the normal activity of the circuit, like the supply current measurement noted in [2], a small resistor like 1.5 ohm in this case could be used not to be too invasive, but on the other hand, the current measured will be less accurate.

A fifth on-chip sensor is also installed at the output terminal of the operational amplifier. This output voltage can be measured in the PCB card by an oscilloscope and a high-frequency probe, after a transmission via package, socket, PCB track and connector, which represent an important interconnect that will filter the timing profile of high frequency signals. This off-chip measurement could be used to verify the on-chip sensor result for DC or low frequency test.

C. Experimental set-up

As described in Fig.3, the operational amplifier is in voltage-follower configuration in our test, because this topology maximizes the susceptibility to EMI [11]. Normally, if there is no disturbance injected in the input terminal of voltage-follower, the output will track the input voltage. A conducted EMI voltage is superimposed to a constant voltage equal to 1.2 V and applied to the input of voltage-follower. Both the input and output voltage waveforms are observed by a 2 GHz oscilloscope with 2.5 GHz active probes. Finally, the analog signals of sensors are obtained and converted to digital by an acquisition card which translates the data to the computer where the waveforms are reconstructed by a post-processing program.

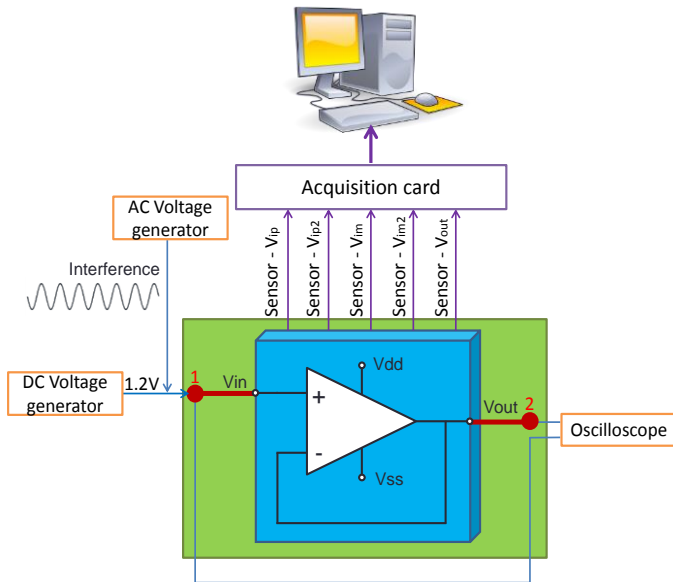


Figure 3. Experimental setup for the susceptibility analysis of the amplifier

III. EXPERIMENTAL RESULTS AND ANALYSIS

A. Off-chip and on-chip measurements

Among the five sensor test points, only the output voltage of amplifier could be compared with an external probe testing. EMI with a given amplitude A_{emi} is injected at various frequencies F_{emi} on the non-inverting input V_+ . As shown in Fig.4, a negative DC offset can be observed in the output by both external and on-chip measurements. Normally the AC part of the EMI-induced distortion is not very harmful because it can be filtered easily. However, the DC offset is nearly not possible to eliminate.

Although both measurement methods give almost the same result of DC offset, the waveforms are not exactly the same. An oscillation with frequency about 300 MHz is completely filtered by the interconnector between the internal V_{out} terminal in chip and the probe test point in the PCB card (Port 2 in Fig. 3). This phenomenon is clearly visible on the on-chip measurements.

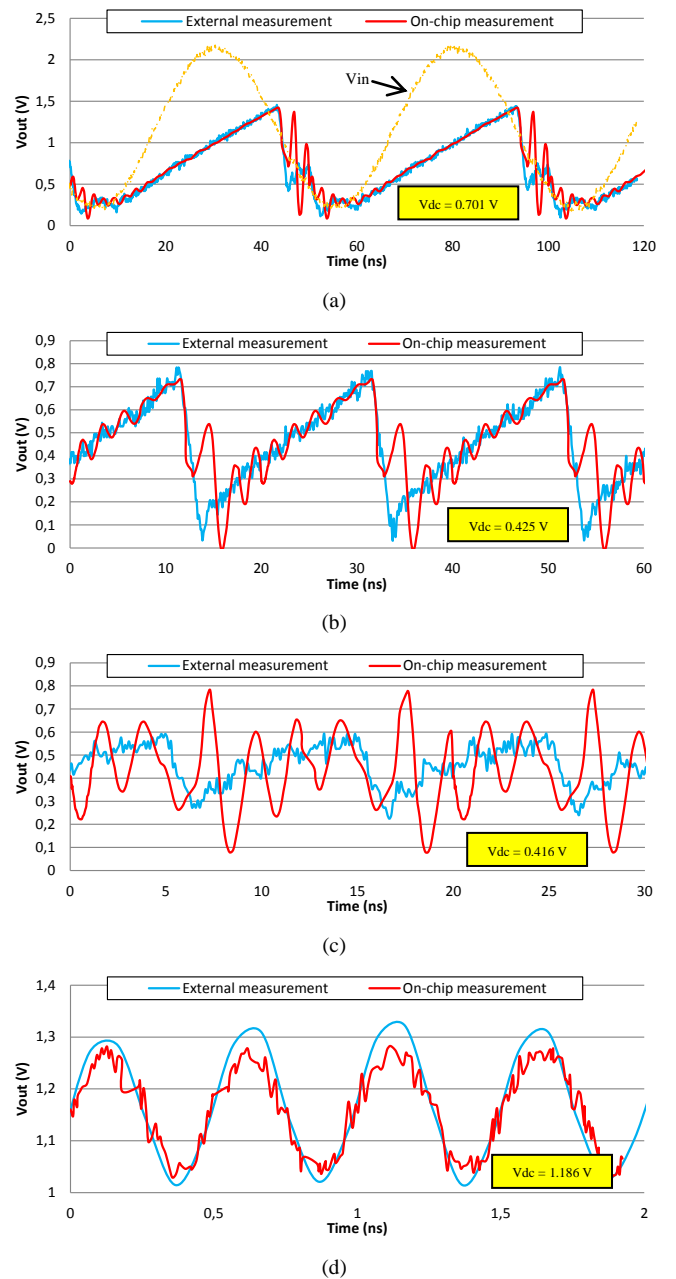


Figure 4. Comparison between external probe measurement and on-chip sensor measurement of V_{out} at same EMI amplitude $A_{emi} = 1V$ and different EMI frequency F_{emi} : (a) 20 MHz; (b) 50 MHz; (c) 100 MHz; (d) 2 GHz

B. On-chip current measurement

The on-chip measurement of current illustrates a good repetition, and a small dispersion between the different devices under test. Fig. 5 illustrates the two currents of the differential pair. The EMI injected in the input is the same as the case (a) of the V_{out} measurement (Fig. 4). The current waveforms reveal the distortions induced when the EMI is injected in the input. When the input voltage is higher than V_{out} , in the minus side the transistor is saturated, and the transistor of the plus side is blocked. The internal ringing exists also in the waveform of currents, but this oscillation is not as obvious as in the voltage measurement. The rapid peak could be related to the sensor

synchronization limitations. This point is still under investigation.

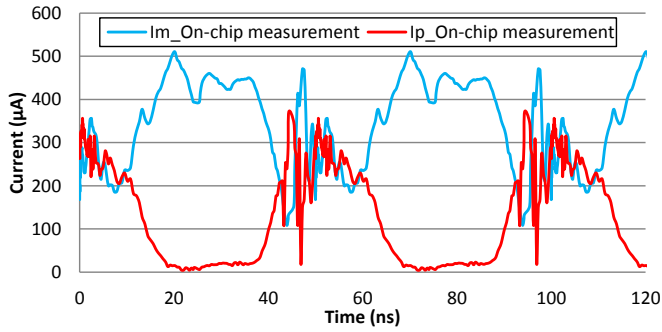


Figure 5. The current of the differential pair of amplifier measured by the on-chip sensor with EMI ($F_{emi} = 20$ MHz, $A_{emi} = 1$ V)

C. Modeling and simulation

As illustrated in Fig. 6, the modeling of system is constructed from the existing transistor net list. Besides, a first simple passive distribution network (PDN) model is built from a two-port S parameter characterization between port 1 and port 2 in the PCB card, as noted in Fig. 3. This simple PDN model fits with the measured impedance profile up to 100 MHz. On-going modeling works are done to extend the validity range of this model. All the simulations are performed with Cadence.

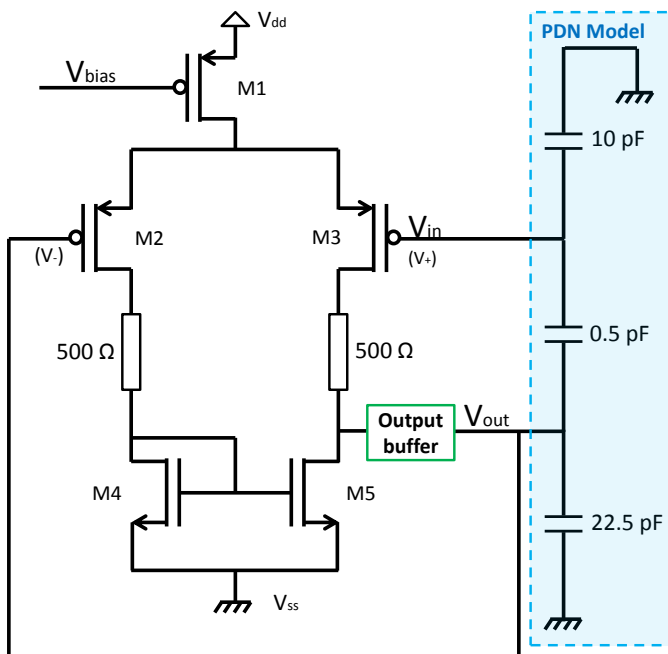


Figure 6. Modeling of the operational amplifier in voltage-follower configuration avec a preliminary PDN model

Fig. 7 illustrates the evolution of the internal current of the minus side of the differential pair for different DC values of input where no interference is injected. The simulation verifies the current value obtained by the on-chip measurement.

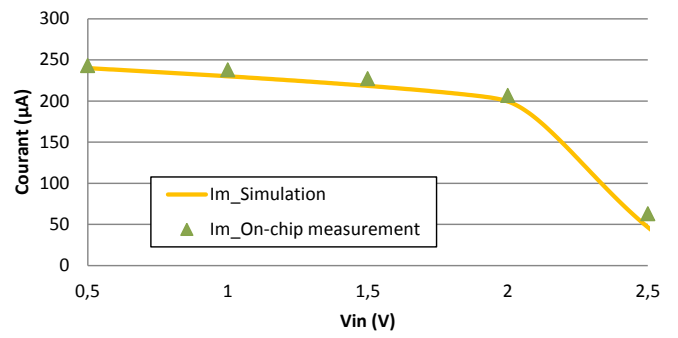


Figure 7. The comparison of the current of the minus side of differential pair of amplifier between on-chip sensor and simulation without EMI

This preliminary susceptibility simulation is limited to 100 MHz owing to the precision of PDN model. As shown in Fig.8, the simulation demonstrates the activity saturation/blockage of differential currents, and the current level of simulation fits well with the measurement. However, there is a gap of saturation/blockage time of transistor between the simulation and the measurement, this difference may relate with the internal parasitic elements which are not modeled enough accurately in the simulation. Both the DC and susceptibility simulations validate the results of on-chip current measurement.

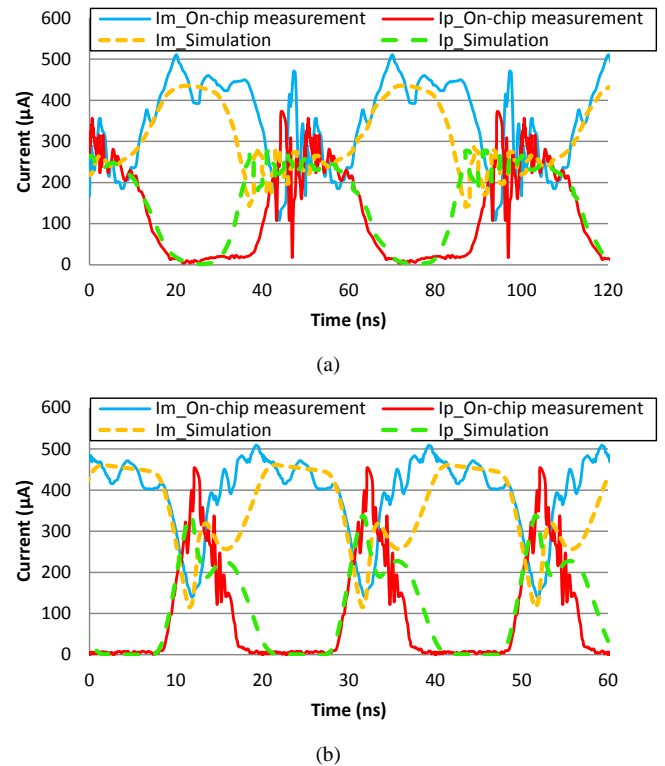


Figure 8. The comparison of the current in the differential pair between on-chip sensor and simulation with EMI: (a) $F_{emi} = 20$ MHz, $A_{emi} = 1$ V; (b) $F_{emi} = 50$ MHz, $A_{emi} = 1$ V

IV. CONCLUSION

This paper has presented an on-chip measurement method used in the susceptibility analysis of a simple operational amplifier. With the on-chip measurement, several important internal inaccessible signals could be observed, like the current flowing in a differential pair of an operational amplifier. Measuring these currents is very useful to understand the susceptibility of the circuit to electromagnetic interferences and to verify the modeling. According to the comparison with the off-chip measurement, the on-chip measurement reveals a good precision in the characterization of high frequency signals. A preliminary model of the operational amplifier has been proposed. The simulation results fit partially with on-chip measurements. Parasitic elements will be introduced in the model to extend its validity at higher frequency.

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