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The Riemann Pump: a Concurrent Transmitter in GaN technology

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Abstract—An original arbitrary waveform generator (AWG) architecture suited for software radio (SR) transmission is presented. A piecewise linear approximation of the wanted signal is generated thanks to a predefined set of slopes. The digital-to-analog (DA) conversion involved in this operation is based on a differential digital coding which drives a custom digital-to-analog converter (DAC), named here the Riemann Pump. This circuit is in charge of outputting the piecewise linear signal by integration of current steps into a capacitive load, potentially being the input impedance of a power amplifier. Simulations have been carried out on a first design, developed in a GaN technology, with a configuration that covers 1 GHz bandwidth with an oversampling ratio (OSR) of 4 and 3 input bits. The generation of concurrent modulated signals is demonstrated, with a rejection of 30 dBr over the whole band. The system exhibits promising performances as for the realization of a multi-standard concurrent radio frequency transmitter with moderate hardware complexity.

I. INTRODUCTION

The growing demand for data services induces the need to improve the handling capacity of the wireless network, with limited frequency resources. This problem could be addressed by the advent of cognitive radio [1], where the static allocation of frequency bands is replaced by a dynamic spectrum management. Such a system is based both on smart network supervision and adaptive radio transceivers. In order to achieve flexible transceivers, the trend is to bring the digital part as close as possible to the antenna, which leads to software radio (SR) architectures [2]. One of the most burning issue is brought by high speed conversion between the digital domain where data processing is performed and the analog domain which enables the propagation of the electro-magnetic signal via the antenna, and vice versa [3]. Regarding transmitter architectures, special efforts are made on the digital-to-analog converter (DAC), which is now intended to cover the whole transmission band, enabling direct generation of modulated signals [4]. The trade-off between conversion performances and resource consumption (power, die area and cost) does not provide viable solutions to address mass market yet; it is however necessary to do so in order to develop large cognitive radio networks. A widespread trend consists in generating bandwidth limited signals that correspond to various standards with an energy efficient method, and then to digitally carry them at the desired frequency [5]–[8]. It leads to reconfigurable systems that often enable concurrent multimode transmission,

but still with less flexibility than a true software radio transmitter. Numerous wideband DACs and signal generators that handle a several gigahertz frequency band have also been presented [9]–[11]. It is then possible to directly generate any combination of modulated signals lying into this band. They rely on a pulse code modulation with a medium to large number of bits (6 to 14) to achieve a high enough signal quality; it usually turns out resource intensive in terms of pin count and power consumption.

An original SR transmitter architecture which will be called the Riemann Pump is presented in section II.

An implementation of the developed architecture is introduced in section III through a design of the Riemann Pump in a GaN technology provided by United Monolithic Semiconductors (UMS). Simulations are carried out on this design with the software Advanced Design System (ADS). Results exposed in section IV show the concurrent generation of modulated signals with carriers distributed in the [0-1GHz] band, evidencing the validity of the principle to address software radio transmission purposes.

II. RIEMANN PUMP ARCHITECTURE

The purpose of the presented system is to generate arbitrary waveforms up to the GHz range with a low cost and low consumption solution, the main target being the generation of modulated signals to address SR applications. At first, the wanted signal is available in a high resolution digital representation. This signal is converted into a lighter size with a specific differential coding, and then converted in the analog domain thanks to a suited DAC, called the Riemann Pump.

An analog version of the wanted signal is thus generated thanks to a pre-determined set of slopes. The generation process can be implemented as shown in Fig. 1. A Digital Signal Processor (DSP) computes the Riemann code (i.e. the slopes index sequence) from the theoretical desired signal. This code controls switched current sources, in order to produce current steps that are integrated into an output capacitive load, producing a piecewise linear approximation of the wanted signal. The current sources and the capacity of the load are calibrated with respect to the wanted bandwidth and dynamic. The digital to analog (DA) operation consists in pumping charges into a capacitor to generate the wanted signal. It involves integration over time to approximate this signal, reminding us of the Riemann Integral. The developed

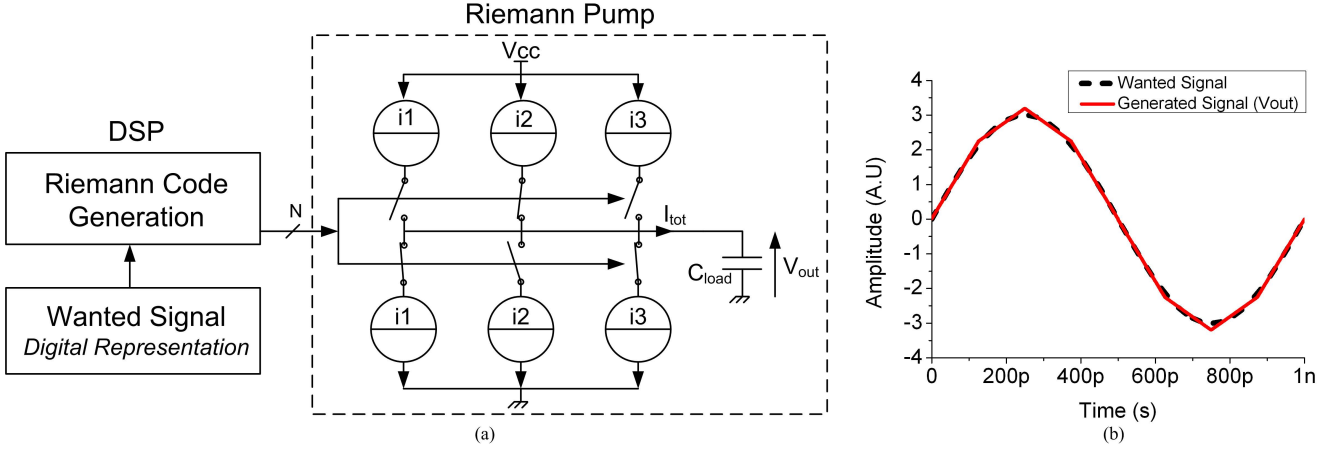


Fig. 1. Transmitter architecture (a) and theoretical signal generation (MATLAB) (b).

circuit is named the Riemann Pump, in reference to this founding principle.

The Riemann code generation process is described thereafter. The analog representation of the theoretical wanted signal is noted y . Let y_s be the sampled version of y at the frequency f_s (which is the maximum switching frequency of the Riemann Pump), and x the corresponding discrete time index sequence, as shown in Fig. 2. The Riemann integral of y , with respect to x , corresponds to the integral of the staircase function that is worth $y_s(k)$ on every interval $[x(k), x(k+1)]$. At each step k , the chosen slope minimizes the difference between the Riemann integrals of y and of its piecewise linear approximation (defined by the sequence y_r), on the interval $[x(k), x(k+1)]$. This difference, noted $e_r(k)$, is worth:

$$e_r(k) = |y_s(k) - y_r(k)|[x(k+1) - x(k)] \quad (1)$$

This is equivalent to choosing the slope that minimizes the quantity:

$$e_q(k) = |y_s(k) - y_r(k)| \quad (2)$$

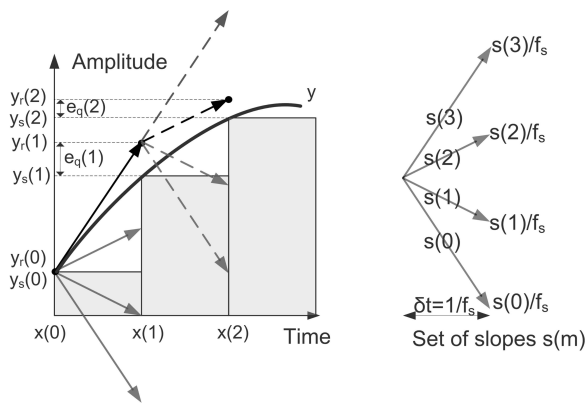


Fig. 2. Riemann reconstruction process.

An example is given with a set of four slopes (Fig. 2), represented as a sequence of real numbers $s(m)$. We have to calculate the sequence of slopes that generates the piecewise

linear signal giving the better approximation of y (in our case the one that minimizes at each step the difference between Riemann integrals). Considering the depicted example, $y_s(0)$ and $y_r(0)$ are equal. From this point, four values are possible for $y_r(1)$, according to the following equation: $y_r(1) = y_r(0) + \frac{s(m)}{f_s}$, with m belonging to $\llbracket 0, 3 \rrbracket$. The value that minimizes $|y_s(1) - y_r(1)|$ is then chosen, $s(3)$ in this example. The process is iteratively repeated for each new step; giving the slope $s(2)$ as the best to calculate $y_r(2)$. The encoded signal that allows us to reconstruct the piecewise linear signal consists of the slopes index sequence. This system is intended to provide an effective way of generating signals, in terms of circuit complexity and bandwidth.

III. RIEMANN PUMP CIRCUIT

A first version of the Riemann Pump is designed in a GaN technology, with HEMT transistors [12]. This technology is suited for power applications, in particular in base station transmitters; the purpose is to drive a power amplifier directly with the Riemann Pump, in order to integrate the whole analog part of the transmitter into a single chip. In this configuration, the capacitive input impedance of the power amplifier replaces the output capacitor of the Riemann Pump. The circuit described herein solely corresponds to the Riemann Pump alone; the integration with a power amplifier will be the subject of a subsequent work. Regarding circuit design techniques, the most important feature is related to the nature of the transistors. Only normally-on N-type transistors are available, which impacts the circuit design. Furthermore, those transistors have a negative threshold of several Volts and a consequent size, limiting their switching speed. A trade-off between circuit complexity and conversion performance leads to a number N of 3 bits. The frequency limitations enable a switching frequency of 8 GHz, allowing the generation of signals up to 1 GHz with an oversampling ratio (OSR) of 4.

The relative value of the slopes is represented in Fig. 3(a); they observe a constant step between them. The circuit architecture implemented to generate those slopes is presented in

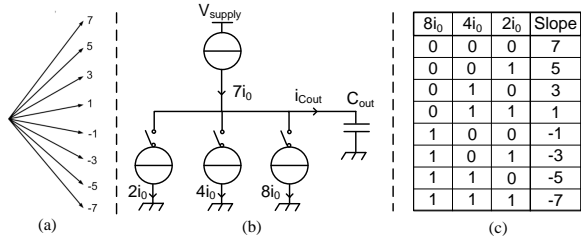


Fig. 3. Slopes Generation.

Fig. 3(b). The absence of P-type transistors in our technology makes the realization of switches on the top rail inefficient. The developed pump topology thus uses only switches on bottom rail current sources, whereas the top rail supplies a constant current. The current i_0 is used as a reference that depends on the calibration of the maximum slopes. The top supply rail delivers a current $7i_0$, while the bottom rail pulls a current depending on the state of the 3 switches, which are controlled by the 3 coding bits. The resulting current, which is worth the sum of the pushed current and the pulled current, goes into the output capacitor. The lower current sources are calibrated in order to generate the wanted slope distribution described above. Respective values of $2i_0$, $4i_0$ and $8i_0$ lead to the wanted slope set, depicted in Fig. 3(c). The pump topology is exposed more precisely in Fig. 4.

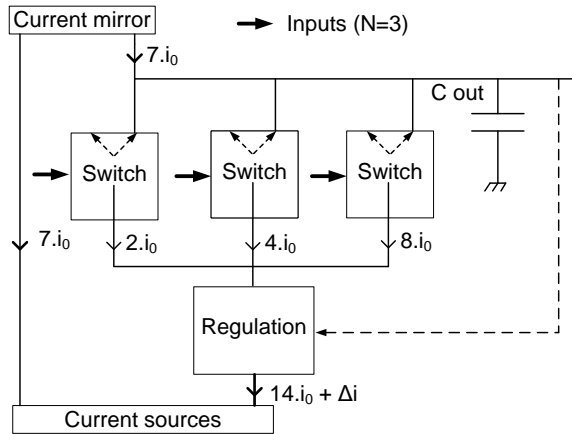


Fig. 4. Riemann Pump circuit topology.

The bottom current sources are derived from a unique source which pulls $14i_0$, while the top source is mirrored from another bottom source that generates $7i_0$. Differential switches are placed on the 3 current branches, so as to pull the corresponding current either from the output capacitor, or from the supply. The current $7i_0$ is pushed continuously from the top supply rail. The output capacitor voltage represents the reconstructed signal; it results from the integration of the constant current steps. Since the system is pumping charges onto the capacitor, any imbalance between the rails could cause a drift of the output voltage. To prevent this effect, a regulation block is inserted onto the bottom current source; it

ensures the mean voltage across the output capacitor remains constant by balancing the bottom rail current generation with respect to the top rail current; it provides robustness to temperature and technological dispersion.

IV. CONCURRENT TRANSMISSION SIMULATIONS

The layout of the designed circuit is displayed on Fig. 5, it occupies a $2.7 * 2.2mm^2$ area. The circuit has an estimated consumption of 200 mW from a 15V supply.

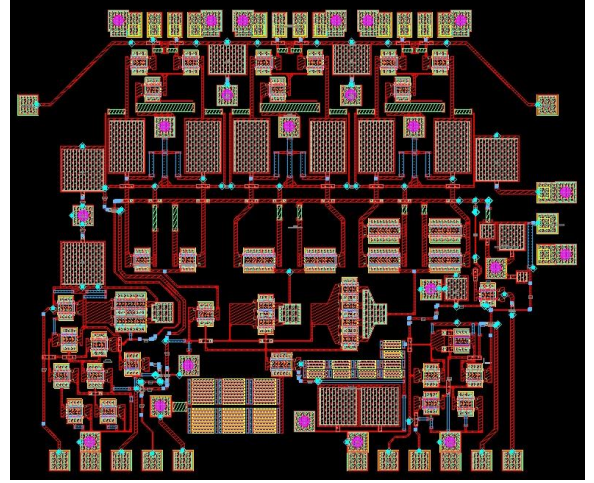


Fig. 5. Layout of the Riemann Pump in GaN technology.

In order to assess signal generation performances of the presented transmission architecture, the following simulation flow has been followed. First of all, the theoretical wanted signal is generated with Matlab; samples are taken from this signal, at the sampling rate f_s of 8 GHz. The Riemann code is computed, generating 3 bit streams corresponding to the control sequences of the 3 switches of the Riemann Pump. These streams are then applied to the inputs of the circuit realized with ADS (schematic and layout), and a transient simulation is launched. Once completed, the output signal of the circuit, namely the voltage across the output capacitor, is saved and processed under Matlab.

The objective of the presented transmitter is to perform concurrent transmission, with different carrier frequencies, bandwidths and modulation schemes. The example presented below shows the generation of a signal containing 3 different modulated signals. The first step is to generate the wanted signal resulting from the sum of the 3 modulated signals, each signal being obtained by the multiplication of a carrier and its corresponding data symbol stream (shaped with a square root raised cosine filter). This signal is then processed as described above and the output voltage is obtained after simulation. Receiver chains suited to each of the 3 transmitted signals are then reproduced with Matlab to assess the quality of transmission. The signal is independently multiplied by the 3 original carriers; the 3 obtained signals are then passed through the filters matched to the respective transmission filters. Processing is then performed onto the 3 obtained signals

to generate eye patterns and constellations. The generated signal consists of the sum of the 3 signals described hereafter. The first corresponds to a QPSK modulation, with a carrier at 600 MHz and a symbol rate of 25 MSps (mega symbols per second). The second one is a MSK modulation, with a carrier at 900 MHz and a symbol rate of 50 MSps (which corresponds to the GSM frequency band and modulation scheme). A 16-QAM is generated as the third signal, with a symbol rate of 20 MSps, carried at 400 MHz. The resulting reconstructed signal power spectrum is displayed (Fig. 6), showing the 3 signal bands corresponding to the respective modulation features in terms of carrier frequency and bandwidth.

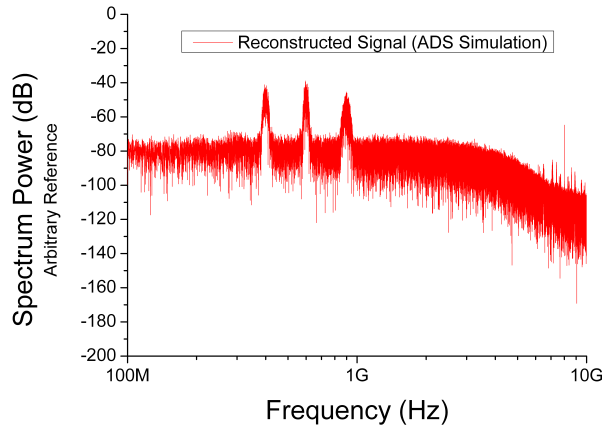


Fig. 6. Modulated signal spectrum – Logarithmic scale.

The noise floor is roughly flat up to half the sampling frequency (lying at about -30 dB with respect to the carriers). A component located at the reconstruction frequency f_s (8 GHz) is also present; it corresponds to the periodic commutations. The diagrams obtained after the demodulation process are exhibited (Fig. 7).

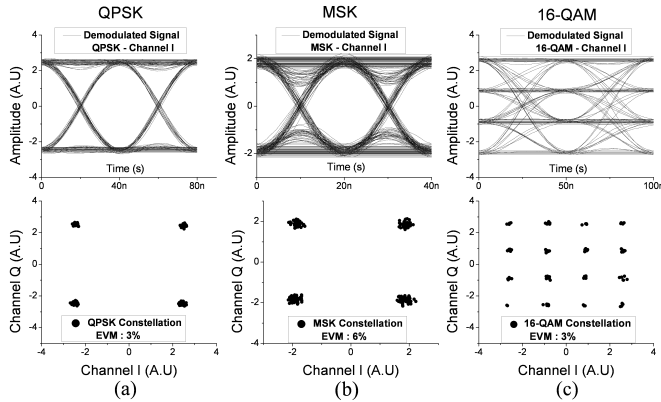


Fig. 7. Demodulated signals – Modulation performances.

The eye diagram of the in-phase channel (channel I) and the constellation for each modulation are displayed in a column of Fig. 7 (respectively (a), (b) and (c)). The error vector

magnitude (EVM) is calculated for each constellation. The signals are not supposed to respect any standard but these EVM values of several percents seem promising as for concurrent transmission of any combination of modulation scheme, carrier frequency and bandwidth. The presented results have been obtained with a moderate OSR and a low number of bits N . It is possible improve the transmission quality by tuning these 2 parameters.

V. CONCLUSION

An original architecture of SR transmitter has been presented in this paper and implemented through a GaN design, optimized for the co-integration with a power amplifier in the same technology; it can be used in base station transmitters. Simulation results confirm the ability of the architecture to handle concurrent transmission of modulated signals over a 1 GHz frequency band, with a fair signal quality. The realization of the presented prototype is planned to provide measurement results. Furthermore, a version in a more common CMOS technology is also considered, to address mobile devices applications.

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