Comparison of junction temperature evaluations in a power IGBT module using an IR camera and three thermo-sensitive electrical parameters

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***Abstract* -- The measurement of the junction temperature with thermo-sensitive electrical parameters (TSEPs) is largely used by electrical engineers or researchers but the obtained temperature value is generally not verified by any referential information of the actual chip temperature distribution. In this paper, we propose to use infrared (IR) measurements in order to evaluate the relevance of three commonly used TSEPs with IGBT chips: the saturation voltage under a low current, the gate-emitter voltage and the saturation current. The IR measurements are presented in details with an estimation of the emissivity of the black paint deposited on the power module. The temperatures obtained with IR measurements and with the different TSEPs are then compared in two cases: the use of only one chip and the use of two paralleled chips.**

***Index Terms*-- Chip temperature, IGBT, Infrared imaging, Multichip modules, Power semiconductor devices, Thermo-sensitive electrical parameter, Thermal measurement.**

I. INTRODUCTION

The junction temperature measurement of a power semiconductor device can be used to characterize thermal performances of its package and as a damage indicator of the power module principally for the detection of a delaminating process in the assembly [1]. Three main methods are used today to evaluate the junction temperature of power semiconductor devices [2]: optical methods, physically contacting methods and electrical methods. The main optical methods are local infrared sensors [3,4], optical fibers [5], infrared microscope [6,7] and infrared camera [8-10]. The main advantage of the IR camera is the possibility to directly obtain a temperature map of the power device. The junction temperature measurement can also be done directly contacting the chip with a thermo-sensitive material. The main solution is the use of thermal probes (thermistors or thermocouples) [11,12]. Although optical and physically contacting methods can be really accurate, the measurement time can hardly be lower than 1ms due to the electronic treatment or to the thermal capacitance of thermo-sensible materials. This is the reason why the common way to measure a junction temperature is the use of a thermo-sensitive electrical parameter (TSEP): the chip is itself the temperature sensor. However the accuracy obtained by this technique can be discussed because the chip temperature is very inhomogeneous. Therefore large junction temperature differences can be obtained using different techniques. As an example Jakopovic et al. [13] show that the measured thermal resistance of power MOSFETs in TO220 packages can vary from 0.9K/W using the channel resistance as a TSEP to 1.25K/W using the threshold voltage, i.e. a 25% difference between each measurement. The main problem of these results is that we do not know the real temperature of the semiconductor devices. A referential measurement using an optic or a physically contacting method could be interesting to explain this difference. In the case of IGBT chips, Schmidt and Scheuermann [8] and Perpiña et al. [9] propose a comparison between a TSEP and an optical measurement. These authors use the saturation voltage $V_{ce,sat}$ under a low current as TSEP [14,15] and compare it with the temperature obtained with an IR camera. Furthermore, Schmidt and Scheuermann [8] show that the temperature difference on the chip surface can reach 40°C. The use of the IR camera is therefore very useful because it provides a temperature map of the semiconductor surface. It makes it possible to determine if the temperature given by the TSEP is close to the mean, the maximum or the minimum temperature. In [8,9], the authors show that the chip temperature obtained using $V_{ce,sat}$ is really close to the mean surface temperature measured with the IR camera.

$V_{ce,sat}$ is today generally used for the thermal characterization of commercial IGBT power modules. However it would be interesting to determine if other TSEPs could be used with better temperature measurement accuracy. Therefore the present paper proposes to compare $V_{ce,sat}$ with two other TSEPs for the temperature measurement of IGBT chips: the gate-emitter voltage $V_{ge,I}$ [16] and the saturation current I_{css} [17-18]. Contrarily to previous studies presented in scientific literature, the comparison of these TSEPs will be carried out in same experimental conditions and using one single or two paralleled IGBT chips. In fact, in multi chip modules, the switches can be realized using one or several paralleled chips. This electrical configuration can have a non negligible impact on the choice of the TSEP. Furthermore, a referential temperature measurement with an infrared (IR) camera will be proposed to strengthen the results.

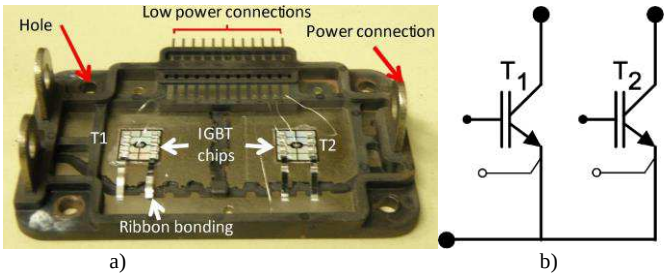
In the first part of the paper, the studied power module and the experimental setup are described. Then the principle of the IR temperature estimation including a calibration of the emissivity of the black paint is outlined. The goal of this section is to provide an accurate referential measurement method in order to compare the different TSEPs. Finally, calibration curves of these TSEPs and temperature measurements are presented and discussed.

II. EXPERIMENTAL SETUP

A. Presentation of the device under test

A dedicated unencapsulated power module free of gel has

been developed especially for this study in order to carry out infrared surface temperature measurements of the power components. The transistors are 600V-200A INFINEON IGBTs (SIGC100T60R3) with an aluminum metallization on the top surface. The power module and the electrical topology with two IGBTs are presented in Fig. 1. This topology is used to perform tests with one single chip or with two IGBTs associated in parallel. Each transistor chip is soldered on a separate copper substrate. As shown in Fig. 1, there are four holes in the corners of the power module. With these holes, it is possible to fix the module with screws on a cooling system. By torque adjustment, screws make it possible to modify the thermal resistance of the interface between the power module and the cooling system. Therefore, the thermal behavior of each silicon die can easily be modified separately as it will be presented in section V.



a) b)

Fig. 1. Power module dedicated to tests (a) and electrical topology (b).

The schematic cross section of the power module fixed on the water cooling system is presented in Fig. 2. The IGBTs power electrical connections are made with aluminum ribbons. They have been chosen because the area viewed by the IR camera is larger than this obtained with wire bonding [8]. Fig. 3 presents the surface temperature distribution on a 100 W dissipating IGBT chip.

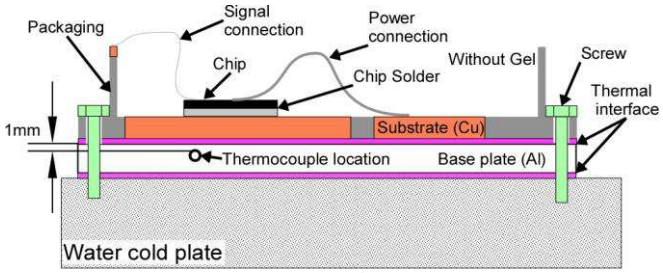


Fig. 2. Power module assembly fixed on a water cold plate.

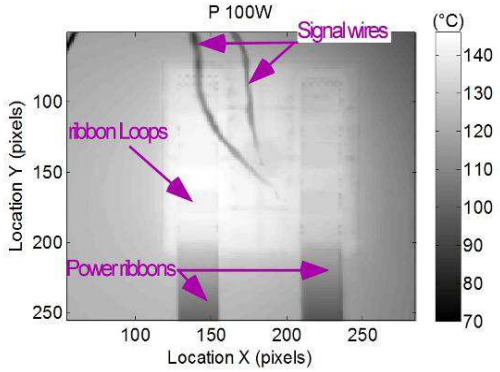


Fig. 3. Surface temperature distribution of a dissipating IGBT chip.

B. *Presentation of the test bench*

The test bench is developed around an infrared camera mounted on a manual positioning solution (Fig. 4). The infrared camera is a TITANIUM 550M CEDIP system (SC7500 FLIR). The measurements are done in the middle wavelength range (3.7µm to 4.8µm) with InSb matrix sensors of 320x256 active cells. All infrared measurements were performed in thermal steady state conditions during 1s with a 100Hz frequency rate. The spatial resolution of the infrared image is defined with an adapted lens which permits a pixel size smaller than 100µm per 100µm.

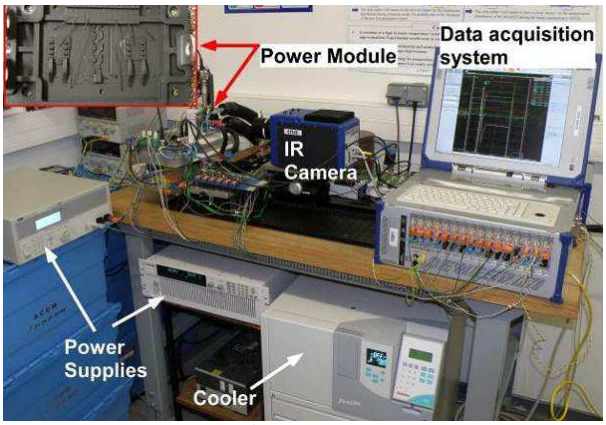


Fig. 4. Test bench for IR and TSEP measurements.

The temperature of the black painted power module is controlled from 40°C to 180°C by the cold plate connected to a temperature control instrument (JULABO Presto). All electrical measurements are made with a DEWETRON data acquisition system (DEWE5000) associated with a dynamic differential isolation amplifier (bandwidth up to 300kHz). The voltage accuracy of this system is 0.04%. All TSEPs are measured with a specific electronic circuit. This circuit is driven by a LabView program and a NI USB-6259 board connected to a computer.

III. INFRARED (IR) MEASUREMENTS

A. *Control and calibration of the surface emissivity*

Large temperature measurement errors may be done using infrared measurements due to the surface degradation of materials and the intrinsic low emissivity of aluminum (<0.1) with a complex geometry of the active parts [19]. Thus, the infrared temperature measurements of power components were conducted controlling the surface emissivity with a paint solution. Experimental campaigns are conducted in order to evaluate the emissivity of two selected paints adapted for operating temperatures from 40°C to 180°C (MOTIP and ACRYL RAL). The paint coats are deposited on a copper base plate (5mm thick) which is thermally controlled with a water cold plate. These elements are thermally isolated with polytetrafluoroethylene material (PTFE) which limits the convective and radiative heat transfers and thus the temperature gradients in the base plate. Windows are realized

in the PTFE part in order to make temperature infrared measurements of the painted surface. Fig. 5 presents the test bench used to qualify the emissivity of different paint solutions versus the temperature.

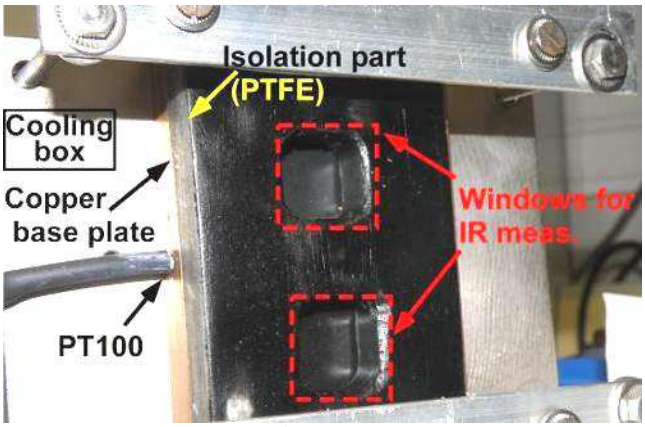


Fig. 5. Test bench for the emissivity evaluation.

The referential temperature (T_{ref}) is evaluated with a RTD temperature sensor (PT100 class 1/10 ±0.06K) connected to a 6.5 digit precision multimeter FLUKE 8846A. The propagated error of the measurement chain is calculated close to ±0.12K. This temperature measurement is located in the center of the copper base plate close to the surface measurement areas. Table I presents the synthesis of the paints and the conditions of use.

TABLE I
DETAILS OF EVALUATED PAINTS

Paints	Number of coats	Times between 2 coats (s)	Finish conditions
ACRYL RAL 9005	8/12/16/18/20/24	180	60min/25°C
MOTIP 04031	8/12/16/24	60	60min/160°C

The infrared temperature measurements are performed with FLIR software emissivity parameter set to one ($T_{IR@\varepsilon=1}$). First, an evaluation of the coats number impact is conducted for a referential temperature close to 100°C. This temperature is arbitrarily chosen. In fact it is representative of temperature conditions that are required to have a good accuracy of the infrared measurements, and it is also in the temperature range of the experimental campaign presented in sections IV and V. A mean value is calculated from one hundred infrared measurement images in order to limit the mechanical vibration impact. As we can see in Fig. 6, the number of paint coats impacts on the standard deviation of the temperature measurements (Std MOTIP and Std ACRYL RAL) and on the difference between T_{ref} and $T_{IR@\varepsilon=1}$ which is representative of the paint emissivity value (DT MOTIP and DT ACRIL RAL). The ACRYL RAL solution presents a higher dispersion due to difficult conditions to adjust the paint coat deposition.

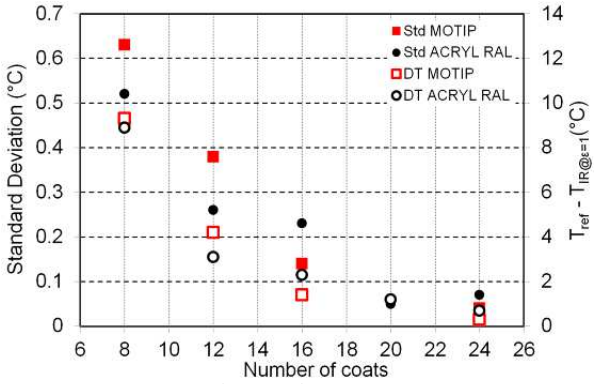


Fig. 6. Influence of the coats number.

The emissivity evaluation versus temperature has been conducted for both paints from 40°C to 180°C. The emissivity evaluation is realized with the same test bench. The infrared temperature measurements are made in steady state conditions. The emissivity parameter is set to one in the FLIR software. These measurements are realized on an area (10mm x 10mm) of each painting zone in the center of the measurement windows presented in Fig. 5. The size of each area is defined to be close to the size of the IGBT chips which are tested in sections IV and V. The mean temperature of each area (1368 pixels) is compared with the referential temperature measured with the PT100 sensor located in the copper base plate just under the location of measurement areas. A first Matlab program is developed with dedicated FLIR functions. The corrected emissivity of the paint is estimated using the program in order to obtain a mean temperature as close as possible to the referential temperature (provided by the PT100 sensor). Fig. 7 presents the results of the corrected emissivity evaluation as a function of the temperature for both the MOTIP and ACRYL RAL paints with 24 coats.

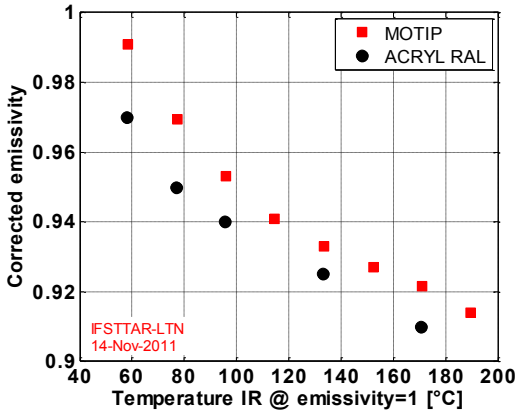


Fig. 7. Evaluation of the emissivity versus the infrared temperature measurement with 24 coats.

An extrapolation of the corrected emissivity variation versus the temperature is calculated. A quadratic interpolation is used to fit the experimental results. Equation (1) presents the expression of the corrected emissivity interpolation for the MOTIP paint.

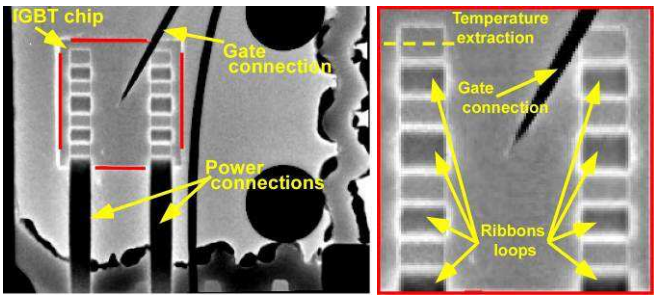
$$\varepsilon_{corr\,MOTIP} = 3.6810^{-6} \times \left(T_{IR@\varepsilon=1}\right)^2 - 1.462110^{-3} \times T_{IR@\varepsilon=1} + 1.0618 \quad (1)$$

where $\varepsilon_{corrMOTIP}$ is the corrected emissivity and $T_{IR@\varepsilon=1}$ is the infrared temperature measurement with a fixed emissivity equal to one.

In this paper, all infrared temperature measurements of IGBT dies are made with the MOTIP black paint. On one hand, the coat number is fixed to twenty four in order to guaranty the good temperature measurement in steady-state conditions. On the other hand, the infrared temperature measurements are calculated from the averaging of one hundred infrared acquisition frames in steady state conditions. The paint layer thickness has been measured to be lower than 100µm ±3µm. It seems to be acceptable for the presented comparison approach. Indeed, we have estimated that the temperature difference between the chip metallization surface and the measurement paint surface is lower than 1K Furthermore, this temperature difference is taken into account in the calculation of $\varepsilon_{corrMOTIP}$ which is carried out under the same experimental conditions.

B. Post-processing of IR images for the evaluation of the chip temperature

A second Matlab program has been developed in order to extract the useful chip temperature. As presented in Fig. 8a, the infrared image is analyzed in order to perform an orthogonal adjustment with the edge detection of the IGBT chip under test. Fig. 8b shows the IGBT view after automated cropping.



a) b)

Fig. 8. Image extraction of the IGBT chip from the infrared acquisition.

As shown in Fig. 8b, the image of the chip temperature from the infrared acquisition is not directly usable. Fig. 9 shows a schematic presentation of the top view of the IGBT chip with the active parts specified in black color.

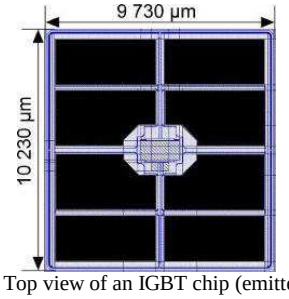


Fig. 9. Top view of an IGBT chip (emitter side).

The chip temperature which is measured by thermosensitive electrical parameters is the temperature of the active parts. Therefore the IR measurements have to be carried out only on these parts. Furthermore, some areas of the active parts are hidden by other elements like ribbon or wire connections. It is therefore necessary to create a numerical tool in order to evaluate the temperature of the active parts only. The elements which have to be excluded from the chip temperature calculation are the following:

- The gate connection which crosses the chip image from the right top corner to the center of the chip,
- The power ribbons loops used to connect each active area of the IGBT chip,
- The inactive areas of the chip which are presented in Fig. 9 (gate pad, passivation…),
- The temperature measurement artifacts due to geometric specifications of ribbons and disturbances due to the paint deposition.

This last point is demonstrated in Fig. 10 with the temperatures extraction along the line presented in Fig. 8b. For this measurement, the IGBT chip is not crossed by any current, the heat dissipation is therefore equal to zero. The temperature of the chip is regulated by the cold plate. Its temperature is 60°C Therefore, the surface temperature should be quasi homogeneous on the whole surface of the IGBT chip. Fig. 10 shows that the temperature of the ribbons stiches areas is close to this of the active parts of the chip but there are thermal artifacts between stiches and chip areas which are due to optical effects. These artifacts have therefore to be excluded from the surface temperature calculation.

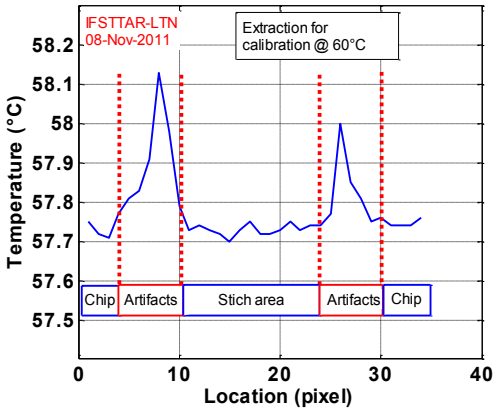
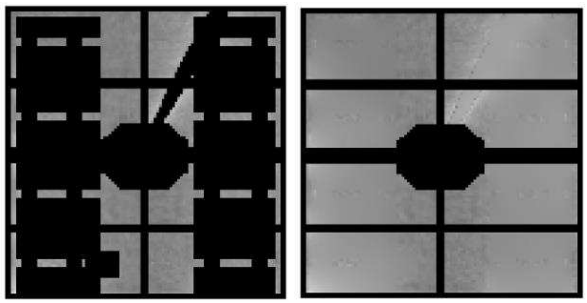


Fig. 10. Profile extraction of the IR temperature measurement along a ribbon stich area (cold plate temperature 60°C).

As presented in Fig. 11a, numerical masks are used to exclude the unusable areas of the infrared temperature measurement of the IGBT chip. These black areas define the temperature zones which are excluded for the raw temperature calculation. The temperature initially measured with an emissivity equal to 1 is corrected during the post-treatment with the corrected emissivity expression presented in (1). Finally, a temperature extrapolation is made with the help of local bilinear fitting adjustments in order to estimate

the temperature distribution in the active areas of the IGBT chip (Fig. 11b).



a) b)

Fig. 11. a) Presentation of the masked zones excluded for the raw temperature calculation b) Recomposed IGBT chip temperature distribution.

IV. Characterization of the TSEPs

In this section the calibration procedure and the measurement conditions are presented for each TSEP. For the TSEP calibration campaign, the power module is fixed on the cold plate. As it will be presented later in this section, the test procedure is defined in order to have a very low self-heating of the devices. The chip temperature is therefore modified by a thermo regulator (JULABO Presto instrument) which permits to control temperature of the power chips through the power module assembly. Due to convection and radiation heat transfers between the power module under test and its environment, and because the room temperature (about 25°C) is lower than the cold plate temperature (between 40°C to 180°C), the chip temperature is lower than the cold plate temperature. Thus the chip temperature has to be measured using the IR camera. The procedure presented in the previous section is used to evaluate the average temperature of the IGBT active part. This average temperature is considered as the chip temperature in the calibration curves.

In this section, for each TSEP, we will outline the dedicated electrical test circuit and the dependence of the TSEP with temperature. In order to study the variation of each parameter in the case a of single chip or two paralleled chips, three characterizations are made, one for IGBT T_1, one for IGBT T_2 and another for $T_1//T_2$.

A. *Measurement of the saturation voltage $V_{ce,sat}$*

This measurement is carried out feeding the IGBT chip with a low current supply I_m (Fig. 12). In the tests, I_m equals 50 mA if only one IGBT is tested and equals 100 mA in the case of two paralleled IGBTs. These values are chosen in order to have a linear characterization curve in all the temperature range. The gate-emitter voltage is 15V. Because the dissipated power is very low in the chip, the current injection can be continuous without any self-heating of the power device.

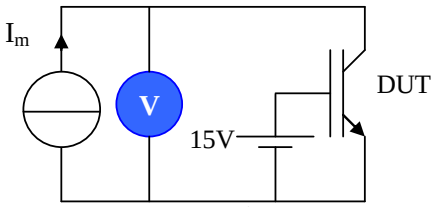


Fig. 12. Measurement of $V_{ce,sat}$ as TSEP.

Fig. 13 shows the variation of $V_{ce,sat}$ as a function of the temperature for T_1, T_2 and $T_1//T_2$. The characterization curves are linear with a slope of -2.3mV/°C.

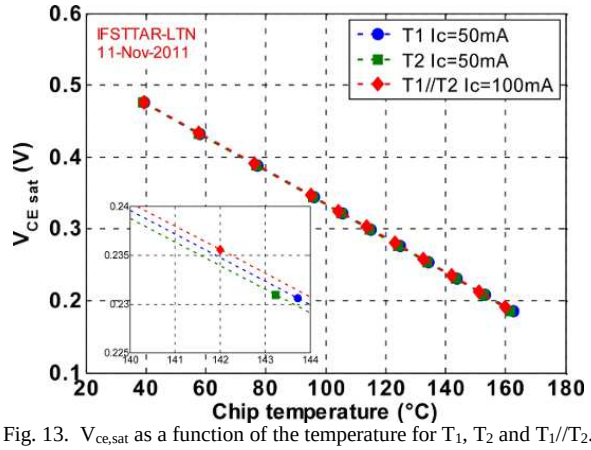


Fig. 13. $V_{ce,sat}$ as a function of the temperature for T_1, T_2 and $T_1//T_2$.

The measurements using T1 and T2 give very close results, the difference between each curve being about 1 mV. The temperature error is thus lower than 0.5°C. Linearity and low variation from one chip to another with the same reference make this TSEP very interesting for junction temperature measurements.

B. *Measurement of the gate-emitter voltage $V_{ge,I}$*

For this measurement, a voltage source E=10V feed the IGBT chip. The collector current I_c=5A is regulated acting on the gate voltage. When T_1 and T_2 are paralleled, the current I_c equals 10A. In order to limit the self-heating due to the power dissipation during this TSEP evaluation, the calibration procedure is made using a pulsed current. As shown in Fig. 14, I_c is measured by a 10mΩ shunt resistor R_{shunt} and regulated by a PI controller.

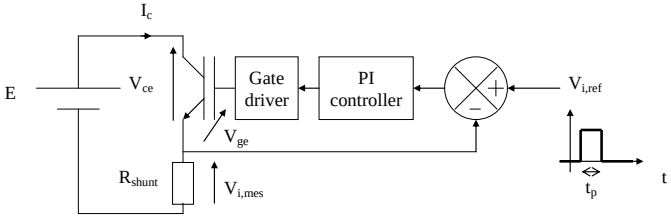


Fig. 14. Regulation of the collector current I_c.

Despite the use of a pulsed current, a measurement error can be made due to the self-heating of the device during the characterization. Fig. 15 shows the evolution of the gate-emitter voltage V_{ge} as a function of the time. Therefore an extrapolation method has to be used to decrease this

measurement error. Because of the low temperature variation during the measurement time, a linear interpolation as a function of the square root of time can be used [2,20]. $V_{ge,I}$ is then estimated calculating the value of the interpolation curve when $t=t_1$.

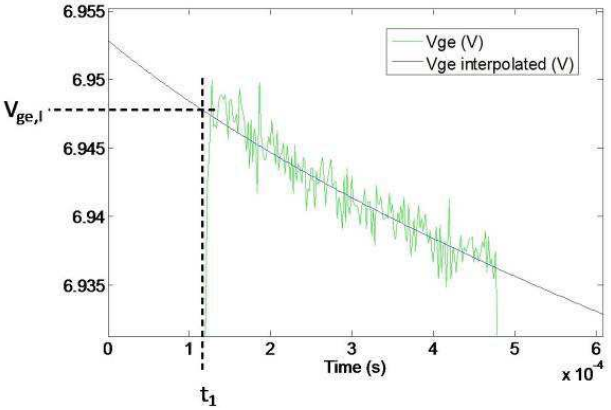


Fig. 15. Principle of the $V_{ge,I}$ measurement.

Fig. 16 presents $V_{ge,I}$ as a function of the chip temperature for T_1, T_2 and $T_1//T_2$. The sensitivity is about -6.5 mV/°C for lower temperatures and -8 mV/°C for higher temperatures. We can see that a voltage difference of about 100mV is obtained using T_1 instead of T_2. The measurement error is thus largely higher than 10°C. As a conclusion this TSEP varies from one chip to another under the same power module. An accurate temperature measurement needs therefore a calibration of each die.

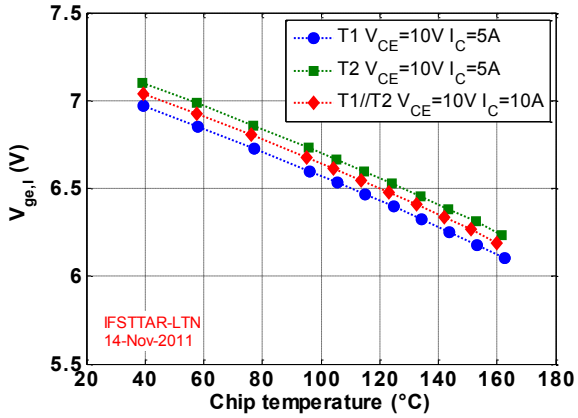


Fig. 16. $V_{ge,I}$ as a function of the temperature for T_1, T_2 and $T_1//T_2$.

C. *Measurement of the saturation current I_{css}*

The measurement of the saturation current I_{css} as a TSEP is made by feeding the IGBT by a voltage supply E=10V. During this measurement, the gate-emitter voltage is constant and equals 6.4V. In order to reduce the self-heating of the device, the IGBT is driven by a pulsed gate-emitter voltage. V_{ge} oscillations during the measurements are avoided by the use of a regulation loop (Fig. 17).

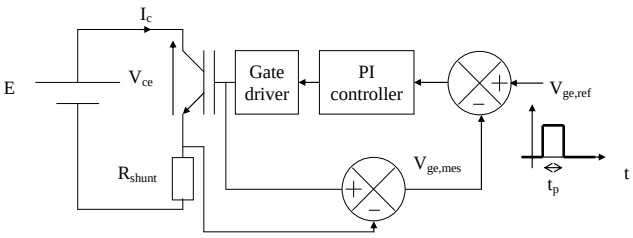


Fig. 17. Regulation of the gate-emitter voltage V_{ge}.

As for the measurement of $V_{ge,I}$, an interpolation process is needed in order to limit the temperature error due to the self-heating of the device. Fig. 18 gives the variation of I_{css} as a function of the temperature for T_1, T_2 and $T_1//T_2$.

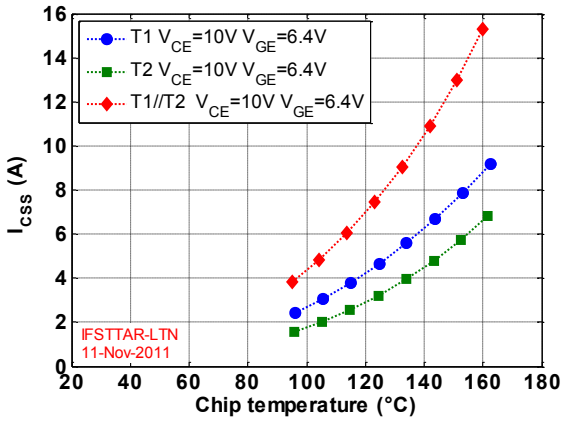


Fig. 18. I_{css} as a function of the temperature for T_1, T_2 and $T_1//T_2$.

This TSEP was not measured in the whole temperature range because the accuracy was poor for low temperatures. As for $V_{ge,I}$, this TSEP is different using T1 or T2. Logically, the value given in the case of T1//T2 is the sum of both values given using T1 and T2.

In the next section, the characterization results of the TSEPs will be used to achieve temperature measurements in the "working" power module. In this case the chips are crossed by a high direct current inducing a non negligible self-heating. The measured temperatures will be compared with referential temperatures provided by IR camera measurements. Then the relevance of each TSEP will be discussed.

V. Temperature Measurements Using Each TSEP

A. *Principle of the temperature measurements*

The chip temperature measurements are made in two steps. During the first step, called "dissipation step", the IGBT is fed by a high current source I_c inducing a self-heating of the device. The gate-emitter voltage equals 15V (the IGBT is in saturation conditions). The dissipated power P is calculated multiplying the collector current value I_c and the collector-emitter voltage value V_{ce}. The second step, called measurement step, begins when the steady state is reached. During this step the device temperature is measured using one of the three presented TSEPs. For this measurement, the electrical circuits depicted in the previous section are used.

The temperature of the cooling fluid is 30°C. This temperature is chosen in order to work with a temperature higher than the room temperature and thus to prevent any condensation process in the tested power module. It is also chosen in order to work with a relatively low cooling temperature allowing for a high dissipation level in the IGBT chips (maximum junction temperature 150°C). Fig. 19 summarizes the measurement process. As shown in this figure, a short dead time is introduced between the two steps. However the junction temperature decreases during this dead time and during the measurement step. An interpolation procedure is thus needed in order to obtain the temperature value at the end of the dissipation step.

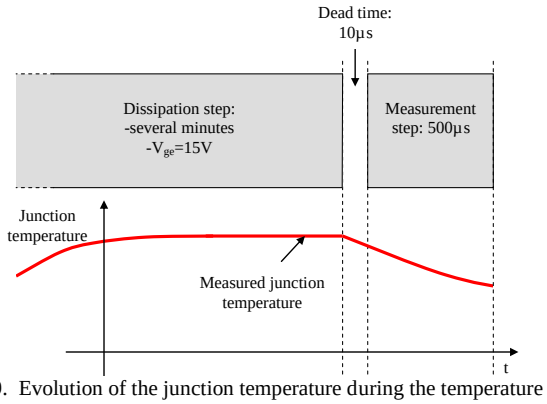


Fig. 19. Evolution of the junction temperature during the temperature measurement process.

During the dissipation step, the temperature of the IGBT chip is not homogeneous. For example, Fig. 20 shows in the left an IR image of a dissipating IGBT (in saturation conditions). In the right is traced the temperature along the measure line which shows the large variation of the chip temperature (>30°C). We can see that in the case of dissipation in saturation region, the ribbons are hotter than the IGBT chip due to the high current density value over 100A/mm². A TSEP giving a global temperature value, the comparison with the actual temperature is thus difficult. In the following paragraphs, we have chosen to compare the temperature given by each TSEP with the mean chip surface temperature measured with the technique presented in section III.

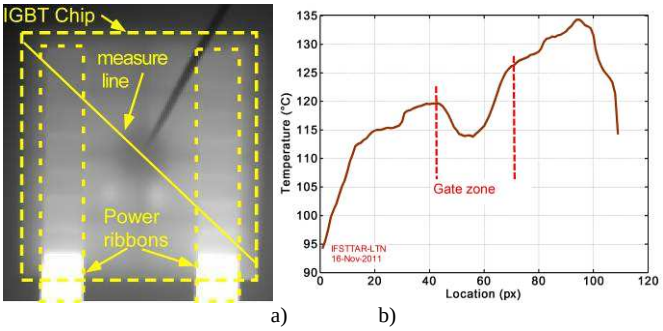


Fig. 20. Temperature distribution on a dissipating IGBT (a) and temperature along the measure line (b).

B. *Temperature measurements using IGBT T_1*

Table II presents a comparison between the temperatures obtained with each TSEP (T_{TSEP}) and the mean temperature obtained by IR measurements (T_{meanIR}). The studied chip is T_1. Three different power levels are used: one close to 45W, a second close to 70W and another close to 95W. The last column represents the difference between T_{TSEP} and T_{meanIR}. The T_{TSEP} value obtained with I_{css} and P close to 45W has not to be taken into account because the measured temperature is not in the range of the calibration curve (Fig. 18).

All TSEPs give temperature values in good agreement with the mean temperature obtained with IR measurements. Surprisingly, $V_{ce,sat}$, which is the most used TSEP, gives the results that have the largest differences. On the other hand, $V_{ge,I}$ and I_{css} are very representative of the mean chip temperature with errors respectively lower than 1°C and 0.5°C.

TABLE II
TEMPERATURE MEASUREMENTS WITH T_1

TSEP	P (W)	T_{TSEP} (°C)	T_{meanIR} (°C)	Error IR / TSEP (°C)
$V_{ce,sat}$	45.8	71.0	69.8	1.2
$V_{ge,I}$	46.3	71.5	71.0	0.5
I_{css}	46.3	74.2	71.1	3.1
$V_{ce,sat}$	70.7	100.1	98.1	2.0
$V_{ge,I}$	70.6	99.2	98.6	0.6
I_{css}	70.7	98.8	98.5	0.3
$V_{ce,sat}$	95.1	125.2	123.8	1.4
$V_{ge,I}$	95.0	124.8	123.9	0.9
I_{css}	95.1	124.1	123.8	0.3

C. *Temperature measurements using IGBT T_2*

Table III shows the results using T_2 instead of T_1. The results are very close to these presented with T_1. In fact, $V_{ge,I}$ and I_{css} give results very close to the mean IR temperature. The use of $V_{ce,sat}$ seems to be better than for T_1 but we can see that the measurement error can reach values higher than 1°C.

TABLE III
TEMPERATURE MEASUREMENTS WITH T_2

TSEP	P (W)	T_{TSEP} (°C)	T_{meanIR} (°C)	Error IR / TSEP (°C)
$V_{ce,sat}$	45.3	74.4	73.9	0.5
$V_{ge,I}$	44.9	74.7	74.1	0.6
I_{css}	45.1	77.0	74.1	2.8
$V_{ce,sat}$	69.4	101.9	100.5	1.4
$V_{ge,I}$	69.0	101.2	100.7	0.4
I_{css}	69.7	101.1	100.8	0.3
$V_{ce,sat}$	94.0	127.6	127.0	0.6
$V_{ge,I}$	94.2	128.0	127.3	0.7
I_{css}	93.7	127.5	127.3	0.1

D. *Temperature measurements using IGBT T1//T2*

As said above (section II), a torque adjustment of the power module mounting conditions permits to modify the thermal resistance between each IGBT chip and the cooling system. So, each IGBT chip temperature can be adjusted in order to perform a TSEP evaluation in different thermal conditions. For example, if this torque is lower in the left hand side of the module, the temperature of IGBT T_1 is

higher than this of IGBT T_2. In a commercial power module, these conditions can be representative of a temperature difference between paralleled chips due to packaging defaults (solder voids for example) or to an unequal current repartition.

Table IV proposes a comparison between results obtained with infrared temperature measurements and with TSEPs in the case of two parallel-connected IGBT chips controlled with the same gate drive circuit. Three cases are studied. In the first one, the mean temperatures of both IGBT are about the same. In the second, IGBT T_1 is hotter than IGBT T_2. In the last case, IGBT T_2 is hotter than IGBT T_1. For each case, the total power level is relatively low (≈40W) and the variation of the junction temperature is obtained modifying the temperature of the coolant liquid. The power dissipation is low in order to have a very low temperature variation on each IGBT chip surface (about 5°C). The last column represents the difference between T_{TSEP} and T_{meanIR} (which is the mean value of the mean temperature of T_1 $T_{meanIR\ T1}$ and the mean temperature of T_2 $T_{meanIR\ T2}$). Next to this column is given the difference between $T_{meanIR\ T1}$ and $T_{meanIR\ T2}$. The results given by I_{css} at lower temperatures have not to be taken into account because this TSEP was not calibrated for this temperature level (Fig. 18).

TABLE IV
TEMPERATURE MEASUREMENTS WITH T_1//T_2

Test conditions	TSEP	T_{TSEP} (°C)	$T_{mean\ IR}$ T_1 (°C)	$T_{mean\ IR}$ T_2 (°C)	T_{meanIR} (°C)	$T_{meaniR\ T1}$ – $T_{meanIR\ T2}$ (°C)	Error IR/TSEP (°C)
T_1 and T_2 with the same temperature	$V_{ce,sat}$	76.5	75.8	75.6	75.7	0.2	0.8
	$V_{ge,I}$	78.3	77.0	76.9	76.9	0.1	1.4
	I_{css}	78.6	76.4	76.4	76.4	0.0	2.2
	$V_{ce,sat}$	108.5	108.3	107.3	107.8	1.0	0.7
	$V_{ge,I}$	108.9	108.3	107.2	107.7	1.1	1.2
	I_{css}	107.8	108.3	107.3	107.8	1.0	-0.1
	$V_{ce,sat}$	129.6	129.9	128.2	129.1	1.7	0.5
	$V_{ge,I}$	129.9	129.9	128.2	129.0	1.7	0.8
	I_{css}	128.9	129.9	128.2	129.0	1.7	-0.1
T_1 hotter than T_2	$V_{ce,sat}$	93.6	98.7	84.4	91.6	14.3	2.1
	$V_{ge,I}$	95.0	98.9	84.7	91.8	14.2	3.2
	I_{css}	94.4	99.2	85.1	92.1	14.1	2.3
	$V_{ce,sat}$	113.0	117.9	104.9	111.4	13.0	1.6
	$V_{ge,I}$	113.8	117.6	104.7	111.1	12.9	2.7
	I_{css}	112.6	117.6	104.6	111.1	13.0	1.5
	$V_{ce,sat}$	132.4	136.9	125.4	131.2	11.5	1.2
	$V_{ge,I}$	133.0	136.7	125.2	130.9	11.5	2.0
	I_{css}	132.0	136.8	125.3	131.0	11.5	0.9
T_2 hotter than T_1	$V_{ce,sat}$	90.9	81.6	96.2	88.9	-14.6	2.0
	$V_{ge,I}$	88.7	80.7	95.3	88.0	-14.6	0.8
	I_{css}	87.8	80.7	95.4	88.0	-14.7	-0.3
	$V_{ce,sat}$	108.4	101.3	112.7	107.0	-11.4	1.4
	$V_{ge,I}$	107.6	101.3	112.7	107.0	-11.4	0.6
	I_{css}	106.2	101.4	112.8	107.1	-11.4	-0.9
	$V_{ce,sat}$	132.9	124.8	138.4	131.6	-13.6	1.3
	$V_{ge,I}$	131.9	124.9	138.7	131.8	-13.8	0.1
	I_{css}	131.3	125.2	139.2	132.2	-14.0	-0.9

If both IGBTs have approximately the same temperature, the three indirect temperature measurements with TSEPs conduct to a good correlation with the mean IR temperature measurement (T_{meanIR}). Especially the results given by I_{css} are very good, the temperature difference between T_{meanIR} and T_{TSEP} being lower than 0.1°C. $V_{ce,sat}$ also gives very good results, the temperature difference being lower than 1°C. The worst results are given by $V_{ge,I}$. The measurement error in this last case could be due to the extrapolation method because the threshold voltage of each IGBT being different, the current repartition is totally different in each IGBT and the self-heating (during calibration) or the cooling (during temperature measurements) of each semiconductor device are completely different. In the case of I_{css} the same problem exists but this TSEP is the sum of the saturation currents of T_1 and T_2. The cooling and self-heating of the device being linear phenomena, the results seem to be not affected by this problem.

If IGBTs temperatures are not equal, the chip temperature evaluation by TSEPs may conduct to significant errors over 3°C in comparison with the mean IR temperatures. If T_1 is hotter than T_2, I_{css} is still the best TSEP but the temperature difference between all TSEPs and IR measurements is largely higher than in the previous case. On the contrary, $V_{ge,I}$ seems to be the best TSEP if IGBT T_2 is hotter than IGBT T_1. Results given by $V_{ce,sat}$ do not depend on the temperature repartition between both IGBTs.

E. Discussion

$V_{ce,sat}$ is the most used TSEP in the case of thermal characterizations of power packages. All experimental results presented in this paper and in [8] show that the temperature obtained with this TSEP is always higher than the mean chip surface temperature. The temperature difference between T_{TSEP} and T_{meanIR} is low in the case of a homogeneous temperature distribution (Table IV – T_1 and T_2 with the same temperature) and higher if the temperature difference is larger (Table II, Table III and Table IV in other cases).

Table IV also shows that the temperature difference values (last column) given if T_1 is hotter than T_2 or if T_2 is hotter than T_1 are approximately the same. For example, if T_{meanIR}≈90°C, the temperature difference equals 2.1°C when $T_{meanIR\ T1}$>$T_{meanIR\ T2}$ and 2.0°C when $T_{meanIR\ T2}$>$T_{meanIR\ T1}$. If T_{meanIR}≈110°C, the temperature difference is respectively 1.6°C and 1.4°C. If T_{meanIR}≈130°C, it is respectively 1.2°C and 1.3°C. Therefore the measurement with $V_{ce,sat}$ as TSEP depends on the temperature distribution but is not influenced by the temperature repartition between several IGBT chips. It is mainly due to the fact that this TSEP has a low variation from one chip to another with the same reference (Fig. 13). Because most power modules are made with several paralleled IGBT chips, this TSEP is very well suited for their thermal characterization.

The other TSEPs ($V_{ge,I}$ and I_{css}) are useful for the temperature measurements of single IGBT chips (Table II and Table III). But, as shown in Table IV, the thermal disequilibrium conditions (T_1 hotter than T_2 or T_2 hotter than T_1) conduct to a more or less good correlation between these TSEPs and IR temperature measurements. In the case of temperature disequilibrium between several chips, the temperature measurements give also good results but the reproducibility is not satisfactory. For example, using I_{css} as

TSEP and $T_{meanIR} \approx 110°C$, the difference between T_{TSEP} and $T_{mean,IR}$ is 1.5°C if $T_{meanIR\ T1} > T_{meanIR\ T2}$ and -0.9°C if $T_{meanIR\ T2} > T_{meanIR\ T1}$. These results are the consequences of two combined factors which are effective chips temperatures and TSEP characteristics differences of each IGBT (Fig. 16 and 18). In conclusion $V_{ge,I}$ and I_{css} can be used for the thermal characterization of power modules using only one chip per switch. In the case of paralleled power devices, their use induces large temperature measurement errors due to the lack of reproducibility.

VI. Conclusion

In this paper an experimental setup was first proposed in order to compare IGBT chip temperature measurements using three TSEPs and an IR camera. These measurements were carried out using only one IGBT or two paralleled IGBTs. The power dissipation was made in the saturation region of the semi-conductor devices (full conduction - V_{ge}=15V). The IR measurement procedure was made with caution in order to obtain the more accurate chip temperature measurements: the emissivity of the black paint was estimated and a numerical procedure was developed in order to extract the real temperature of the active part of the device excluding the electrical connections, the inactive areas, and also the artifacts due to radiative reflections.

With these experimental and numerical tools, a calibration campaign was first carried out. Results were obtained for each TSEP. Large differences were obtained between both IGBTs in the case of $V_{ge,I}$ and I_{css} due to the variation of the threshold voltage from one chip to another with the same reference. Finally a comparison between temperature measurements given by the TSEPs was presented, the IGBTs being in dissipation conditions. All TSEPs in all conditions give temperature results close to these provided by IR measurements. However I_{css} seems to give the best accordance in the case of using a single IGBT. If both IGBTs are paralleled, this TSEP and $V_{ge,I}$ give results depending on the temperature repartition between both chips because of the variation of these TSEPs from one chip to another. That is not the case for $V_{ce,sat}$ which is a more robust TSEP. Therefore this parameter seems to be the best for the thermal characterization of power modules with paralleled power devices.

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