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Anisotropic Deep Reactive Ion Etching without Aspect Ratio Dependence Etching for silicon power devices

Aurélie LECESTRE[1,3] , Pascal DUBREUIL[1,3], Sylvain NOBLECOURT[1,2], Josiane TASSELLI[1,3], Eric IMBERNON[1,3], Frédéric MORANCHO[1,2]

[1]CNRS, LAAS, 7 avenue du colonel Roche, BP 54200 F-31031 Toulouse Cedex4, France

[2]Univ de Toulouse, UPS, LAAS, F-31031 Toulouse, France

[3]Univ de Toulouse, LAAS, F-31031 Toulouse, France

We present the optimization of the critical etching step for the fabrication of silicon Deep Trench-SuperJunction (DT-SJ) Diodes in order to obtain breakdown voltages of 1200V. The influence of the technological parameters on electrical performances has been studied by simulations, showing the importance of trenches verticality and width [1-2]. The aim is to fabricate an array of trenches of 6 µm-width and 110µm-depth near to junction termination trenches of 80um width. The main challenge for etching deep trenches in silicon is high anisotropy with high aspect ratio: we studied the influence of DRIE passivation time on Critical Dimension loss [3]. ARDE effect (Aspect Ratio Dependent Etching) has been reduced by using a thermal silicon oxide mask: SiO_2 thicknesses have been determined in order to obtain the same depth whatever the trench aperture.

Critical points for deep trenches etching are: High Aspect Ratio (HAR), CD losses, low roughness surface of sidewalls (scalloping), narrowing on the trench top, Aspect Ratio Dependent Etching (ARDE).
First of all, an HAR around 20 has been obtained thanks to Bosch process including two cycles: an etching step with SF_6 followed by a passivation one with C_4F_8/O_2. This work is carried out with Alcatel - AMS4200 ICP (Inductively Coupled Plasma) DRIE equipment. In order to reduce CD loss, we have varied the passivation time/etching time ratio from 1.3 to 3. High anisotropy and low roughness surface have been achieved for a ratio of 1.75 (3.5s/2s). In these conditions, for trenches of 6µm-wide and 110µm-depth, the width difference between the top and the bottom of trenches is around 100nm and the scalloping is around 60nm (Fig. 1-a).

The second study has been carried on the ARDE effect. The aim is to obtain the same depth for two different widths. Indeed, for 80µm-trench the etch rate is two times faster than for a 6µm one. In order to reduce this etching rate difference, an oxide mask has been added only on the biggest aperture [4]. The influence of the oxide thickness on etching depth for various trench widths is reported on Fig. 2-a, for 25min and 65min etching times. Using a 1.6µm oxide, the depth gap between 6µm and 40µm apertures is 5µm, and the depth gap between 6µm and 80µm apertures is 20µm as illustrated on Fig.1-b for a 65min etching time.
Moreover, the oxide layer on top of trenches allows the reduction of some negative effects related to Bosch process such as roughness surface (scalloping) and narrowing of the trench top (Fig. 2-b). So, the scalloping depth is decreased until 40nm.

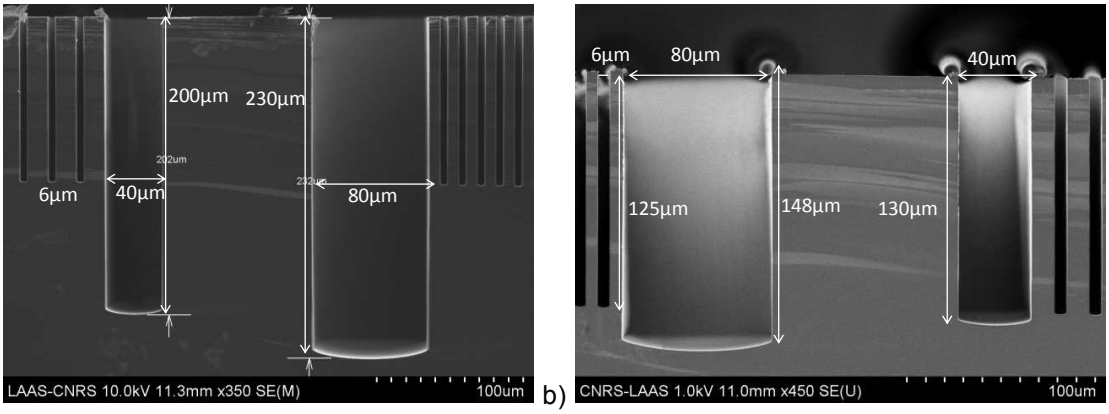

Fig.1: SEM images of trenches with high aspect ratio (HAR>28) for an etching time of 65min: a) with SiO_2 mask (300nm). b) with a selective SiO_2 mask (1.6µm) to reduce the ARDE.

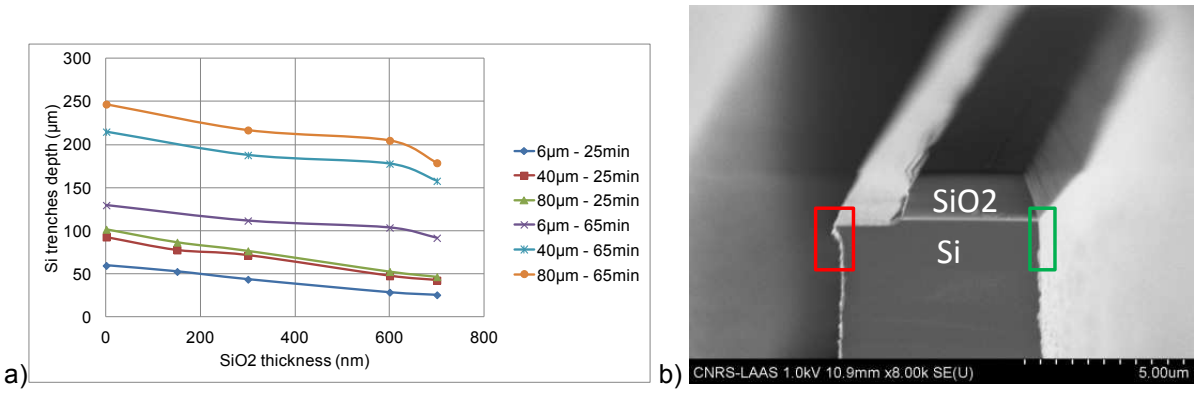

Fig.2: a) Si trenches depth variation versus SiO_2 mask thickness for two Si etching times (25min and 65min) and several trench widths (6µm, 40µm, 80µm).
b) Oxide effect on narrowing after photoresist elimination.

References
1. L.Théolier, K. Isoird, F. Morancho, J. Roig, H. Mahfoz-Kotb, M. Brunet, P. Dubreuil, EPE 2007.
2. L. Théolier, H. Mahfoz-Kotb, K. Isoird, F. Morancho, S. Assié-Souleille, and N. Mauran, IEEE Electron Device Letters, vol. 30, no. 6, June 2009, p687-689.
3. Y. Zhu, G. Yan, J. Fan, J. Zhou, X. Liu, Z. Li and Y. Wang, J. Micromech. Microeng. 15 (2005) 636–642.
4. D. Belharet, P.F. Calmon, P. Dubreuil, J. Tasselli, H. Granier, PESM2012, Plasma Etch and Strip in Microelectronics, 15-16 mars 2012, Grenoble.

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* *corresponding author e-mail: alecestr@laas.fr*