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Analysis and Optimization of Lateral Thin-Film Silicon-on-Insulator (SOI) PMOS Transistor with an NBL layer in the Drift Region

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Abstract

This paper analyses the experimental results of voltage capability ($V_{BR} > 120V$) and output characteristics of a new lateral power P-channel MOS transistors manufactured on a $0.18 \mu m$ SOI CMOS technology by means of TCAD numerical simulations. The proposed LDPMOS structure have an N-type buried layer (NBL) inserted in the P-well drift region with the purpose of increasing the RESURF effectiveness and improving the static characteristics (R_{on-sp}/V_{BR} trade-off) and the device switching performance. Some architecture modifications are also proposed in this paper to further improve the performance of fabricated transistors.

1. Introduction

Lateral double diffused MOS (LDMOS) transistor is the best suited power switch for integrated circuits thanks to its faster switching time [1] compared to bipolar transistor and its ease of integration with CMOS technology. P-channel LDMOS (LDPMOS) transistors are widely used as high side power devices since it reduces its gate drive circuitry. Associated with the N-channel (LDNMOS) counterpart, they are employed in level shifters in many applications such as motor drivers or display panels. Good specific on-state resistance / breakdown voltage (R_{on-sp}/V_{BR}) trade-off of LDNMOS [2] is possible thanks to the Reduced SURface Field (RESURF) principle, since substrate is grounded and drain forward biased. However, for LDPMOS, this principle is inhibited because drain and substrate are commonly biased to the same potential. Some designs were developed in order to overcome this issue. In Bulk and thick film SOI technology the vertical depletion is possible with the inclusion of N-type floating layers at the surface [3] or deep inside the active Silicon region [4]. The presence of the N-type floating layer associated with a field plate defines the double RESURF [5] which leads to competitive R_{on-sp}/V_{BR} trade-off. However, in thin-film SOI, the small active Silicon area reduces the possibility to define an N-type floating region without degrading the device R_{on-sp} . Consequently, only the effect of the field plate is possible and the doping concentration of the drift region which sustains the voltage has to be lowered, leading to an inevitable increase of R_{on-sp} . Adopting the fine CMOS process technology to the LDMOS process enables the shrinking of power devices and the possibility to use different design architectures and methodologies, such as the super-junction concept, to improve their switching performance [6]. In this work, the already proposed LDPMOS

design in thin-SOI technology with a controlled N-type buried layer (NBL) in the drift region obtained by means of high-energy Phosphorus and Boron multi-implantation sequence [6] has been fabricated to improve the $R_{\text{on-sp}}/V_{\text{BR}}$ trade-off of the conventional LDPMOS without any additional CMOS process steps. The experimental results are analysed in this paper, and some possible design modification are proposed by means of TCAD numerical simulations results [7].

2. LDPMOS structures description

Fig. 1 shows the schematic cross-section of a conventional LDPMOS and the proposed NBL-LDPMOS transistor, being both structures based upon a 0.18 μm smart power technology on thin-SOI substrate with a SOI layer (T_{SOI}) and buried oxide (T_{BOX}) thicknesses of 1.5 μm and 1 μm , respectively. An STI (Shallow Trench Isolation) oxidation is previously defined, partially or totally covering the drift region length (L_{LDD}). The same L_{LDD} of 8 μm for a total cell length of 11.5 μm is also considered. Other additional common design parameters defined in Fig. 1 are a channel oxide thickness (T_{ox}) of 7 nm, a Poly-gate length not covered by the STI (L_{PolyTox} of 2 μm) and covered by the STI (ΔL_{Poly} of 3.5 μm) and a STI thickness (T_{STI}) of 0.46 μm . The NBL layer, which is defined with the same P-well mask, could connect to the N-well diffusion, as observed in Fig. 1b.

The addition of an NBL deep inside the drift region supports a space-charge depletion region which highly increases the RESURF effectiveness, thus improving the V_{BR} . Then, an optimum NBL implanted dose has to be set in order to ensure fully depletion before breakdown, thus achieving the best reliability conditions with a compensated charge balance among N and P doping in the drift region. Since the drift depletion action is enhanced with the addition of the NBL layer, the P-well implanted dose can be further increased to maintain charge balance, which could lead to a reduction of the $R_{\text{on-sp}}$ value. Nevertheless, if an active Silicon area of only $T_{\text{SOI}} = 1.5 \mu\text{m}$ is considered, the NBL thickness (T_{NBL}) must be as small as possible in order to not excessively reduce the drift current path which could highly penalize the device $R_{\text{on-sp}}$ value [6]. As it can be inferred from the schematic of Fig. 1b, NBL is depleted by the combined action of substrate field-effect action, and the P-well/NBL junction. Then, the optimal NBL implanted charge must be appropriately chosen to compensate both depletion effects. An extensive comparative analysis of both LDPMOS structure can be found in [6].

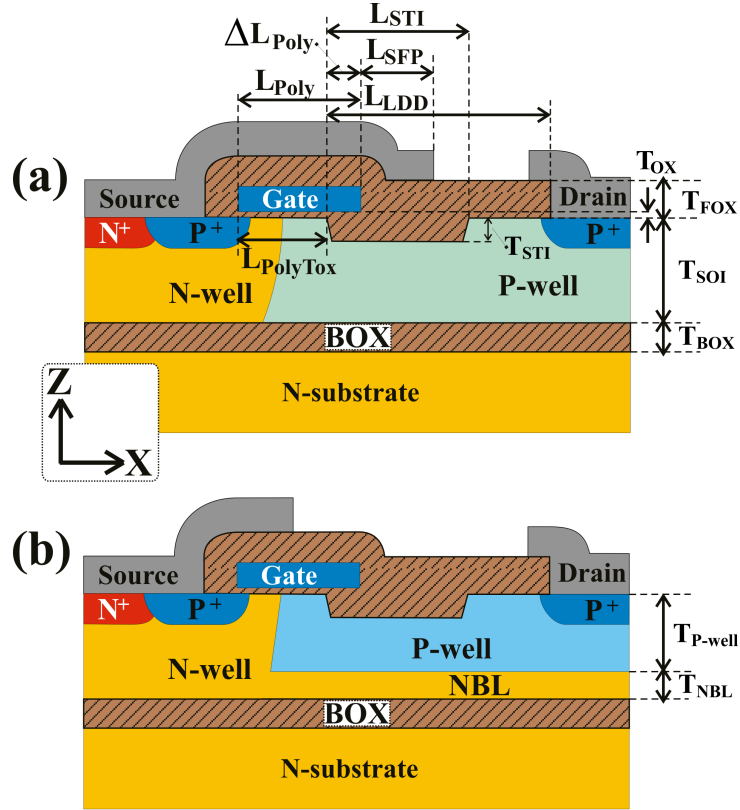


Fig. 1 Schematic cross-section of the (a) conventional LDPMOS and (b) proposed NBL-LDPMOS transistors

3. Analysis of the experimental results of NBL-LDPMOS

The complete set of measured electrical characteristics presented in this article are investigated using TCAD tools [7]. Fig. 2 shows the NBL-LDPMOS structure obtained with TCAD technological simulations, by using the same process flow of the fabricated transistors. As observed in Fig. 2, the N-well implantation window is not self-aligned with the Poly at the Source side (ΔN_{well} of $0.75 \mu\text{m}$) and the P-well implantation window is at a certain distance (ΔW_{ells}) from the N-well mask. Concretely, two different ΔW_{ells} values are taken into account: ΔW_{ells} of $0.75 \mu\text{m}$ and $1.25 \mu\text{m}$. Considering an $L_{PolyTox}$ of $2 \mu\text{m}$ (see Fig. 1), a ΔW_{ells} of $0.75 \mu\text{m}$ leads to a portion of the P-well mask overhanging the Gate region not covered by the STI. As a result, high BF_2 concentration is located at the gate oxide surface close to the STI (see Fig. 2a) due to the BF_2 low energy implantation used in the threshold voltage (V_{TH}) adjustment in complementary N-channel LDMOS. On the other hand, no presence of surface BF_2 concentration is resulted when ΔW_{ells} is $1.25 \mu\text{m}$ (see Fig. 2b). The resulting net doping profile through the Silicon active area at $X = 3.2 \mu\text{m}$ is illustrated in Fig. 3a ($\Delta W_{ells} = 0.75 \mu\text{m}$) and Fig. 3b ($\Delta W_{ells} = 1.25 \mu\text{m}$). The presence of the Phosphorus queue due to the NBL implantation is also observed in Fig. 3a ($\Delta W_{ells} = 0.75 \mu\text{m}$). However, no contact between the N-diffusion and the NBL layer is achieved in any case. The obtained doping profile in the drift region ($X = 8 \mu\text{m}$) in Fig. 3c shows higher Boron effective concentration ($Q_{P_{well}} = 1.2e12 \text{ cm}^{-2}$) as compared with the Phosphorus effective concentration ($Q_{NBL} = 6.2e11 \text{ cm}^{-2}$) of the NBL layer. The RESURF effectiveness analysis of the NBL layer have shown optimal voltage capability when

Q_{NBL} is similar to Q_{Pwell} [6]. Then, higher NBL dose implantation should be required for compensate the P-well dose implanted in the drift region.

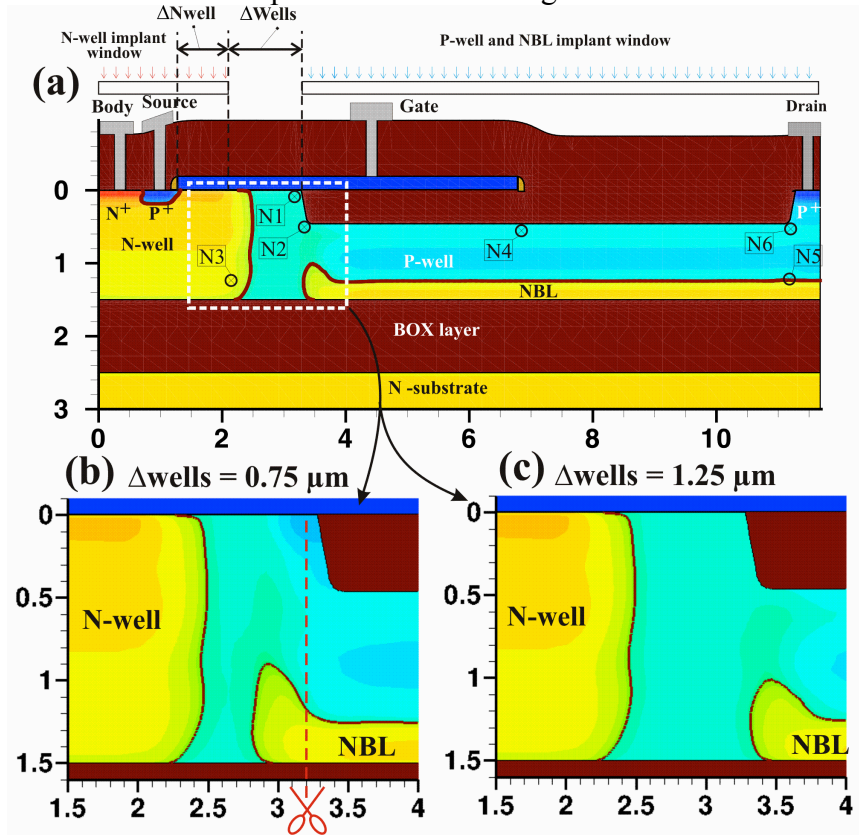


Fig. 2 Simulated cross section of the NBL-LDPMOS structure and the details of the resulted Poly-gate/STI corner region when a Δw_{ells} of $0.75 \mu m$ and $1.25 \mu m$ is used.

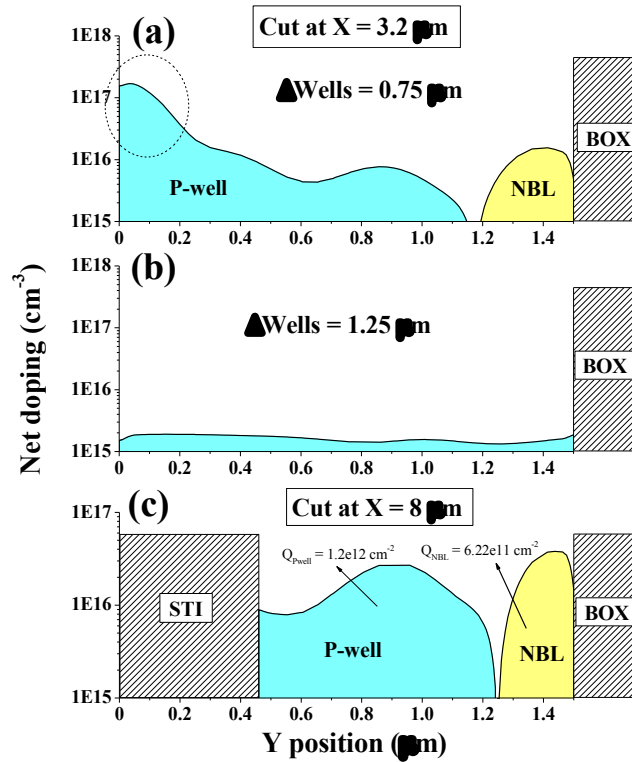


Fig. 3 Net doping profile through the active Silicon active area at Poly-Gate/STI corner region ($X = 3.2 \mu\text{m}$) for (a) ΔWells of $0.75 \mu\text{m}$ and (b) for $\Delta\text{Wells} = 1.25 \mu\text{m}$, and in the drift region covered by the STI ($X = 8 \mu\text{m}$).

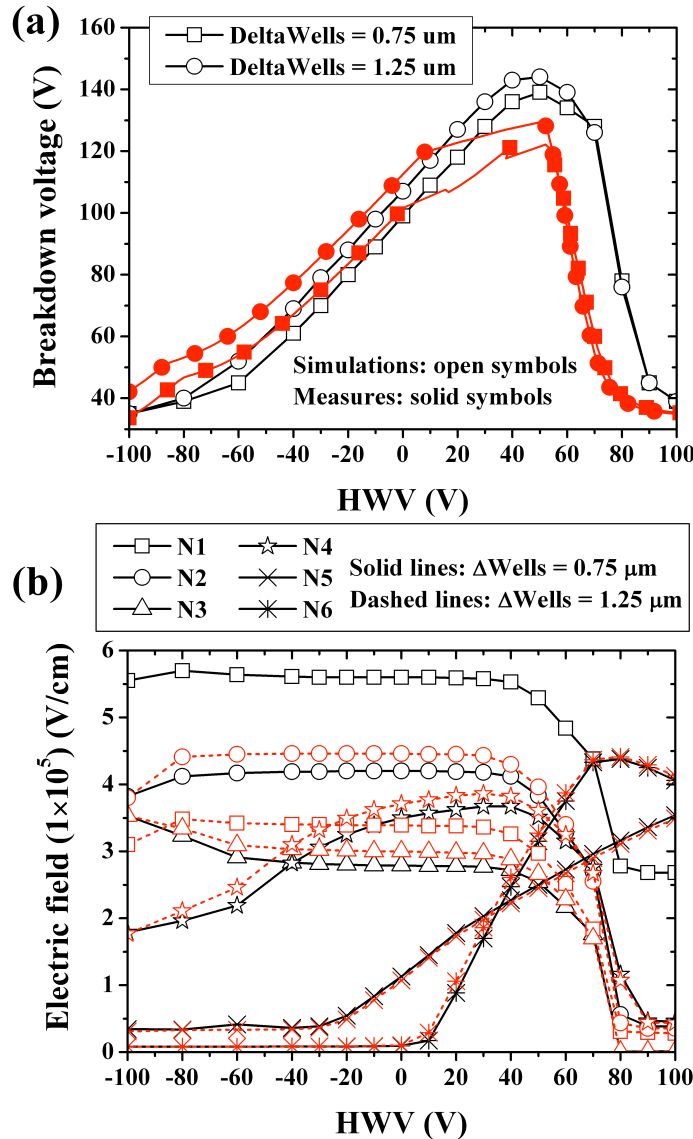


Fig. 4 (a) Comparison between measured and simulated V_{BR} vs HWV and (b) the electric field extracted in the most stressful nodes in NBL-LDPMOS structures with ΔWells of $0.75 \mu\text{m}$ and $1.25 \mu\text{m}$.

Device off-state characteristics

Fig. 4 shows the comparison between measurements and simulations of the breakdown voltage (V_{BR}) evolution as a function of the substrate (handle wafer) voltage (HWV). The reverse biased simulations and measurements at different HWV values are carried out with the Drain electrode grounded and both the Source and Gate electrodes biased with the same voltage. From Fig. 4a, it can be observed that the maximum V_{BR} value is obtained for high positive HWV, which clearly indicates that higher Phosphorus dose must be implanted in the NBL layer to compensate the P-well effective dose. The evolution of the electric field in the most stressful nodes illustrated in Fig. 2a is plotted in Fig. 4b as a function of HWV. According to this plot, the optimal HWV value leads to the best electric field distribution among the defined nodes. The difference between the structures with different ΔWells values is the much higher electric field located at

node N1, observed in the case of Δ Wells of 0.75 μm , especially at negative HWV values. This harmful electric field is clearly related with the high BF_2 concentration in the gate oxide surface close to the STI [8].

Device on-state characteristics

The comparison of the measured and simulated (non-isothermal) on-state characteristics illustrated in Fig. 4 shows (a) the voltage transfer characteristic and (b) the output characteristics of the NBL-LDPMOS structures. The direct biased simulations and measurements are carried out with the drain and HWV electrodes grounded and both the Source and Gate electrodes biased with the same voltage keeping a V_{gs} of -3V. Similar measured and simulated V_{TH} values in the range of -0.3 V (see Fig. 4a) are obtained in both structures. However, in spite of the good fit between measured and simulated output curves achieved for Δ Wells of 1.25 μm (Fig. 4b), high discrepancy is obtained for Δ Wells of 0.75 μm at linear region. As commented before, for Δ Wells of 0.75 μm , a certain portion of the P-well implantation mask is not covered by the STI, thus leading to an increment of Phosphorus (NBL queue) and BF_2 and Boron concentration close to the STI Source corner. Then, in spite of using a more accurate Monte Carlo implantation simulation, the drift between simulated and measured effective dose implanted due to possible mask misalignments or Si/SiO₂ species segregation will be more noticeable in the case of Δ Wells of 0.75 μm . Besides, from output curves results, high $|V_{\text{ds}}|$ saturation voltage are obtained in both cases, especially when Δ Wells of 1.25 μm , due to the low boron concentration in the Gate/STI region (see Fig. 3b), which highly increases the drift resistance, and thus the $R_{\text{on-sp}}$. Table I shows the final results of $R_{\text{on-sp}}/V_{\text{BR}}$ trade-off obtained in the NBL-LDPMOS experimental structures.

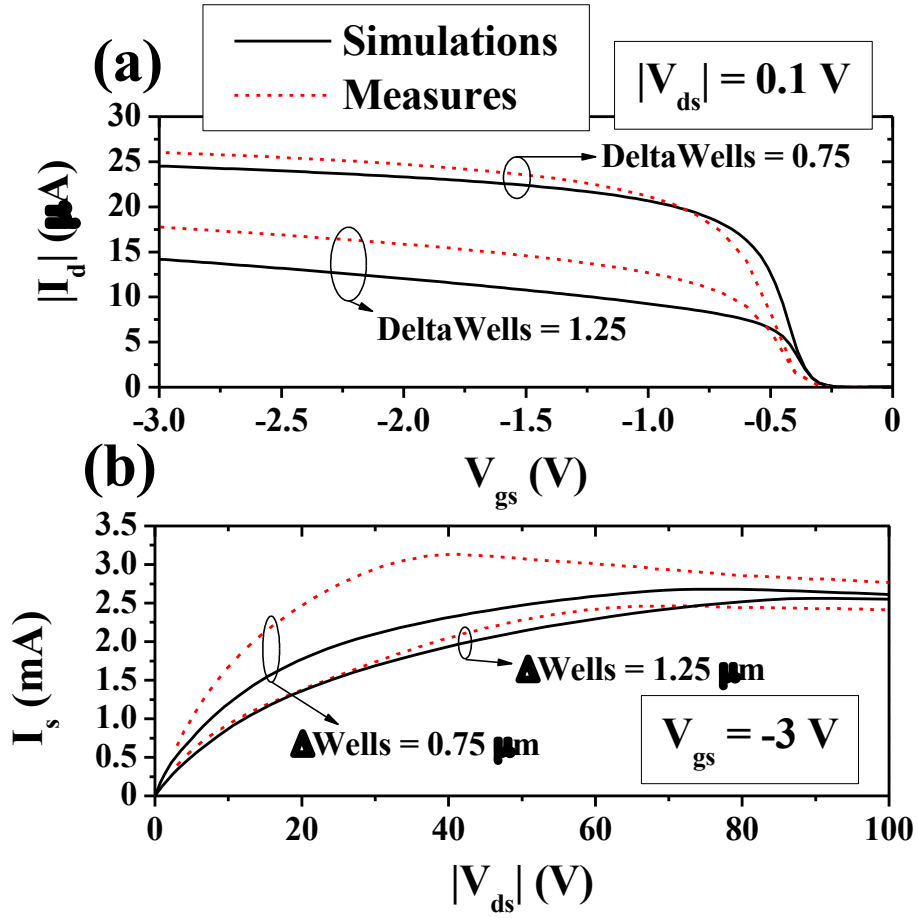


Fig. 5 Measured and simulated device on-state (a) $|I_d|$ - V_{gs} and (b) I_s - $|V_{ds}|$ characteristics in NBL-LDPMOS structures with Δ Wells of $0.75 \mu\text{m}$ and $1.25 \mu\text{m}$

NBL-LDPMOS description	V_{BR} (V)	R_{on-sp} ($\text{m}\Omega \times \text{cm}^2$)
Δ Wells = $0.75 \mu\text{m}$	122 @ HWV = 52 V	14.5 @ $V_{gs} = -3$ V
$L_{LDD} = 8 \mu\text{m}$, $L_{STI} = 8 \mu\text{m}$		12.4 @ $V_{gs} = -10$ V
Δ Wells = $1.25 \mu\text{m}$	130 @ HWV = 50 V	22.2 @ $V_{gs} = -3$ V
$L_{LDD} = 8 \mu\text{m}$, $L_{STI} = 8 \mu\text{m}$		16 @ $V_{gs} = -10$ V

Table 1 NBL-PLDMOS R_{on-sp}/V_{BR} characteristics.

4. NBL-LDPMOS structure optimization

In the NBL-LDPMOS structures from previous sections, the technological criteria used in their fabrication is linked with the CMOS technology, thus leading to some restrictions. Particularly, those concerning the multi-implantation sequences that define the N-well and the P-well/NBL regions. In order to improve the voltage capability of the NBL-LDPMOS transistors, better RESURF effectiveness must be achieved by providing similar $Q_{P\text{-well}}$ and Q_{NBL} in the drift region [6]. As a consequence, a new multi-implantation sequence of Boron and Phosphorus is defined in the drift region. Besides, the N-well multi-implantation sequence is also modified with the purpose to obtain a more uniform doping profile through the active SOI Silicon layer.

Some other structure modifications are taken into account: Different mask definition parameters such as Δ N-well of $0.25 \mu\text{m}$, Δ Wells values from $0.75 \mu\text{m}$ to $1.75 \mu\text{m}$ and a

$\Delta LPoly$ of 1.5 μm . Different thicknesses such as a T_{SOI} of 1.6 μm , a T_{STI} of 0.4 μm , and a T_{OX} of 20 nm which leads to a V_{TH} of -1.5 V. And finally different length definitions such as slightly shorter L_{LDD} of 7 μm and different L_{STI} partially (L_{STI} of 2 and 4) and totally covering the LDD (L_{STI} of 7 μm) have been also considered. The STI partially covering the LDD is defined with the purpose of not only improving the electric field distribution at breakdown and so the R_{on-sp}/V_{BR} trade-off [9], but also improving the device safe-operating-area (SOA) [2].

The proposed new NBL-LDPMOS structure with the STI partially covering ($L_{STI} = 4 \mu m$) is shown in Fig. 6a, while a detail of the new P-well/NBL drift doping profile is illustrated in Fig. 6b. In this case the NBL layer connects with the N-well diffusion thanks to the low ΔN -well and the $\Delta Wells$ of 0.75 μm used. For higher $\Delta Wells$ values, no NBL/N-well overlapping is achieved.

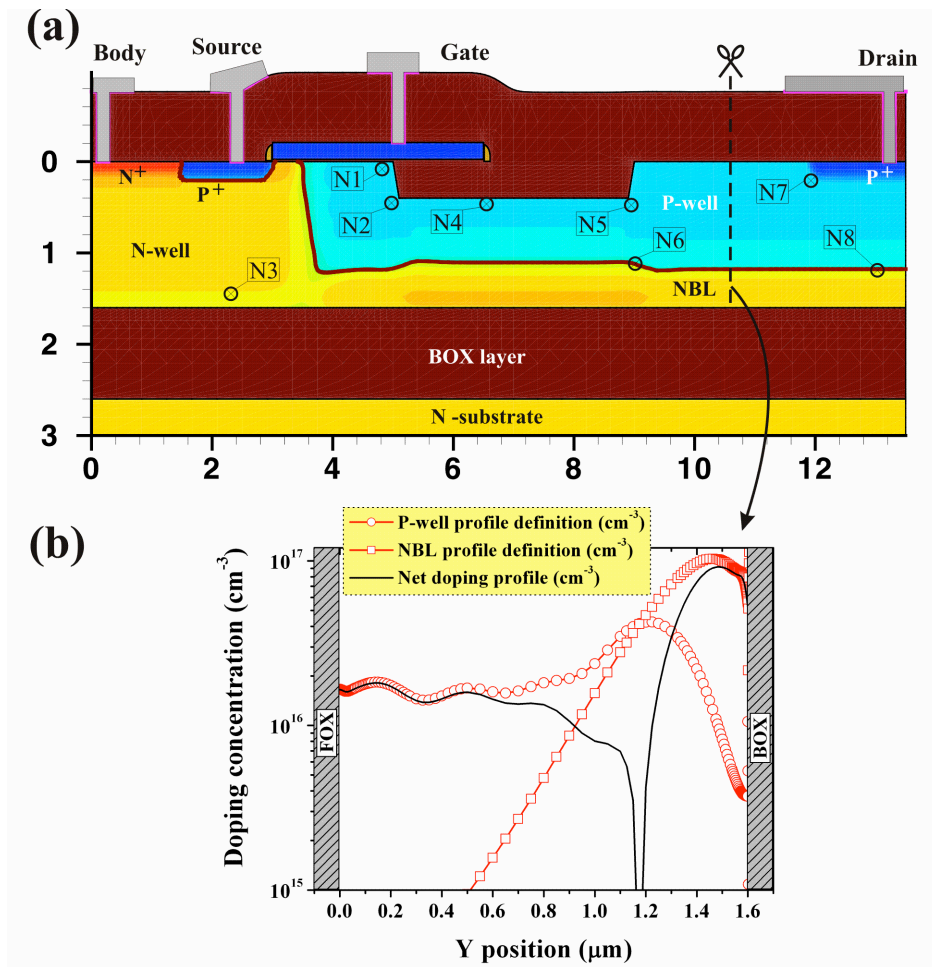


Fig. 6 (a) Schematic cross-section of the proposed new NBL-LDPMOS transistor and (b) the obtained doping profile throughout the SOI layer. Parameters used in this structure: ΔN -well of 0.25 μm , $\Delta Wells$ of 0.75 μm , L_{STI} of 4 μm and $\Delta LPoly$ of 1.5 μm .

R_{on-sp}/V_{BR} trade-off

Previous optimization of the NBL (Phosphorus) and P-well (Boron) implantation dose has been performed to obtain the best performance in terms of R_{on-sp}/V_{BR} trade-off for different L_{STI} values. Fig. 6b shows the doping profile in the LDD region not covered by the STI where the different doping peaks corresponds to a different implantation energy. However, the low energy Boron implantation peak will be located inside the STI block

in the region covered by the STI [9]. As a consequence, the longer the L_{STI} , the higher the P-well optimal implantation dose. Fig. 7 shows the simulation results of R_{on-sp}/V_{BR} trade-off as a function of P-well implantation dose increment in the new NBL-PLUDMOS structures with different L_{STI} values. Although the maximum V_{BR} value is achieved for L_{STI} values of 2 μm , optimal R_{on-sp}/V_{BR} trade-off is obtained in L_{STI} of 4 μm structures since high V_{BR} values is maintained for a wide P-well implantation dose. Moreover, the voltage capability is highly reduced when the STI completely covers the LDD region. Table 2 resume the final optimal results obtained in this plot.

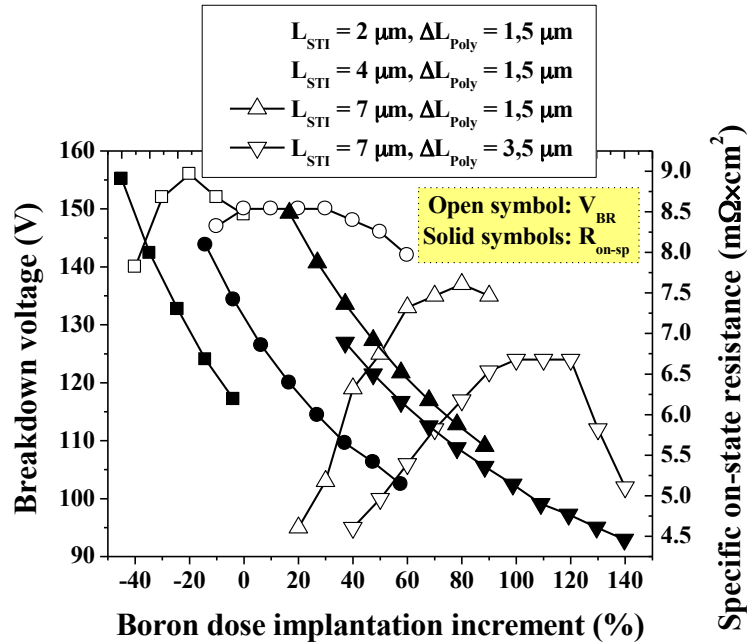


Fig. 7 R_{on-sp}/V_{BR} trade-off as a function of P-well dose percentage increment in the new NBL-LDPMOS structures with different L_{STI} and ΔL_{poly} definitions. The R_{on-sp} simulations are performed with $V_{gs} = -10$ V. Parameters used in this structure: ΔN -well of 0.25 μm , ΔW wells of 0.75 μm .

VBR vs HWV

The simulation evolution of the V_{BR} vs HWV of the best NBL-LDPMOS structures in terms of R_{on-sp}/V_{BR} trade-off from Fig. 7 have been compared in Fig. 8a. As observed in this figure, in spite of reducing the L_{LDD} , slightly higher V_{BR} can be reached in the proposed structure. Moreover, the highest V_{BR} peak and the best V_{BR} evolution vs HWV are obtained for L_{STI} of 2 μm and 4 μm , respectively. In Fig. 8b, the NBL-LDPMOS structure with L_{STI} of 4 μm is further analysed by means of the electric field evolution vs HWV in the most stressful nodes illustrated in Fig. 6a. A well distributed electric field in all nodes can be observed at a HWV range between 0 V and 30 V, where the V_{BR} maximum plateau is reached. At negative HWV, the NBL layer is easily depleted by the field-effect action of the substrate, thus avoiding the P-well depletion in the drift region. Besides, the N-well is vertically and laterally depleted by the substrate and the P-well layer. As a consequence, breakdown will be located at the gate/STI corner region (nodes N1 and N3) as observed in Fig. 8b. The same way than in fabricated NBL-LDPMOS transistors with Δ wells of 0.75 μm , high electric field also appears in N1 at negative HWV in spite of avoiding the BF2 surface implantation. Although the Poly-gate acts as a field plate by smoothing the surface electric field, the low ΔN -well of 0.25

μm used in these simulations has increased the P-well implantation window overhanging the Gate region. This fact leads to an increment of Boron concentration which is difficult to deplete specially at negative HWV values. Positive HWV leads to an opposite situation where P-well layer in the drift region easily depletes thanks to the combined action of the substrate field-effect and the NBL layer. Therefore, the breakdown region is shifted to the STI Drain corner, especially at nodes N8 (see Fig. 8b).

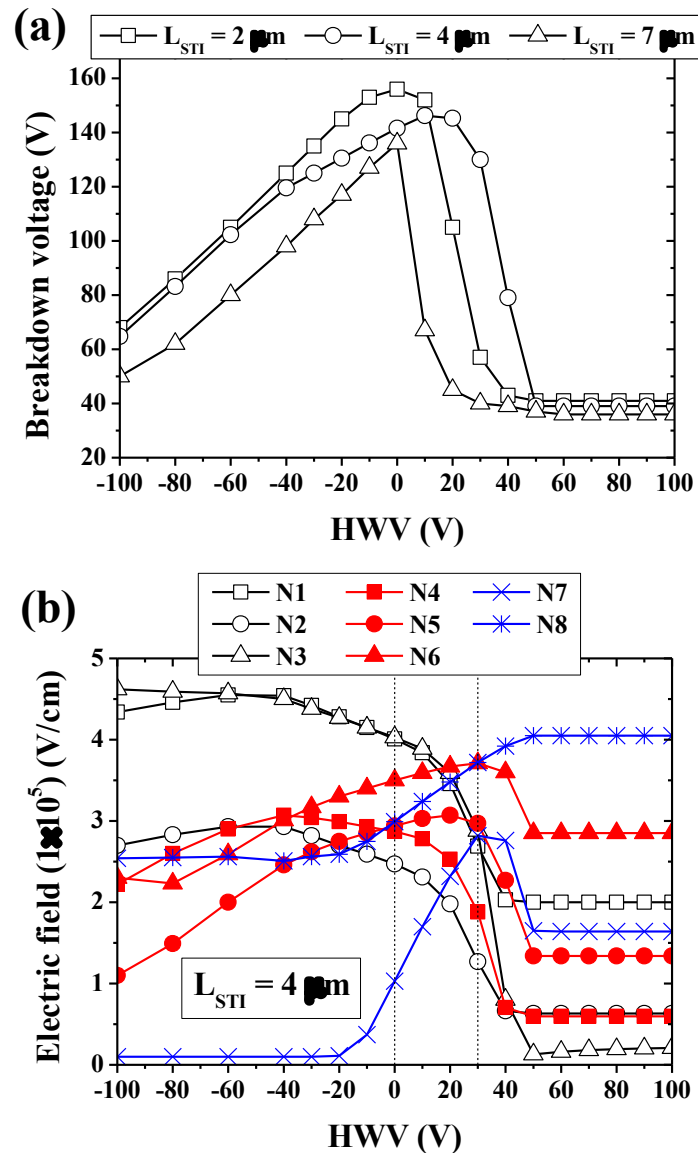


Fig. 8 (a) Simulated VBR vs HWV and (b) the electric field extracted in the most stressful nodes in the new NBL-LDPMOS structure with different L_{STI} values. Parameters used in this structure: ΔN -well of $0.25 \mu\text{m}$, ΔW ells of $0.75 \mu\text{m}$, $LLPoly$ of $1.5 \mu\text{m}$.

NBL-LDPMOS description	V_{BR} (V)	R_{on-sp} ($m\Omega \times cm^2$)
$\Delta Wells = 0.75 \mu m$ $L_{LDD} = 7 \mu m, L_{STI} = 2 \mu m$	156 @ HWV = 0 V	9.7 @ $V_{gs} = -3$ V 7.73 @ $V_{gs} = -10$ V
$\Delta Wells = 0.75 \mu m$ $L_{LDD} = 7 \mu m, L_{STI} = 4 \mu m$	146 @ HWV = 10 V	7.8 @ $V_{gs} = -3$ V 6.32 @ $V_{gs} = -10$ V
$\Delta Wells = 0.75 \mu m$ $L_{LDD} = 7 \mu m, L_{STI} = 7 \mu m$	136 @ HWV = 0	7.33 @ $V_{gs} = -3$ V 5.97 @ $V_{gs} = -10$ V

Table 2 new optimized NBL-PLDMOS R_{on-sp}/V_{BR} simulated characteristics.

SOA boundary

In this section, non-isothermal simulations of the output characteristics are performed to define the SOA boundary of the fabricated NBL-LDPMOS transistor (see Fig. 2) and the proposed new NBL-LDPMOS structure with L_{STI} of $4 \mu m$ (see Fig. 6). The same thermal resistances configuration extracted from simulations in Fig. 5 are used in this study. Hence, the simulated Drain voltage where the snap-back occurs is plotted at different applied effective ($V_{gs} - V_{TH}$) Gate voltages in Fig. 9. As a first glance, much better SOA boundary conditions can be obtained in the new optimal NBL-LDPMOS structure, especially at high Gate voltage values. On the other hand, the $\Delta Wells$ parameter increment has almost no repercussion in the voltage operation limit in both structures, as seen in Fig. 9. The high differences between both structures at high V_{gs} values is attributed not only due to better optimal NBL/P-well layer but also to the higher Phosphorus effective concentration in the N-well layer (Q_{N-well}) of the optimized NBL-LDPMOS structure which reduces the activation of parasitic bipolar transistor [10].

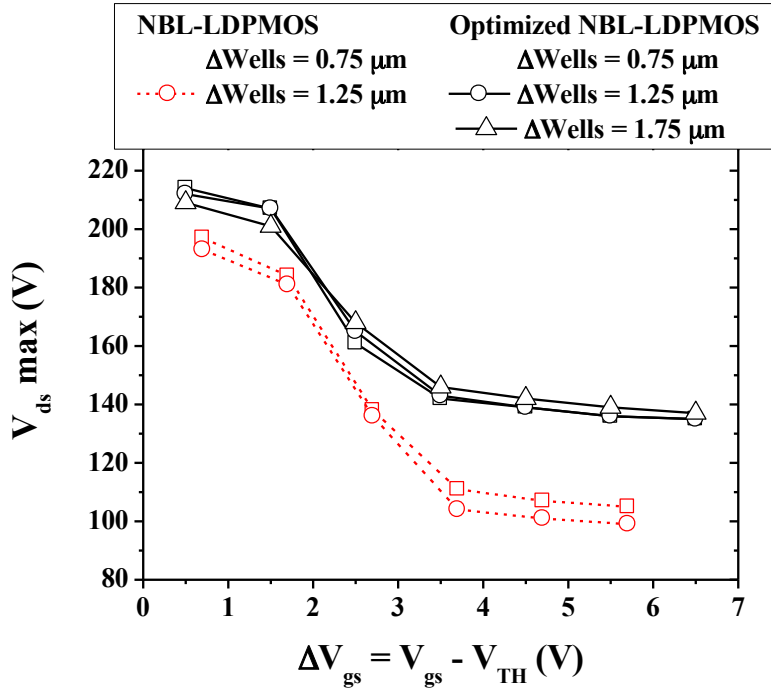


Fig. 9 SOA boundary comparison between fabricated NBL-LDPMOS transistors and proposed new NBL-LDPMOS structures considering different $\Delta Wells$ values.

5. Conclusions

The low RESURF effectiveness found in conventional P-channel LDMOS transistors requires the search of better optimal drift region design configurations such as the proposed LDPMOS with a NBL layer placed deep inside the SOI Silicon region. A significant improvement of the static performances can be achieved with the NBL-LDPMOS structure which assures competitive performances for switching applications. However, the technological process linked with the CMOS technology leads to some restrictions, especially those concerning the multi-implantation sequences that define the N-well and the P-well/NBL regions. Some design modification has been added in the structure to further optimize the performance by means of TCAD technological simulations, e.g. optimal NBL/P-well layers definition by changing the drift and body implantation sequence or definition of an STI partially covering the drift region.

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