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Direct power control of shunt active filter using high selectivity filter (HSF) under distorted or unbalanced conditions

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Abstract

This paper describes the design of a new configuration of direct power control (DPC) based on high selectivity filters (HSF) to achieve near-sinusoidal source current waveforms under different source voltage conditions. The proposed method uses the high selectivity filters instead of the classical extraction filters (low pass filters). The basic idea of the proposed DPC is to choose the best inverter voltage vector in order to minimize instantaneous active and reactive power errors using two hysteresis comparators. Their outputs associated with a switching table, control the active and reactive powers by selecting the optimal switching states of the inverter. Simulation results have proved excellent performance, and verify the validity of the proposed DPC scheme, which is much better than conventional DPC using low pass filters.

Keywords: Shunt active power filter (SAPF), Instantaneous powers, Direct power control (DPC), Switching table, High selectivity filter, Distorted or unbalanced conditions.

1. Introduction

Nowadays, the widespread use of non-linear loads leads to degradation of power quality of the electrical distribution systems due to generation of high harmonic currents. This results in multiple disagreements such as: increase of line losses, saturation of distribution transformers, and interference to adjacent communication systems. These effects can be worse in the case where the voltages and/or loads are unbalanced.

To improve the power quality, traditional solutions like passive LC filters have been widely used for a long time [1]. However, bulk passive components, series and parallel resonance and fixed compensation characteristics for fixed values of L and C are the main drawbacks of passive LC filters. In order to overcome all these problems simultaneously, various active power filters (APFs) have been developed in recent years [1, 2] due to the development in power converters and digital signal processors. The objective of these APFs is to reduce the voltage and current harmonic distortion [3]. The active power filter topology can be connected in series or parallel and combinations of both (unified power quality conditioners). Passive filters combined with active shunt and series are some typical (hybrid) configurations. Most of the industrial applications need current harmonic compensation, so the shunt active filter is more popular than over APFs [2, 4]. The shunt active power filter (SAPF) is based on the pulse width modulation voltage source inverter topology. Its basic function consists in the injection of currents which are load currents in opposite-phase, so that the load harmonic currents are cancelled [5, 6].

The performances of the SAPF depend on the voltage-source inverter design, the extraction method used to generate the reference signal (current or power), and the control method used to generate the filter current [5, 6]. In this context, the most popular control technique is usually based on current controller which forces the SAPF current to follow its reference [7–16].

A number of control methods have been reported in the literature such as proportional-integral (PI) control [7], hysteresis control [7], dead-beat control [8], repetitive-based control [9], adaptive control [10], and nonlinear control [11]. Also, there has been tremendous progress during the last decade in current control techniques for active power filters [12–16] including of a proportional controller plus multiple sinusoidal signal integrators [12], a PI controller plus a series of resonant controllers [13, 14], or vector PI (VPI) controllers [15]. This is due to the development of powerful and fast microprocessors. In recent work [16], the authors presented an advanced control strategy to improve the shunt active power filter compensation characteristics, which is based on a PI

plus VPI controllers. This control is capable of mitigating harmonic currents as well as reactive power without the demand of a load current measurement and harmonic detector [16].

In conventional control strategies applied for SAPF, these current controllers (usually proportional integral (PI) controllers) are employed for controlling output filter currents by an internal current control loop. However, the main drawbacks for this control method have resulted in steady-state errors, and their bandwidth limitation turns into a decrease of quality compensation [17]. Due to these facts, many new control strategies are being developed in recent decades. One of the most efficient is the direct power control (DPC), which presents the advantages of fast dynamic performance and simple control implementation, compared to other strategies.

The DPC method is derived from the direct torque control (DTC) used commonly in the high performance induction motor drive [18]. The DPC controls active and reactive powers, while the DTC is able to control torque and flux [19, 20]. The DPC strategy is based on the instantaneous reactive power theory introduced by Akagi et al. [21] and on the evaluation of the instantaneous active and reactive power error values. In DPC, there are no internal current control loops and no pulse width-modulation (PWM), because the converter switching states are appropriately selected by a switching table. This last is based on the instantaneous errors, between the commanded and estimated values of the active and reactive power, and the power-source voltage vector position (classic DPC [20]) or virtual flux vector position (VF-DPC [22]). First of all, DPC is a widely used control strategy for three-phase PWM rectifiers [20, 22]. In recent years, several authors have studied and analyzed the shunt active filter behavior under ideal conditions [23, 24]. Many control techniques have been used to improve the performance of the active filters in the situation of unbalanced conditions, but they most need to get synchronous rotation angle by using PLL and are difficult to implement. Besides the problems of harmonic distortion, there exist also low power factor and unbalanced load currents at the point of common coupling (PCC) due to the power delivered by the nonlinear loads [17, 25]. To overcome the limitations mentioned before, this paper presents a modified version of direct instantaneous power control strategy for three-phase shunt active power filter. In this novel scheme the high selectivity filters (HSF) have been utilized instead of the classical extraction filters (low pass filters). This allows to regulate directly the instantaneous active and reactive powers injected by the active filter, without any current control loops and phase locked loop involved. Moreover, this algorithm works effectively not only under balanced supply voltages, but also under distorted or unbalanced conditions.

The remainder of this paper is organized as follows. Section 2 presents a power circuit configuration of the SAPF and its modelization. In Section 3, the basic principles of proposed DPC are outlined. In Section 4, the

validity and effectiveness of the proposed SAPF is tested for several cases. Finally, the main contributions and significant results of this paper are summarized in the conclusion.

2. System description and modeling

2.1. SAPF topology

SAPF can suppress the current harmonics in the distribution networks by generating and injecting current harmonics (compensating current) at the PCC which have the same magnitude but opposite in phase of the current drawn by the nonlinear loads. Thus, the resulting total current drawn from the ac mains is sinusoidal. Fig. 1 shows the fundamental building block of the shunt APF. The SAPF system is made of a standard three-phase IGBT based voltage source inverter (VSI) bridge with the input ac inductors (L_f, R_f) and a dc bus capacitor (C) to obtain a self-supporting dc bus for an effective current control. A three-phase ac mains with line impedance (L_s, R_s) is feeding power to a three-phase diode bridge rectifier with a resistive-inductive load.

2.2. SAPF model

The considered SAPF is an ideal two-level three-phase inverter which is made of three branches ($a; b; c$) with two switches (1,2) each. The state of switch number n of branch x , S_{xn} , can be defined as $S_{xn} = 0$ if the switch is opened and $S_{xn} = 1$ if the switch is closed. For each branch x , a switching state S_x can be defined so that $S_x = 0$ if $S_{x1} = 1$ and $S_{x2} = 0$, and $S_x = 1$ if $S_{x1} = 0$ and $S_{x2} = 1$. The switching state of the inverter can then be defined by the triple ($S_a; S_b; S_c$).

The three-phase three-wire shunt active power filter is shown in Fig. 1. It is assumed that the three-phase source voltages are balanced as:

$$\begin{aligned} e_{sa}(t) &= E_m \sin(\omega t) \\ e_{sb}(t) &= E_m \sin\left(\omega t - \frac{2\pi}{3}\right) \\ e_{sc}(t) &= E_m \sin\left(\omega t - \frac{4\pi}{3}\right) \end{aligned} \quad (1)$$

where E_m and ω are the amplitude of the phase voltage and the angular frequency of the ac source, respectively.

Taking into account the absence of the zero sequence in the three-wire system and assuming that the ac supply voltages are balanced, the following assumptions are deduced:

$$\begin{aligned}
e_{sa} + e_{sb} + e_{sc} &= 0 \\
i_{sa} + i_{sb} + i_{sc} &= 0 \\
i_{La} + i_{Lb} + i_{Lc} &= 0 \\
i_{fa} + i_{fb} + i_{fc} &= 0
\end{aligned} \tag{2}$$

Fig. 2 shows the equivalent circuit of the SAPF system considering impedances in both the power grid and the load. In this system, the power grid is represented by the internal voltage e_s connected in series with an impedance Z_s . The load is represented by an equivalent circuit, where the current generator i_L represents the purely distorting current load. The active filter is composed of a voltage source v_f connected to the PCC by means of the filter impedance Z_f .

From the equivalent circuit of Fig. 2, considering the ideal case in which the power-grid impedance is negligible, that means $Z_s = 0$, the relationship between the supply, inverter voltages, and filter current is given as:

$$v_f = e_s - L_f \frac{di_f}{dt} - R_f i_f \tag{3}$$

Considering a symmetrical and balanced three-phase system and applying Kirchhoff laws to the three-phase equivalent circuit, the voltages supplied by the inverter are obtained in the three-phase coordinates:

$$\begin{aligned}
v_{fa} &= e_{sa} - L_f \frac{di_{fa}}{dt} - R_f i_{fa} = S_a v_{dc} - v_{nk} \\
v_{fb} &= e_{sb} - L_f \frac{di_{fb}}{dt} - R_f i_{fb} = S_b v_{dc} - v_{nk} \\
v_{fc} &= e_{sc} - L_f \frac{di_{fc}}{dt} - R_f i_{fc} = S_c v_{dc} - v_{nk} \\
C \frac{dv_{dc}}{dt} &= S_a i_{fa} + S_b i_{fb} + S_c i_{fc}
\end{aligned} \tag{4}$$

where v_{nk} : the voltage between the nodes n and k .

The summation of the three first equations of (4) gives:

$$\begin{aligned}
v_{fa} + v_{fb} + v_{fc} &= 0 \\
v_{nk} &= \frac{S_a + S_b + S_c}{3} v_{dc}
\end{aligned} \tag{5}$$

Substituting Eq. (5) to Eq. (4), the simplified differential equations can be obtained:

$$\begin{aligned}
\frac{di_{fa}}{dt} &= -\frac{R_f}{L_f}i_{fa} - \frac{v_{dc}}{L_f}\left(S_a - \frac{S_a + S_b + S_c}{3}\right) + \frac{1}{L_f}e_{sa} \\
\frac{di_{fb}}{dt} &= -\frac{R_f}{L_f}i_{fb} - \frac{v_{dc}}{L_f}\left(S_b - \frac{S_a + S_b + S_c}{3}\right) + \frac{1}{L_f}e_{sb} \\
\frac{di_{fc}}{dt} &= -\frac{R_f}{L_f}i_{fc} - \frac{v_{dc}}{L_f}\left(S_c - \frac{S_a + S_b + S_c}{3}\right) + \frac{1}{L_f}e_{sc} \\
\frac{dv_{dc}}{dt} &= \frac{1}{C}\left[S_a i_{fa} + S_b i_{fb} + S_c i_{fc}\right]
\end{aligned} \tag{6}$$

where i_{fa} , i_{fb} and i_{fc} are VSI compensating currents, and C is the capacitance of the VSI dc-side capacitor.

From the system of equations (4), a new control functions (u_a, u_b, u_c) can be defined as follows:

$$\begin{aligned}
u_a &= \left(S_a - \frac{S_a + S_b + S_c}{3}\right) \\
u_b &= \left(S_b - \frac{S_a + S_b + S_c}{3}\right) \\
u_c &= \left(S_c - \frac{S_a + S_b + S_c}{3}\right)
\end{aligned} \tag{7}$$

where the matrix of switching functions is expressed as:

$$u_{abc} = T_s S_{abc} \tag{8}$$

with

$$u_{abc} = [u_a, u_b, u_c]^T \quad S_{abc} = [S_a, S_b, S_c]^T$$

$$T_s = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \tag{9}$$

3. Proposed formulation for DPC using HSF

3.1. Instantaneous power references generation

The operation of the DPC technique is based on the control of instantaneous active (p) and reactive (q) powers, which are defined by the so-called instantaneous reactive power theory (IRPT) and the evaluation of the active and reactive instantaneous power error values [20, 21].

According to the instantaneous reactive power theory, the system voltage and the load current are transformed from $a - b - c$ coordinates into $\alpha - \beta$ coordinates by using the transformations (10) and (11) [26, 27]:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \quad (10)$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (11)$$

In fact, instantaneous real power (p) is equal to following equation:

$$p = v_{sa}i_{La} + v_{sb}i_{Lb} + v_{sc}i_{Lc} \quad (12)$$

The possibility of calculating them from $\alpha - \beta$ coordinates, as follows

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (13)$$

The instantaneous power p can be decomposed to $p = \bar{p} + \tilde{p}$, with \bar{p} the continuous component and \tilde{p} the harmonic component. The dc and ac components in these instantaneous active and reactive powers are due to fundamental and harmonic currents of the load, respectively. The power values of the dc components are filtered out by two low-pass filters (LPF) or high pass filters (HPF) as described in Fig. 3a. However, the instantaneous reactive power theory, in its standard form, does not allow to work under unbalanced conditions. In this paper, we propose a new method for the computation of instantaneous power reference based on HSFs (Fig. 3b), so the power reference can be calculated. By using the HSF filter, one can operate under any distorted and/or unbalanced conditions. On the other hand, the obtained instantaneous power terms in this method are the instantaneous active power reference p_{ref} and the instantaneous reactive power reference q_{ref} . The first one is generated based on the instantaneous active power ripples drawn by the nonlinear load, plus the power requirement of the dc bus voltage control loop to compensate switching loss, and the second one is equal to the instantaneous reactive power ripples consumed by the nonlinear load [23].

3.2. High selectivity filter

HSFs are used in the harmonic extraction instead of classical extraction filters (HPF or LPF). Hong-sock Song in [28, 29] had presented that the integration in the synchronous reference frame is defined by:

$$V_{xy}(t) = e^{j\omega t} \int e^{-j\omega t} U_{xy}(t) dt \quad (14)$$

where U_{xy} and V_{xy} are the instantaneous signals, respectively before and after integration in the synchronous reference frame. The equation (14) can be expressed by the following transfer function after Laplace transformation:

$$H(s) = \frac{V_{xy}(s)}{U_{xy}(s)} = \frac{s + j\omega}{s^2 + \omega^2} \quad (15)$$

We think of introducing a constant K in the transfer function $H(s)$, to obtain a HSF with a cut-off frequency ω_c . So the previous transfer function becomes:

$$H(s) = \frac{V_{xy}(s)}{U_{xy}(s)} = K \frac{(s + K) + j\omega_c}{(s + K)^2 + \omega_c^2} \quad (16)$$

By replacing $V_{xy}(s)$ by $X_{\alpha\beta}(s)$ and $U_{xy}(s)$ by $\hat{X}_{\alpha\beta}(s)$, the following expressions can be obtained:

$$\hat{X}_{\alpha}(s) = \frac{K(s + K)}{(s + K)^2 + \omega_c^2} X_{\alpha}(s) - \frac{K\omega_c}{(s + K)^2 + \omega_c^2} X_{\beta}(s) \quad (17)$$

$$\hat{X}_{\beta}(s) = -\frac{K\omega_c}{(s + K)^2 + \omega_c^2} X_{\alpha}(s) + \frac{K(s + K)}{(s + K)^2 + \omega_c^2} X_{\beta}(s) \quad (18)$$

where X can either be a current or a voltage.

The equations (17) and (18) can be expressed as follows:

$$\hat{X}_{\alpha}(s) = \frac{K}{s} [X_{\alpha}(s) - \hat{X}_{\alpha}(s)] - \frac{\omega_c}{s} \hat{X}_{\beta}(s) \quad (19)$$

$$\hat{X}_{\beta}(s) = \frac{K}{s} [X_{\beta}(s) - \hat{X}_{\beta}(s)] + \frac{\omega_c}{s} \hat{X}_{\alpha}(s) \quad (20)$$

The block diagram of the HSF for extracting the fundamental component $\hat{X}_{\alpha\beta}(s)$ from the signal $X_{\alpha\beta}(s)$ in the $\alpha - \beta$ reference frame is shown in Fig. 4.

3.3. Control Block Diagram

The block diagram of the proposed DPC technique is shown in Fig. 5. Initial voltages at the coupling point and load currents values are required in order to compute the initial active and reactive powers (p, q). The objective of the inner control loop is to minimize the errors between reference and actual values in each sampling step. This is done by selecting the appropriate inverter output voltage vector to push the state of the system towards the reference values. In this case the injected values of instantaneous active and reactive powers

are compared with their reference values and in proportion to the error signals the proper switching state is selected from a switching table.

The instantaneous active and reactive powers injected by the active filter are expressed:

$$p_{inj} = v_{sa}i_{fa} + v_{sb}i_{fb} + v_{sc}i_{fc} \quad (21)$$

$$q_{inj} = \frac{-(v_{sa}(i_{fb} - i_{fc}) + v_{sb}(i_{fc} - i_{fa}) + v_{sc}(i_{fa} - i_{fb}))}{\sqrt{3}} \quad (22)$$

Therefore, we define the active power error e_p and the reactive power error e_q as the difference between the power references p_{ref} , q_{ref} and the injected powers p_{inj} , q_{inj} respectively:

$$e_p = p_{ref} - p_{inj} \quad (23)$$

$$e_q = q_{ref} - q_{inj}$$

The error signals of the powers are compared in a two-level hysteresis comparators, which provide two digital signals (S_p and S_q), where:

$$\begin{cases} S_p = 1 & \text{if } p_{ref} - p_{inj} \geq h_p \\ S_p = 0 & \text{if } p_{ref} - p_{inj} \leq -h_p \end{cases} \quad (24)$$

$$\begin{cases} S_q = 1 & \text{if } q_{ref} - q_{inj} \geq h_q \\ S_q = 0 & \text{if } q_{ref} - q_{inj} \leq -h_q \end{cases} \quad (25)$$

Furthermore, the outputs S_p and S_q are used to access the voltage vector lookup table, along with the corresponding sector. The selection of the voltage vector depends on the location of the PCC voltage in the $\alpha - \beta$ plane. Therefore this plane is divided into 12 sectors as shown in Fig. 6. The table has as outputs the gating signals that generate the corresponding voltage vector. Table 1 shows the proper switching table to control the mentioned SAPF. In our work, all of the simulations tests are based on the switching table proposed in [23] (Table 1).

4. Simulation results

To confirm the effectiveness of the proposed DPC for SAPF, simulations are conducted in the environment of Matlab/Simulink. The data used for the simulation studies are given in Appendix B. For the two HSFs, we chose $K = 80$ to satisfy filter selectivity [29].

Simulation study has been carried out with non-linear load under three different source voltage conditions:

Case A: balanced sinusoidal source voltage.

Case B: unbalanced sinusoidal source voltage.

Case C: balanced distorted source voltage.

Source voltage and load current data along with total harmonic distortion (THD) for different cases are given in Table 2. Load currents are balanced and highly distorted. During uncompensated condition, source currents are same as load currents. Hence, uncompensated source currents are highly distorted and as a result the percentage of THD exceeds above IEEE-519 standard harmonic current limits.

Following information have been presented in the simulation results for the two control algorithms (DPC based LPF and DPC based HSF) under above mentioned cases:

- (i) Three-phase source voltages and frequency spectrum of source voltage of phase-a;
- (ii) Three-phase load currents and frequency spectrum of load current of phase-a;
- (iii) Three-phase source currents and frequency spectrum of source current of phase-a for the conventional DPC;
- (iv) Three-phase source currents and frequency spectrum of source current of phase-a for the proposed DPC;
- (v) The compensator current of phase-a and source voltage and source current of phase-a for the conventional DPC;
- (vi) The compensator current of phase-a and source voltage and source current of phase-a for the proposed DPC.

In order to plot source voltages and currents on the same scale, source voltages are scaled down by a factor of 10.

4.1. Balanced sinusoidal source voltage (case A)

For this case, balanced sinusoidal source voltage condition has been considered. Simulation results of case A are presented in Fig. 7 and summarized in Table 3. From Fig. 7(iii) it can be observed that sinusoidal source currents are achieved after compensation. The magnitude of compensated source current has reduced compared to that of uncompensated condition. The THD of source currents after compensation is restricted as per IEEE-519 standard harmonic current limit. Hence, harmonic mitigation is achieved effectively. Furthermore, the two control strategies converge to similar results under balanced sinusoidal source voltage conditions. Fig. 8 shows simulation results for the dc bus voltage. It can be seen that the voltage v_{dc} is stable and regulated around its reference.

4.2. Unbalanced sinusoidal source voltage (case B)

For the case B, source voltages are imbalance in magnitude. The magnitude of source voltage of phase-a is less than source voltage of phase-b and phase-c by 20%. Simulation results of case B are presented in Fig. 9 and tabulated in Table 4. The effect of unbalance in source voltage can be observed in load currents. It can be noted from the FFT spectrum of load current that third harmonic and its multiple are present in load current due to unbalance source voltages. It can be noted from Table 4 that the THD of the source current is restricted as per IEEE-519 standard only with proposed scheme. Therefore, source currents are very close to sinusoidal waveforms and are in phase with their corresponding source voltages, thus guaranteeing operation with a power factor very close to unity. It can be seen from these simulation results that the proposed DPC is much better than DPC using LPF.

4.3. Balanced distorted source voltage (case C)

For case C, source voltages are balanced and distorted. The seventh harmonic component with amplitude of 1/14 of the fundamental component is present in source voltage. For this case, both source voltage and load currents are harmonically contaminated. The performance of SAPF is shown in Fig.10 and summarized in Table 5. The harmonics are almost eliminated by the proposed control. It can be noted from Table 5 that only the proposed control is able to limit the THD as per IEEE-519 standard and power factor correction at the same time. However, source currents for conventional DPC are highly distorted due to the presence of the 3rd harmonic, caused by the 7th harmonic voltage component.

4.4. Analysis of results

Tables 3, 4 and 5 show the simulation results obtained using two different control techniques for three different cases, respectively. With reference to Tables 3, 4 and 5, following observations are made for compensated system under various source voltage conditions:

- (i) For case A, both control techniques give almost same results. Balanced and sinusoidal source currents, harmonic mitigation and reduction in rms value of source currents are achieved.
- (ii) For case B, balancing of source currents is provided by two methods. Among the two techniques, the proposed DPC is outperforms than the conventional one. Moreover, it is also capable to reduce the THD of compensated source current below IEEE-519 standard harmonic current limits.

(iii) For case C, it can be observed that only the proposed DPC guarantees near-sinusoidal source current waveforms.

From the above discussion, it is clear that the proposed control scheme satisfactorily compensates the distorted or unbalanced conditions in three phase system.

In order to demonstrate superiority and performance of the proposed control over the current control method introduced in [29], various comparative evaluation points can be noted under the same conditions. With regard to the control system shown in [29], it must be calculate that the current reference of SAPF is based on the use of HSF. In [29], analysis, simulation and experimental results were given to illustrate the harmonic cancellation using SAPF, and a modulated hysteresis current controller was used to fast track the current reference. A thorough investigation of the simulation results reported in both techniques reveals that the THD in the source currents cannot be brought down below 5% to satisfy the IEEE-519 standard. Therefore, the experimental results presented in [29] have conformed the effectiveness of using HSF in the SAPF control for various conditions. In addition, proposed DPC provides two advantages, compared to other approach. First, there are no internal SAPF current loops or modulator block because the inverter switching states are selected via a switching table. The second advantage is related to reduce the number of hysteresis comparators. Unfortunately, there have been few publications on DPC applied to the shunt active power filter [23, 24]; however, it considers the only in case of sinusoidal source voltages.

5. Conclusion

This paper has discussed a novel approach for DPC in order to control shunt active power filter. A comparative evaluation of two different control techniques for SAPF has been presented in this paper. A new proper active and reactive power reference generation strategy based on high selectivity filter have been developed. The performance of these control techniques has been evaluated under various source voltage conditions. Under ideal mains conditions, these two control techniques give almost similar results. Under unbalanced or non-sinusoidal source voltage conditions, only one proposed DPC technique shows excellent behaviour in terms of harmonic mitigation, balanced and sinusoidal source currents, and low THD of source currents. Simulation results have proven excellent performance of the proposed DPC scheme which is largely better than conventional DPC.

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Fig. 1. Configuration of the SAPF.

Fig. 2. Equivalent circuit of the SAPF.

Fig. 3. Block diagram of the power references generation: (a) conventional based LPF and (b) proposed based HSF.

Fig. 4. Block diagram of the HSF.

Fig. 5. Configuration of the proposed DPC.

Fig. 6. Sectors on stationary coordinates.

Fig. 7. Simulation results of case A: (i) three-phase source voltages and frequency spectrum of source voltage of phase-a, (ii) three-phase load currents and frequency spectrum of load current of phase-a, (iii) three-phase source currents and frequency spectrum of source current of phase-a for the conventional DPC, (iv) three-phase source

currents and frequency spectrum of source current of phase-a for the proposed DPC, (v) The compensator current of phase-a and source voltage and source current of phase-a for the conventional DPC, (vi) The compensator current of phase-a and source voltage and source current of phase-a for the proposed DPC.

Fig. 8. dc capacitor voltage.

Fig. 9. Simulation results of case B: (i) three-phase source voltages and frequency spectrum of source voltage of phase-a, (ii) three-phase load currents and frequency spectrum of load current of phase-a, (iii) three-phase source currents and frequency spectrum of source current of phase-a for the conventional DPC, (iv) three-phase source currents and frequency spectrum of source current of phase-a for the proposed DPC, (v) The compensator current of phase-a and source voltage and source current of phase-a for the conventional DPC, (vi)The compensator current of phase-a and source voltage and source current of phase-a for the proposed DPC.

Fig. 10. Simulation results of case C: (i) three-phase source voltages and frequency spectrum of source voltage of phase-a, (ii) three-phase load currents and frequency spectrum of load current of phase-a, (iii) three-phase source currents and frequency spectrum of source current of phase-a for the conventional DPC, (iv) three-phase source currents and frequency spectrum of source current of phase-a for the proposed DPC, (v) The compensator current of phase-a and source voltage and source current of phase-a for the conventional DPC, (vi) The compensator current of phase-a and source voltage and source current of phase-a for the proposed DPC.

Table 1

The switching table.

Table 2

Source voltage data and load current data along with THD under various source voltage conditions.

Table 3

Simulation results of two different control strategies under case A.

Table 4

Simulation results of two different control strategies under case B.

Table 5

Simulation results of two different control strategies under case C.

Appendix A. List of symbols

Appendix B. System parameters

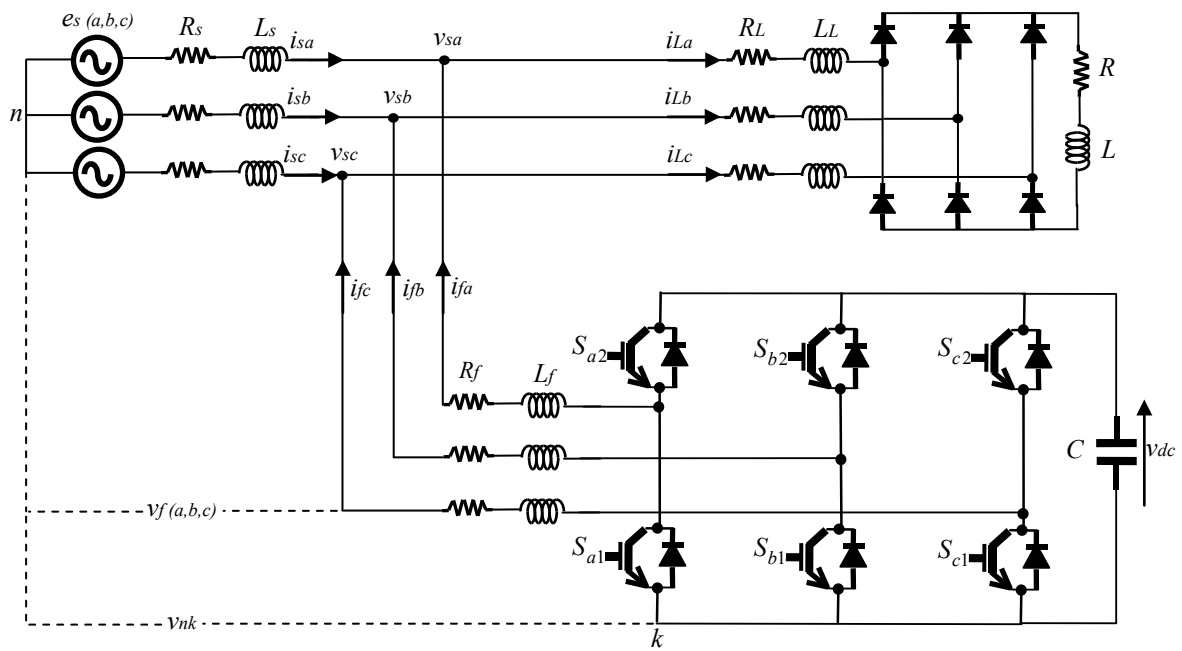


Fig. 1.

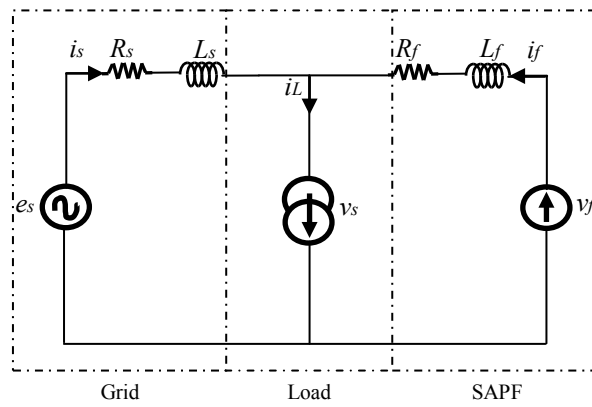


Fig. 2.

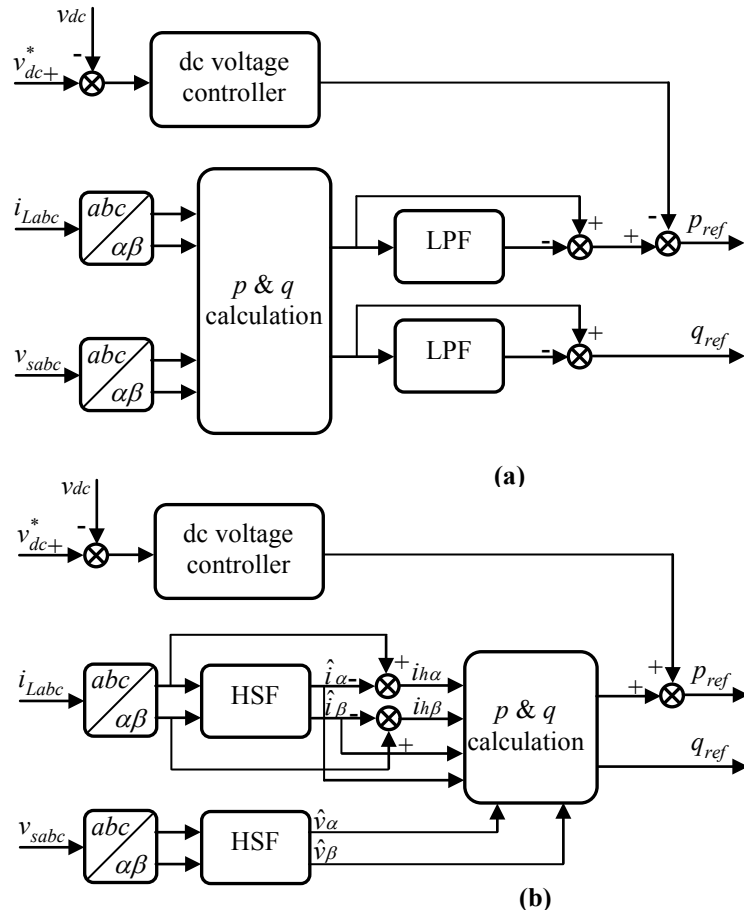


Fig. 3.

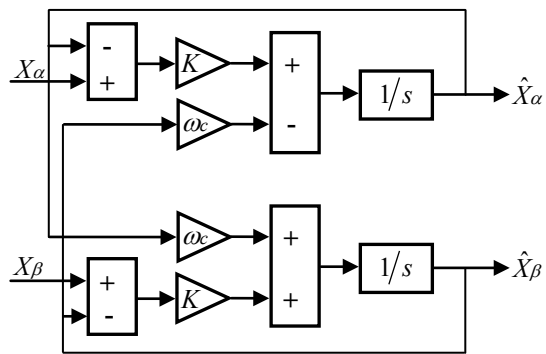


Fig. 4.

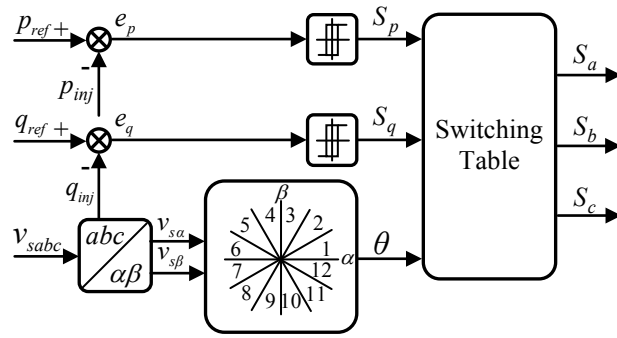


Fig. 5.

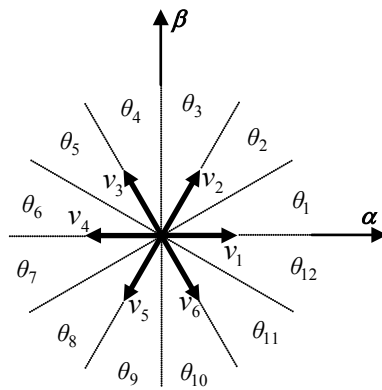


Fig. 6.

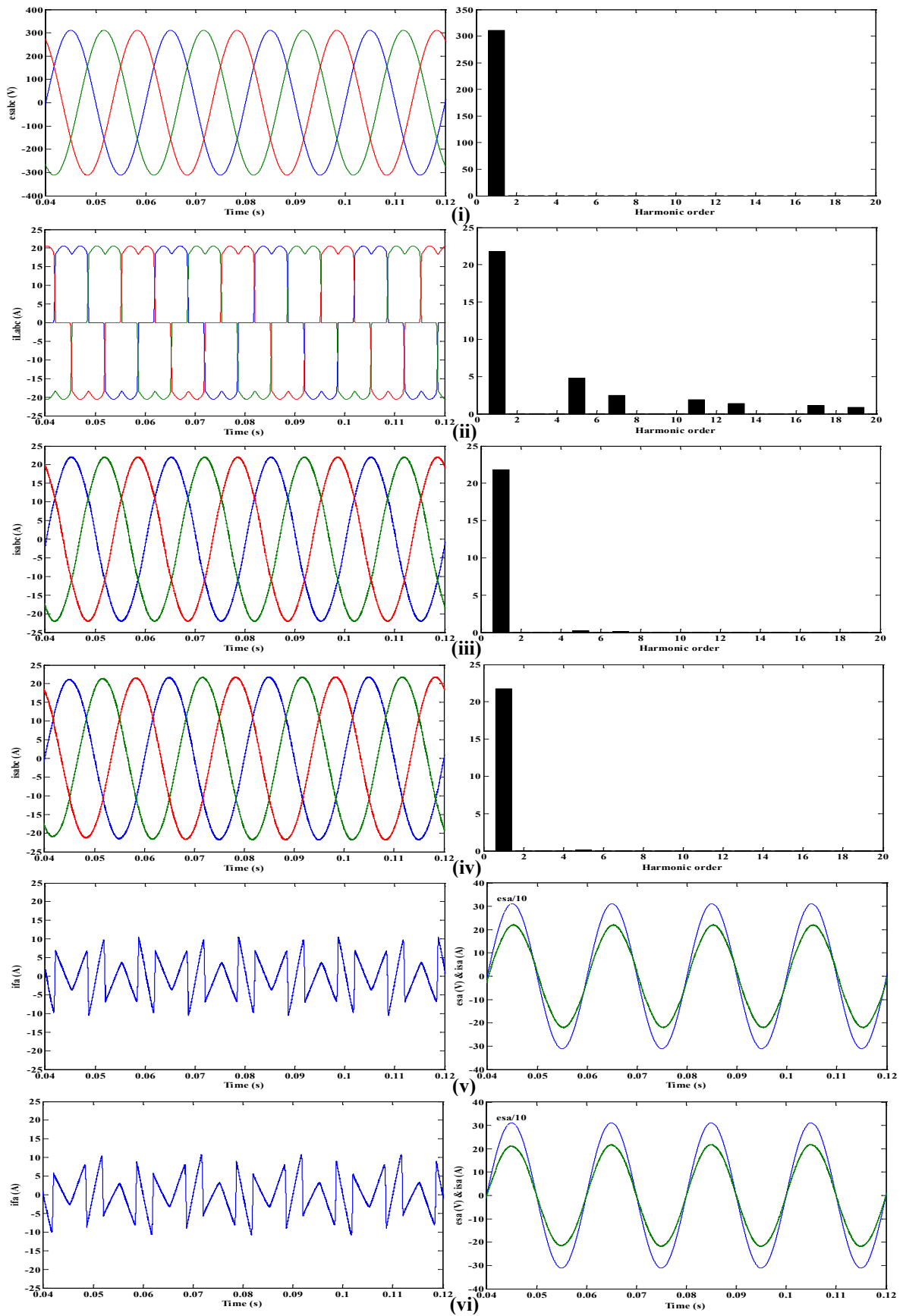


Fig. 7.

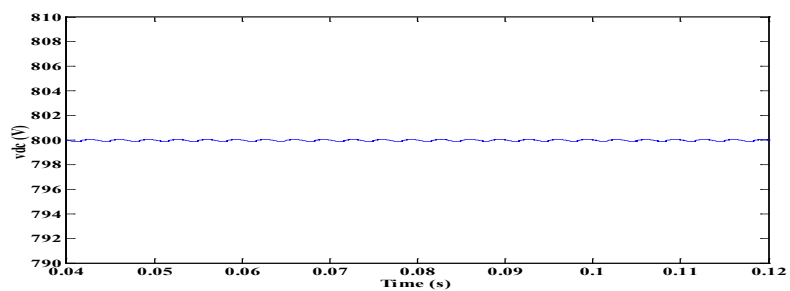


Fig. 8.

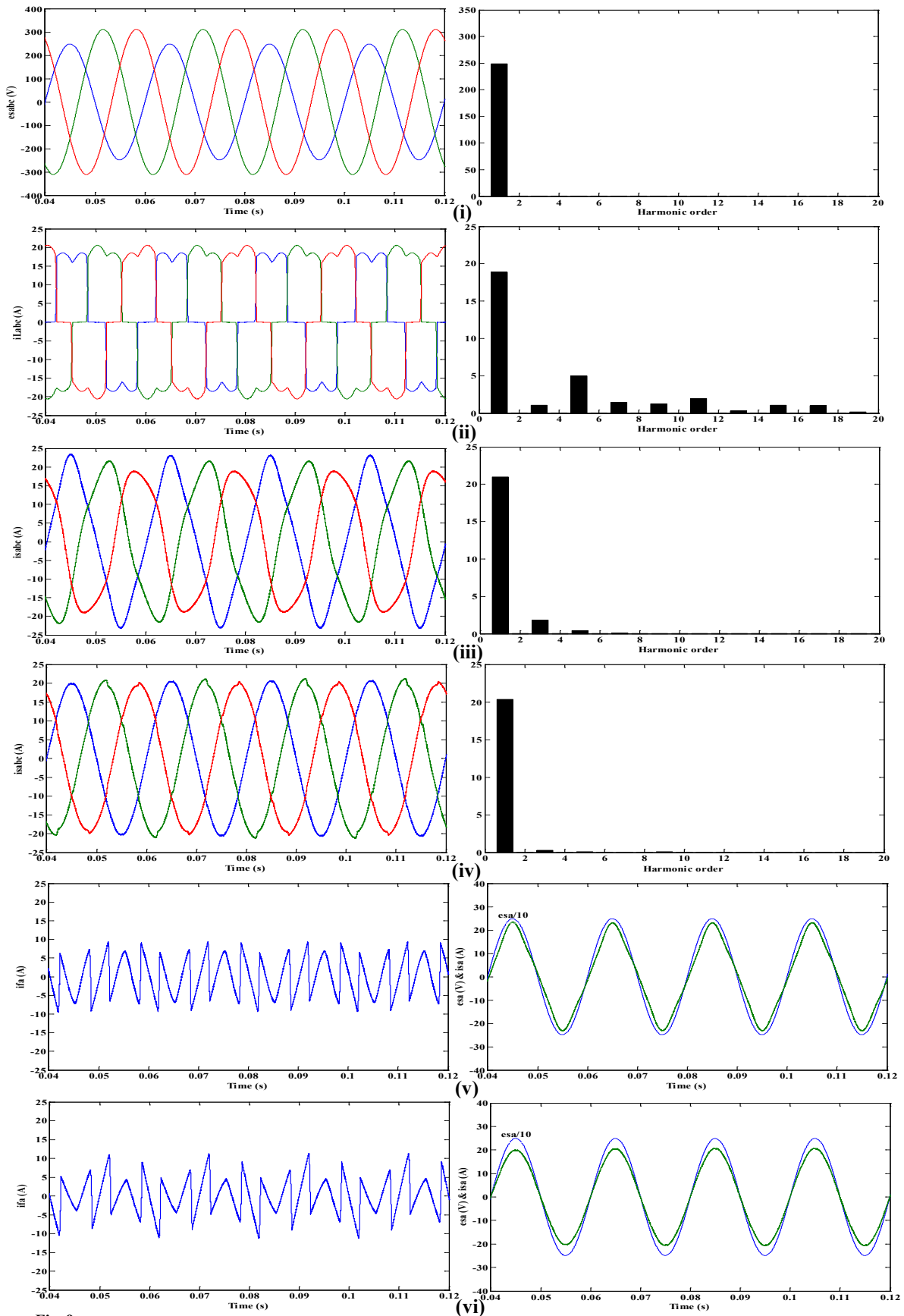


Fig. 9.

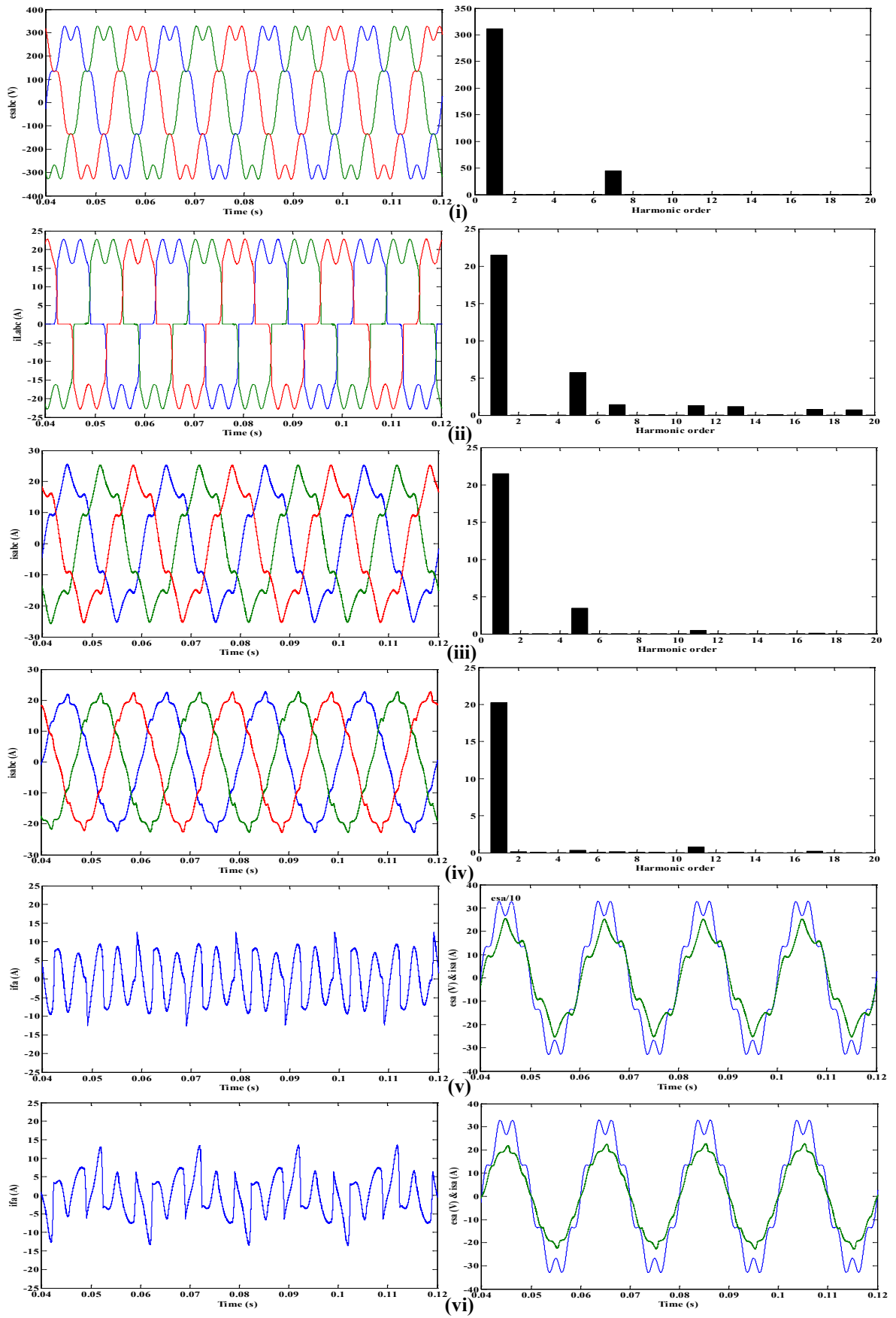


Fig. 10.

Table 1

S_p	S_q	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9	θ_{10}	θ_{11}	θ_{12}
1	0	110	110	010	010	011	011	001	001	101	101	100	100
	1	100	100	110	110	010	010	011	011	001	001	101	101
0	0	010	011	011	001	001	101	101	100	100	110	110	010
	1	001	101	101	100	100	110	110	010	010	011	011	001

Table 2

Case	Source voltage						Load current					
	e_{sa}		e_{sb}		e_{sc}		i_{La}		i_{Lb}		i_{Lc}	
	rms (V)	THD (%)	rms (V)	THD (%)	rms (V)	THD (%)	rms (A)	THD (%)	rms (A)	THD (%)	rms (A)	THD (%)
A	220	0	220	0	220	0	16.03	27.86	16.02	27.82	16.02	27.83
B	176	0	220	0	220	0	14.01	31.69	15.47	25.95	15.46	26.15
C	222.2	14.29	222.2	14.29	222.2	14.29	15.82	29.07	15.76	29.55	15.79	29.12

Table 3

Control strategies	Three-phase source currents						Three-phase compensator currents		
	i_{sa}		i_{sb}		i_{sc}		i_{fa}	i_{fb}	i_{fc}
	rms (A)	THD (%)	rms (A)	THD (%)	rms (A)	THD (%)	rms (A)	rms (A)	rms (A)
Conventional DPC	15.44	1.28	15.45	1.28	15.45	1.28	4.57	4.57	4.57
Proposed DPC	15.36	0.47	15.35	0.45	15.38	0.43	4.56	4.57	4.56

Table 4

Control strategies	Three-phase source currents						Three-phase compensator currents		
	i_{sa}		i_{sb}		i_{sc}		i_{fa}	i_{fb}	i_{fc}
	rms (A)	THD (%)	rms (A)	THD (%)	rms (A)	THD (%)	rms (A)	rms (A)	rms (A)
Conventional DPC	14.90	9	14.80	9.82	14.07	10.33	4.85	4.69	4.60
Proposed DPC	14.38	1.54	14.53	2.06	14.33	2.61	4.64	4.02	4.46

Table 5

Control strategies	Three-phase source currents						Three-phase compensator currents		
	i_{sa}		i_{sb}		i_{sc}		i_{fa}	i_{fb}	i_{fc}
	rms (A)	THD (%)	rms (A)	THD (%)	rms (A)	THD (%)	rms (A)	rms (A)	rms (A)
Conventional DPC	15.38	16.34	15.40	16.38	15.41	16.36	6.17	6.23	6.19
Proposed DPC	15.00	4.63	15.01	4.46	15.02	4.08	5.64	5.63	5.63

Appendix A. List of symbols

$e_s(a, b, c)$	source voltage of phase-a, phase-b and phase-c respectively
$v_s(a, b, c)$	voltage at the coupling point of phase-a, phase-b and phase-c respectively
$v_f(a, b, c)$	inverter output voltage of phase-a, phase-b and phase-c respectively
$i_s(a, b, c)$	source current of phase-a, phase-b and phase-c respectively
$i_L(a, b, c)$	load current of phase-a, phase-b and phase-c respectively
$i_f(a, b, c)$	compensator current of phase-a, phase-b and phase-c respectively
p_{inj}	instantaneous active power injected by the active filter
p_{ref}	instantaneous active power reference
q_{inj}	instantaneous reactive power injected by the active filter
q_{ref}	instantaneous reactive power reference
–	over the letter: continuous component
~	over the letter: harmonic component
<i>Subscripts</i>	
α	α component in $\alpha - \beta$ coordinates system
β	β component in $\alpha - \beta$ coordinates system
nh	nth harmonic component

Appendix B. System parameters

Source voltage	220 V (rms value)
Source impedance	$R_s = 0.25 \text{ m}\Omega$, $L_s = 19.4 \text{ }\mu\text{H}$
Source frequency	50 Hz
Load ac impedance	$R_L = 1.2 \text{ m}\Omega$, $L_L = 0.3 \text{ mH}$
SAPF dc reference voltage & C capacitor	$v_{dc}^* = 800\text{V}$, $C = 8.8\text{mF}$
SAPF resistance & inductance	$R_f = 5 \text{ m}\Omega$, $L_f = 3 \text{ mH}$
Non-linear load parameters	$R = 26 \text{ }\Omega$, $L = 10 \text{ mH}$