Design of on-chip sensors to monitor electromagnetic activity in ICs: Towards on-line diagnosis and self-healing

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Design of On-Chip Sensors to Monitor Electromagnetic Activity in ICs: Towards On-line Diagnosis and Self-Healing

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Abstract—**With the growing concerns about electromagnetic compatibility of integrated circuits, the need for accurate prediction tools and models to reduce risks of non-compliance becomes critical for circuit designers. On-chip characterization of noise becomes necessary for model validation and design optimization to reduce redesign costs and time-to-market for IC manufacturers. This paper presents an on-chip noise sensor dedicated to the study of various aspects of electromagnetic compatibility at circuit level, such as power and signal integrity, substrate coupling, conducted emission and susceptibility to electromagnetic interferences. The different architectures of the sensor are presented as well as a demonstration of its measurement performance and benefits through many case studies. Applications of on-chip measurement may be extended towards online diagnosis and self-healing.**

Index Terms— **Electromagnetic compatibility, signal and power integrity, integrated circuits, on-chip sensor.**

I. INTRODUCTION

THESE last years, the concerns about electromagnetic compatibility (EMC) of integrated circuits (IC) (emission and susceptibility issues), power and signal integrity have grown considerably. The need for prediction, during the design stage, of electrical failure risks has become critical for IC manufacturers in order to reduce redesign costs and time-to-market [1]. Although several tools and prediction methodologies have been developed recently [2] [3], accurate measurements of on-chip noise are still critical information for designers for model validation and design optimization.

For ICs emission characterization, on- chip measurement is an efficient method to study fast transient current induced by circuit activity instead of external characterization that is limited by the bandwidth of CMOS analog buffer and electrical parasitic elements of chip and package interconnects. For ICs immunity issues, on-chip measurement is the most efficient way to characterize EMI-induced noise and its effects on a sensitive node of a circuit. Studying noise propagation path and sensitivity of a disturbed function are critical information for IC designers to provide robust designs.

This paper aims at demonstrating the positive contribution of on-chip measurements to characterize accurately and solve power integrity, simultaneous switching noise, ground bounce, crosstalk, near-field and substrate coupling issues. Section II of this paper presents the general requirements of the on-chip noise sensor, its architecture and two different acquisition modes. The third section describes the sensor design and the experimental characterization of its performances. In the last section, a demonstration of its measurement performance and benefits through three cases studies is proposed.

II. ON-CHIP NOISE SENSORS

Most on-chip waveform capturing circuits are based on subsampling cell [4] [5] dedicated to repetitive signal measurements with very small time resolution, comprised between 100 ps [6] and 10 ps [7] [8]. Despite excellent time resolution characteristics, the circuit under test must operate in a special mode where a reproducible event is generated, so the noise produced during normal operating mode cannot be characterized. To overcome this issue an asynchronous sensor using a random sampling acquisition is proposed to provide valuable information about non-periodical signals.

A. Synchronous on-chip noise sensor

A first version of the on-chip noise sensor was designed in the early 2000s to address signal and power integrity issues at circuit level [9] [10]. The sensor is based on a sequential equivalent-time sampling [11]. Its architecture and the principle of signal reconstruction are described in Fig. 1. An on-chip sample and hold (S/H) circuit directly probes the voltage along circuit interconnects and operates in sub-sampling conditions. The probe input impedance is large enough to ensure a non-invasive measurement. The signal acquisition is made over several occurrences of a reproducible phenomenon, and only one sample is taken at each repetition.

An external synchronization signal is used to both trigger off the on-chip event to characterize and activate the S/H cell.
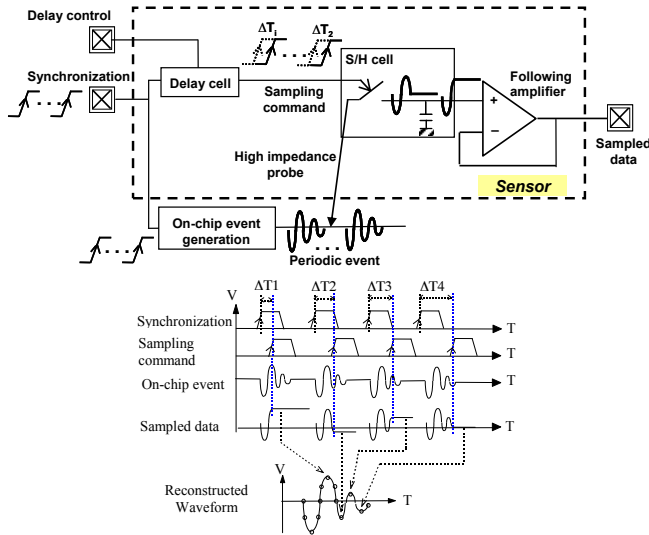
Fig. 1. Original synchronous on-chip noise sensor architecture and sequential equivalent-time sampling principle

The sampling command is shifted from the synchronization signal by a delay cell. The time resolution of the reconstructed waveform is set by the minimum delay step, while its duration is set by the maximum delay produced by the delay cell. Samples are externally stored for waveform reconstruction. A very high virtual sample rate can be reached without severe constraints on hardware bandwidth.

B. Asynchronous on-chip noise sensor

In some case as for EMI-induced noise, reconstruction of waveforms based on sequential equivalent-time is difficult. By definition, the EMI characteristics are unknown (amplitude, frequency, and waveform). Waveform reconstruction of the EMI-induced noise relies on acquisitions triggered on a repeatable external interference, which is possible only if the characteristics of the interference are known in advance. However this condition is not always ensured, so the signal is sampled at random instants and the waveform cannot be reconstructed. Nevertheless, even if the sampling cannot be synchronized with the noise, an asynchronous or random sampling can provide valuable information [13] [14]. The proposed sensor reuses the same architecture but operates in asynchronous sampling mode. The S/H cell and the output amplifier are kept but the delay cell is removed. A low frequency trigger commands the S/H cell to randomly subsample the input signal. The value stored at the S/H cell output is a random variable that constitutes the outcome of the instantaneous amplitude of input signal measurement. As explained on Fig. 2, this random acquisition allows the extraction of signal amplitude probability density function (PDF). The PDF provides the likelihood of the input signal having a given amplitude at any time. Whatever the input signal frequency, the PDF of the signal amplitude can be correctly extracted provided that the S/H cell the output amplifier does not distort or filter the sampled signal.
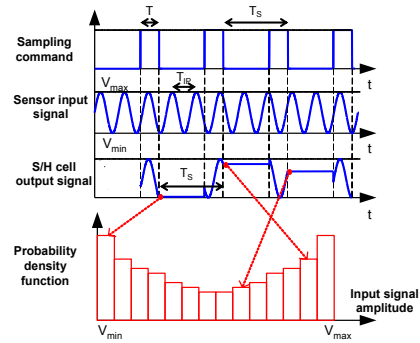

Fig. 2. Asynchronous sampling of a signal and extraction of probability density function of the signal amplitude [12]

III. SENSOR DESIGN AND CHARACTERIZATION

A. Design of the on-chip noise sensor

1) General architecture

Fig. 3 presents the general architecture of the on-chip noise sensor that is split in two parts: the probes and the core. Each of the 8 sensor probes is made of three main elements: an attenuator, a sample and hold cell that operates in sub sampling mode and an output amplifier. The attenuator and the S/H cell form a high impedance probe that ensures a low intrusive voltage measurement. The sensor core aims at selecting one of the 8 probes, generating the sampling command with a controlled delay (in order to reconstruct the signal in time domain) and at providing the output signal through a non-inverting CMOS amplifier.
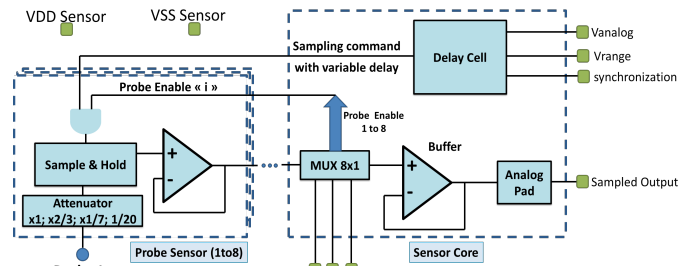

Fig. 3. On chip sensor general architecture

The sensor response is sensitive to voltage fluctuations coupled on its power supply and its substrate reference. The isolation of the sensor to external disturbances and to noise produced by the other blocks of the circuit is a critical requirement. Thus the output amplifier and sensor input-outputs are supplied by an external and dedicated power supply. At board level, this power supply is separated and carefully decoupled. The S/H cell and the amplifier input stage are supplied by a quiet power supply provided by an internal built-in voltage regulator and powered by sensor power supply. To prevent from interference coupling on the sensor by the substrate, all the devices of the sensor are isolated from the P substrate by a buried N layer and dielectric-filled trenches on the sides.

2) Attenuator design and Sample-and-Hold cell

The attenuator and the S/H cells (fig. 4) are the most critical part of the sensor to ensure a large bandwidth, improve the linearity and reduce the voltage dependence. They are made of isolated low voltage transistors to prevent the impact of external disturbance and reach a bandwidth higher than 2GHz. The attenuator is based on a resistive voltage divider made of polysilicon resistor. Polysilicon capacitors C1 and C2 are added to compensate the parasitic capacitance of the resistors (C_{R1} and C_{R2}) and maintain a flat frequency response. The input impedance of the attenuator is large enough to ensure a non invasive voltage measurement.

The S/H cell is composed of a transmission gate switch and a storage node (switch parasitic capacitors, amplifier input capacitor and an extra storage capacitor). The sizes of the transmission gate transistors are carefully chosen to optimize the bandwidth and reduce the voltage dependence of the on-state resistance. Moreover, a dummy transmission gate compensates the charge injection effect when the switch is turned off.
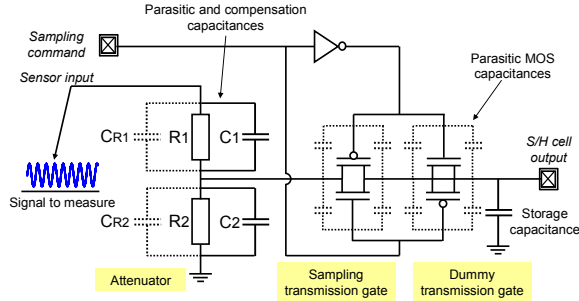

Fig. 4. Schematic of the attenuator and the sample and hold cell

3) Sensor Delay Cell

The delay computed between nodes A and B (fig. 5) depends on two external analog voltages, "Vanalog" and Vrange, applied to control the delay cell. The delay law versus "Vanalog" features a good linearity. "Vrange" offers the possibility of tuning the delay range to be compatible with the signal to measure.
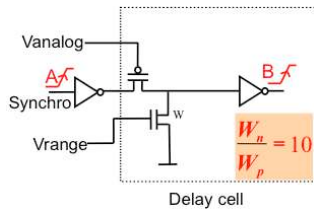

Fig. 5. Schematic of the delay cell

4) Sensor Output

Analog output signals are driven off the chip through a non-inverting CMOS amplifier, externally stored and processed by a digital acquisition card. The output stage has been optimized to keep a constant gain up to few MHz, reduce parasitic offset and stability issues. The bandwidth of the output amplifier does not affect the sensor bandwidth since the amplifier does not process the sensor input signal, but the S/H output signal (constant value).

B. Characterization of the sensor

The sensor operation is affected by imperfections and mismatch in the implementation of its elements, which degrades the output responses. The output amplifier is not perfectly linear so the gain is not constant. Besides, errors in attenuator resistance values can change the gain of the sensor. Moreover, both the amplifier and the parasitic capacitance of the S/H cell produce an offset voltage. The input-output characteristic is measured to check the sensor linearity and then calibrate the sensor. It consists in applying a constant and known voltage on the sensor input and measuring the voltage amplitude of the output samples. A linear relation can be established between sensor output and input. From this relation, both static gain and offset can be extracted to compensate sensor imperfections. However, this characterization and the measurement repeatability are disturbed by random errors due to intrinsic noise, interference coupling, and accuracy of equipments used to produce the reference voltage and measure the sensor output. In order to evaluate the measurement accuracy, for different input voltage values included in the sensor input voltage range, the output signal is sampled 10 times at various moments and the standard deviation of the output sample distribution is computed. The measurement uncertainty is estimated to 10mV and the time resolution is about 10 ps.

The sensor bandwidth is limited by the cut-off frequency of the equivalent RC filter composed by the attenuator and the S/H cell. The S/H cell transfer function is measured by sampling a sinusoidal signal of known amplitude with a varying frequency. The sensor bandwidth increases with the technology (2.5 GHz in 0.25 µm, 10 GHz in 90nm, 15 GHz in 65nm)

When measurements are conducted in a harsh environment, if a very high accuracy is required, sensor performance has to be evaluated to apply data post processing in order to compensate gain and offset drifts due to very high or very low temperature.

IV. EXPERIMENTS

A. Power integrity characterization

A test chip designed in Freescale CMOS 90 nm technology, which includes a digital core and synchronous on-chip sensors dedicated to power supply voltage fluctuations measurements, has been developed to characterize the evolution of PI vs. time [15]. The digital core structure is a basic 100-stage shift register, synchronized by a 40 MHz clock. In order to monitor the voltage drops on the power supply of the digital core, the on-chip voltage sensor is placed along the core power supply rail and synchronized on the core clock. It is able to measure the waveform of voltage bounce in time domain with a precise time resolution (up to 15 ps). Its analog bandwidth is equal to 10 GHz in this technology. Fig 6 presents the power supply voltage fluctuations produced by the digital core activity

measured by the on-chip sensor. Positions of clock edges are indicated. Rapid droops appears at each clock switching. This event is linked to the rapid current demand from every gates and latches of the core. A damped oscillation with a pseudo-period equal to 4.5 ns follows the first rapid current impulsion. It is linked to the anti-resonance produced by on-chip capacitor and package inductor. On-chip measurements to characterize power integrity have both interests: offering measurement points to non accessible nodes and suppressing the high frequency attenuation due to I/O pads and package. Comparison between the power supply voltage fluctuations measured by the on-chip sensor and simulated by a standard ICEM model (fig. 7) demonstrates that accurate measurements of on-chip noise is useful for model validation [16].
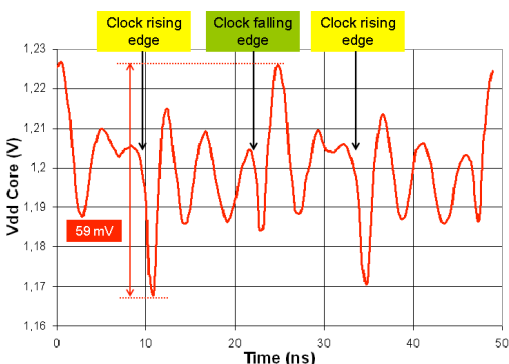

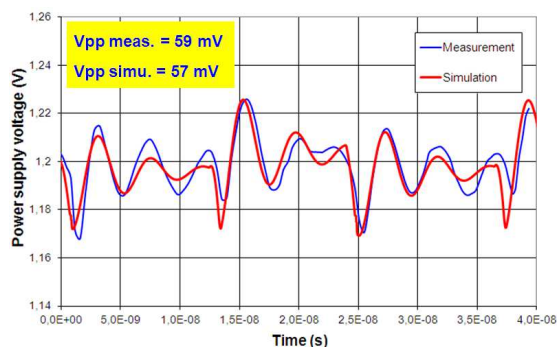Fig. 6. Measurement of the power supply voltage bounce of the digital core

Fig. 7 Comparison between measurement and simulation of the digital core power supply voltage bounce

B. Characterization of propagation of conducted noise along a power supply rail

An asynchronous on-chip sensor has been implemented on the power supply rail of the digital core in a 0.25 µm SMARTMOS technology test chip from Freescale Semiconductor dedicated to the susceptibility characterization. The sensor aims at measuring the amplitude and the statistical distribution of voltage fluctuations induced by conducted EMI [16] injected by DPI on the digital core power supply. This information is critical to study on-chip induced noise propagation and its effects on ICs susceptibility.

Power supply voltage fluctuations are measured either

externally with an oscilloscope active probe, or internally with the sensor. The oscilloscope and the active probe present large frequency bandwidths (2.5 GHz) to characterize accurately EMI voltage fluctuations up to 1 GHz.

Results illustrated in Figure 8 show the susceptibility threshold of the digital core with the 0.25 V voltage fluctuation criterion applied on the power supply net, obtained with on-chip and off-chip measurements. The most critical frequency band regarding susceptibility issues is above 50MHz. When the EMI frequency is less than 50 MHz, both measurement methods provides the same susceptibility thresholds, i.e. for a given EMI amplitude, the power supply voltage fluctuation is the same off-chip and on-chip. However, above 50 MHz, inside and outside IC measurement methods give divergent results. An over-estimated immunity level with the external measurement is observed. The difference between both susceptibility thresholds reaches 23 dB. The origin of these differences is linked to the different measurement locations. Package and circuit filtering affect differently on-chip and off-chip EMI-induced noise. The significant measurement discrepancies between on-chip and off-chip EMI-induced noise can lead to different evaluation of circuit susceptibility. This measurement shows that the on-chip noise sensor provides a more accurate measurement of EMI-coupling across the digital core above 50 MHz. Around 100 MHz, the amount of EMI-induced noise tends to be underestimated by off-chip measurement, while it is overestimated above 200 MHz. Moreover, the complex on-chip propagation of conducted EMI can be understood more clearly by on-chip noise sensor measurement.
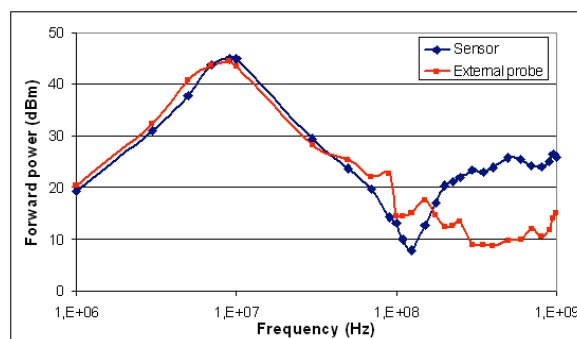

Fig. 8. Comparison of the susceptibility threshold between on-chip and off-chip measurements.

C. Characterization of digital clock integrity

The on-chip sensor (OCS) can be also used to observe the failures induced in analog or digital circuits by the coupling of electromagnetic disturbances on power supply and ground references. The following example illustrates the characterization of desynchronization issues of a digital circuit by the on-chip sensor. The voltage fluctuations induced on power supply and ground references leads to a degradation of the quality of clock signals, especially by the generation of jitter. If timing constraints on set-up and hold times are violated, failures may arise [17].

An on-chip sensor has been placed within the clock tree of the digital core presented in IV.A to characterize its degradation when electromagnetic disturbances are conducted along the power supply network of the circuit. The conditions of time reconstruction of the clock are ensured since the sensor sampling command is synchronized on the clock signal. In order to capture the worst-case degradation of the clock, the electromagnetic disturbance generation is not synchronized on the clock signal and thus on the sensor sampling command. As a large number of clock waveforms are acquired (1500 waveforms) and superimposed, the sensor is equivalent to an oscilloscope with persistence display mode. Fig. 9 presents the reconstructed time profile of the clock disturbed by a 500 MHz harmonic signal coupled on the power supply pin. Two types of degradation are measured. First, the logic levels '0' and '1' are affected by a sinusoidal voltage fluctuation with peak-to-peak amplitude equal to 450 mV. If the noise amplitude exceeds the switching threshold V_{TH} of core flip-flops, the logic state of the clock may change. The second degradation is the increase of jitter. It is extracted by measuring the distribution of the instants at which the clock crosses the threshold level V_{TH}.
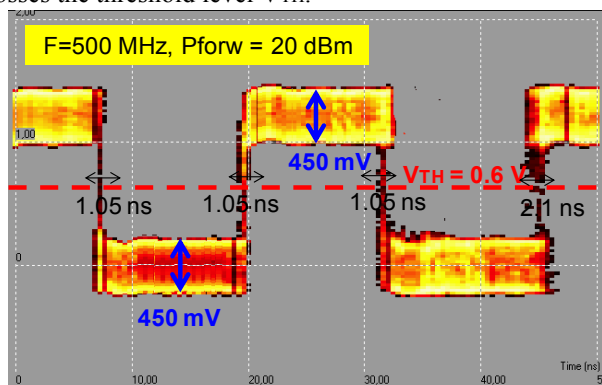

Fig. 9. Time profile reconstruction of the clock of a digital synchronous circuits disturbed by a 500 MHz harmonic signal [18]

The dependency of jitter to the electromagnetic disturbance frequency and amplitude can be characterized with the on-chip sensor, as shown in Fig. 10. The previous acquisition is repeated by changing the frequency and the amplitude of the harmonic disturbance. The jitter increases quasi linearly with the disturbance amplitude, but tends to decrease with disturbance frequency. The measured evolution of jitter can be compared to simulations to validate the modeling of jitter generation and digital failure prediction.
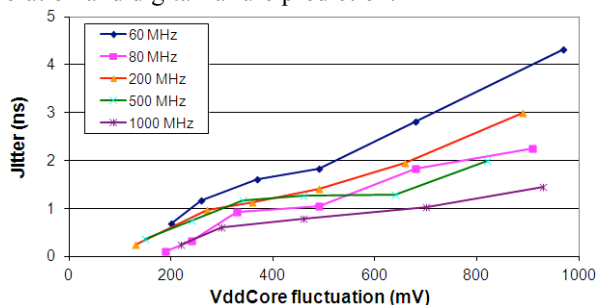

Fig. 10. Measurement of clock jitter evolution vs. amplitude and frequency of a disturbance conducted on power supply [ref2]

D. Near field probe Induced noise characterization

The on-chip sensor constitutes a powerful tool to characterize the physical interaction between a noise source and a circuit, and validate its modeling. The following part shows an original use of the on-chip sensor during near-field injection test. Near-field injection constitutes a promising method for electromagnetic attacks on cryptographic circuits [19] or local fault injection for functional safety evaluation. The method consists in placing a miniature near-field probe in the vicinity of a die and injecting disturbance signals in the probe in order to induce a local voltage fluctuation along circuit interconnects and thus trigger a failure. The prediction of failure triggering relies on an accurate modeling of the physical interaction between the near-field probe and the circuit under test. For this purpose, a test chip has been designed core in a 0.25 µm SMARTMOS technology test chip from Freescale. The circuit contains 32 on-chip sensors placed on various lines and digital buses. The sensor measurements aim at proving that the injection is local, enough powerful to induce failure and validating the model of the coupling between the injection probe and the circuit under test.

The following example presents the measurements of voltage fluctuations induced along parallel silicon lines by a magnetic near-field probe. The lines are identical and separated by an increasing distance. The reference line is noted 0 µm. The on-chip sensor measurements are performed on this line and three other lines separated by 0.455, 120 and 320 µm respectively. The near-field probe is placed at 300 µm above the surface of the die and moved perpendicularly to the lines, as described in Fig. 11.
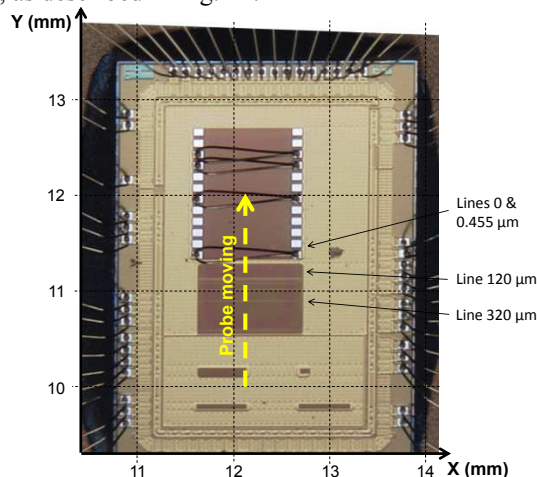

Fig. 11. Position of test line structures and probe moving trajectory

The near-field probe is excited by a 1.4 GHz harmonic signal, which is synchronized on the on-chip sensor sampling command in order to ensure time reconstruction of voltage fluctuation profiles. Fig. 12 compares the evolution of the voltage fluctuation amplitude induced on the four lines according to the near-field probe position. Arrows indicate the probe positions for which the injection is optimal on each line. The induced voltage is optimal on a line when the probe is placed just above. If two lines are separated by a distance greater than the probe resolution, it is possible to distinguish
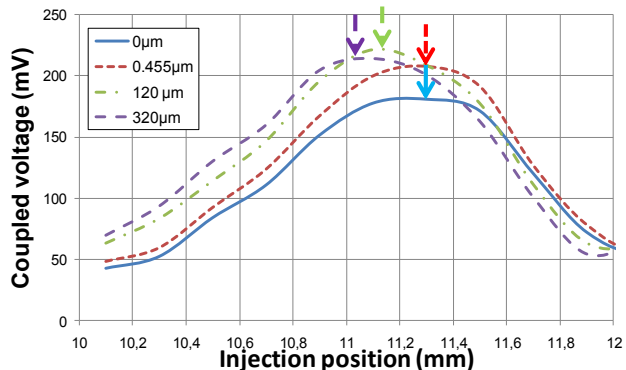
which line is the more disturbed.

Fig. 12. Evolution of the voltage induced on four parallel silicon lines according to the position of a magnetic near-field probe

V. CONCLUSION

This paper aims at demonstrating the positive contribution of on-chip measurements to characterize accurately and solve power integrity, simultaneous switching noise, ground bounce, crosstalk, near-field and substrate coupling issues… Several versions of this sensor have been developed over years in different technologies and for various experimental characterizations. Two versions of the sensor have been presented in the paper: synchronous and an asynchronous acquisition principle. The main advantages of this sensor are its small surface, its large bandwidth, its high linearity and robustness to electrical stress, at the price of a simple design.

Through the four different experiments, presented here, we demonstrate the benefit of on chip noise measurements.

For example, for circuit designers, using this type of on-chip sensor are of great interest as it provides a precise characterization of noise propagation within the die, helps to identify the sensitive blocks, extract their actual susceptibility level and validate their models. On chip measurements could facilitate failure diagnosis and the modeling of complex parasitic couplings between separated blocks, such as substrate coupling, crosstalk…

Prospective of this work will be an extension of the method towards on-line Diagnosis and Self-Healing by developing a self-adaptive technique based on on-chip sensor to design power-supply noise-immune ICs.

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