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# NMOS Device Optimization for the Design of a W-band Double-Balanced Resistive Mixer

Christophe Viallon, *Member, IEEE*, Grégory Ménéghin, and Thierry Parra

**Abstract**—This letter describes the implementation of NMOS devices in a passive ring mixer whose operating frequency reaches device’s cut-off frequency. Conversion gain, linearity and required LO power are discussed regarding device geometry using simple analytic formulas and electrical simulations. The mixer is then embedded in a down-converter including RF, LO and IF buffers and integrated in a 130 nm BiCMOS SiGe technology. Measurements indicate a conversion gain of 14.5 dB at 76.8 GHz, an output-referred 1 dB compression point of  $-10$  dBm and a DSB noise figure of 6.3 dB confirming the interest of double-balanced passive mixers at millimeter-wave frequencies.

**Index Terms**—millimeter-wave, low-noise, resistive mixer, passive mixer, W-band, zero-IF receiver.

## I. INTRODUCTION

THE last decade has seen a growing number of applications in the millimeter-wave frequency range. Under constant developments, nanoscale silicon technologies become competitive with III-V for applications exceeding 100 GHz.

Whereas resistive mixers are widely used on III-V technologies at such high frequencies, active mixer topologies seems to be so far preferred on Si technologies. W-band active mixers meet an abundant literature [1]–[3]. These mixers provide good port-to-port isolation and conversion gain. Nevertheless, some recent works have reported 60 GHz single-ended [4] [5] and single-balanced [6] resistive mixers using 90, 130 and 65 nm CMOS process respectively, and more recently, a 65 nm CMOS single-balanced resistive mixer has been demonstrated at 283 GHz in a sub-harmonic configuration [7]. Despite conversion losses, these resistive mixer topologies exhibit better linearity and better noise performances, particularly for zero-IF receivers because the absence of flicker noise.

In this letter, a double-balanced resistive mixer is demonstrated in a 130 nm BiCMOS SiGe process. As presented in section II, mixer performances can be kept at frequencies close to NMOS cut-off frequency ( $f_t \simeq 85$  GHz), when device geometry is carefully optimized. The implementation of this mixer within a zero-IF UWB automotive radar down-converter, as well as overall performances are given, then, in section III.

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## II. DESIGN METHODOLOGY

A MOS device used under cold bias condition ( $V_{DS} = 0$ ) acts as a simple conductance  $g_{ch}$  whose value is controlled by the intrinsic part of Gate-Source Voltage  $V_g$  (see Fig.1a).

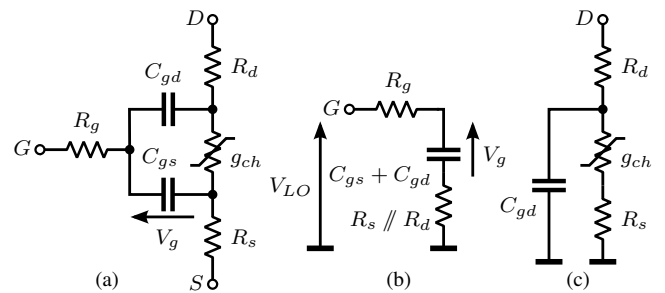


Fig. 1. Simplified equivalent circuit of a cold MOS device (a), ring mixer circuit seen by LO source (b), simplified Drain-Source impedance model (c).

A pump signal applied to the gate turns the channel into a time-varying nonlinear conductance that produces the frequency mixing. Two major limitations appear as the transistor is pushed toward its frequency limits.

The first one is located at the command side of the device, between gate and source connections. The channel conductance is controlled by the voltage  $V_g$  across  $C_{gs}$  (Fig.1a). The ratio between  $V_g$  and  $V_{GS}$  is decreasing as frequency increases and depends on the extrinsic elements  $R_g$  and  $R_s$ . When a differential LO voltage is applied across the gates of the four mixing devices of a ring mixer, drains and sources appear to be virtually grounded at the LO frequency. Since  $R_d \simeq R_s$  and  $C_{gs} \simeq C_{gd}$  at  $V_{DS} = 0$ ,  $V_g$  is deduced from  $V_{LO}$  using the equivalent circuit of the LO input of the mixer (Fig.1b):

$$V_g \simeq \frac{V_{LO}}{1 + j\omega (R_g + R_d // R_s) (C_{gs} + C_{gd})} \quad (1)$$

This expression suggests that the device remains efficiently driven as long as the condition  $\omega_{LO} \ll \omega_{c1}$  is fulfilled, with

$$\omega_{c1} = \frac{1}{(R_g + R_d // R_s) (C_{gs} + C_{gd})} \quad (2)$$

$\omega_{c1}$  is maximized using the smallest possible NMOS device, since  $C_{gs}$  and  $C_{gd}$  are proportional to gate area.

The second limitation comes from the drain-source time-varying equivalent impedance (Fig.1c). This network is derived from Fig.1a given that for a ring mixer gates are virtually grounded at RF frequency and that  $C_{gs}$  and  $C_{gd}$  reactances are much greater than  $R_g$  and  $R_s$  [8]. The lowest and highest values taken by  $g_{ch}$  are driven by the amplitude of  $V_g$  and the

DC bias. The drain-source impedance then swings between  $Z_{on}$  and  $Z_{off}$  :

$$Z_{on} \simeq R_s + R_d + \frac{1}{g_{ch}} = R_s + R_d + \frac{L}{W} \rho_{ch} \quad (3)$$

$$Z_{off} \simeq R_d + \frac{1}{j\omega C_{gd}} \simeq \frac{1}{j\omega C_{gd}} \quad (4)$$

with  $L$ ,  $W$  the gate length and width, respectively, and  $\rho_{ch}$  the channel resistivity. The equivalent circuit displayed on Fig.1c suggests that the transistor is operating as a diode and thus can be analyzed in the same way [9]. Hence, the optimal conversion losses  $L_{opt}$  depend on the  $Z_{on}/Z_{off}$  ratio:

$$L_{opt} = 1 + 2 \left( \frac{Z_{on}}{Z_{off}} \right)^2 \left[ 1 + \sqrt{1 + \left( \frac{Z_{on}}{Z_{off}} \right)^2} \right] \quad (5)$$

$$\left| \frac{Z_{on}}{Z_{off}} \right| \simeq \frac{\omega_{RF}}{\omega_{c2}} \text{ with } \omega_{c2} \simeq \frac{1}{(R_s + R_d + \frac{L}{W} \rho_{ch}) C_{gd}} \quad (6)$$

$L_{opt}$  is lowered if  $\omega_{c2}$  is maximized. As for  $\omega_{c1}$ , this condition occurs using the smallest NMOS device. The resistive mixer is then theoretically optimized for low conversion losses but the linearity must be now investigated.

The linearity is mainly affected by the transition time between ON-state and OFF-state of NMOS devices which produce the mixing. This switching time may be reduced by improving the rate of change of the channel conductance  $g_{DS}$  over  $V_{GS}$ . Starting from the simple square-law  $I_{DS}$  expression of a NMOS device driven in triode region, the following relation is deduced [10]:

$$\frac{\partial g_{DS}}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} \quad (7)$$

with  $\mu_n$  the electron mobility and  $C_{ox}$  the gate-to-channel capacitance per unit area. This expression means that linearity is improved by increasing  $W$ . But parasitic effects are not taken into account and, as long as  $W$  is increased, the aforementioned first limitation arises ( $\omega_{c1}$ ), pulling down linearity.

One last remaining issue is the terminal resistances  $R_g$ ,  $R_d$  and  $R_s$  of NMOS transistors. With today nanoscale MOS technologies, these resistance values appear to be quite large, especially  $R_g$ . As displayed on Fig.2, this resistance results from the contact resistance  $R_{con}$  along with a salicided polysilicon resistance from contact to active region  $R_{ext}$ , and the distributed gate resistance over active area [11], [12].  $R_g$  expression is then:

$$R_g = \frac{R_{con}}{n} + \frac{R_{ext}}{n} + \frac{R_{g\Box} W_f}{3 n L} \quad (8)$$

with  $R_{g\Box}$  the gate sheet resistance per square,  $W_f$  the finger width, and  $n$  the number of fingers. This expression points out that  $R_g$  scales down as the number of gate fingers increases, as for  $R_s$  and  $R_d$  [13].

Finally, the expressions (2), (6) and (7) suggest that conversion losses and linearity of a resistive mixer are enhanced using NMOS devices with the smallest  $L$ .  $W$  is chosen to provide the best linearity, and the number of fingers is increased to minimize the influence of extrinsic elements, because of (8). This result has been verified by performing electrical

simulations on a resistive ring mixer fed with ideal baluns. The gates bias is adjusted near threshold voltage so that the best  $Z_{on}/Z_{off}$  ratio can be reached from the swing of  $V_g$ . Conversion loss and output-referred 1 dB compression point ( $OP_{1dB}$ ) are plotted on Fig.3 at a LO power of 5 dBm for various device geometries. As expected, the best conversion efficiency is obtained using a device with the smallest allowed length and width. The linearity is optimized by increasing  $W$  up to the range 10–20  $\mu\text{m}$ . Both characteristics are improved as the number of gate fingers is increased. However, no further improvement is observed above 8 fingers.

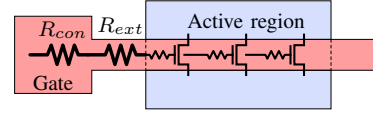


Fig. 2. Gate parasitic resistance distribution on MOS device.

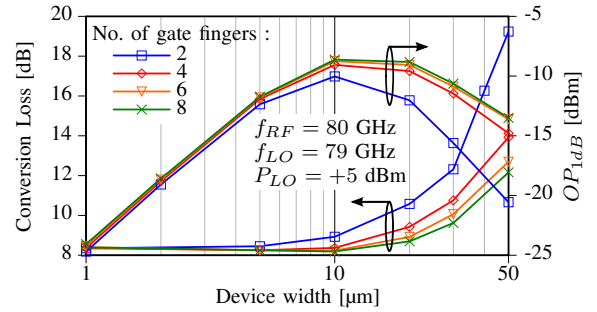


Fig. 3. Simulated conversion loss and  $OP_{1dB}$  of a ring mixer fed with ideal baluns for different NMOS width  $W$  and number of fingers.

### III. DOWN-CONVERTER DESCRIPTION AND MEASUREMENTS

Previous stated rules have been applied to the design of a double-balanced down-converter. The passive ring mixer using four  $0.13 \times 2.5 \times 8 \mu\text{m}^2$  NMOS devices is surrounded by three amplifiers at RF, LO and IF terminals (Fig.4). SiGe HBTs are used for RF and LO buffers to take advantage of their attractive performances regarding noise and  $f_t$ . The total DC power consumption is 118 mW at 2.5 V (42 mW, 36 mW and 40 mW for LO, RF and IF buffers, respectively). More details on this chip are given in [14]. It has been fabricated using a  $0.13 \mu\text{m}$  SiGe BiCMOS process with HBT cutoff frequencies  $f_t/f_{max}$  of 230/280 GHz from ST-Microelectronics. On-chip rat-race baluns have been included at RF and LO balanced terminals to enable single-ended on-wafer characterization. Without baluns and pads, the active part of the chip is  $700 \times 400 \mu\text{m}^2$ . A specific test-bench has been developed to extract the conversion gain, compression point and noise figure. IF signal is measured from one of both outputs, the other one is connected to an AC-coupled  $50 \Omega$  load. All measurement data are referred to the pads of the chip.

The conversion gain versus LO power is shown in Fig.5 at a LO frequency of 76 GHz. The measured  $OP_{1dB}$  is  $-10$  dBm. This power is strongly limited by the IF amplifier which

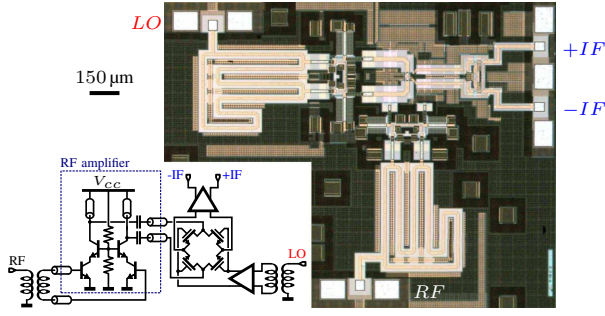


Fig. 4. Block-diagram and micro-photograph of the designed chip.

provides a gain of  $\sim 14$  dB from DC up to 2 GHz. It could be improved up to  $+5$  dBm by increasing the linearity of the IF-amplifier since the simulated  $OP_{1dB}$  of the NMOS ring mixer, alone, is  $-8$  dBm (Fig.3).

The double sideband noise figure has been extracted using the cold-source technique from measured conversion gains  $G_{usb}$  and  $G_{lsb}$  at both upper and lower sideband around LO frequency. In our case,  $G_{usb} = G_c$ . The noise figure  $NF_{dsb}$  is extracted from the measured output noise power spectral density  $N_{out}$  using:

$$NF_{dsb} = \frac{N_{out}}{(G_{lsb} + G_{usb}) kT_0} \quad (9)$$

$k$  is Boltzmann's constant and  $T_0$  is 290 K. The noise figure of a resistive mixer can be close to conversion losses by minimizing  $R_s$  and  $R_d$ . Moreover, this kind of mixer is well suited for zero-IF receiver because the absence of shot and flicker noises. Finally, the RF cascode amplifier acts as the RF transconductance stage in the Gilbert mixer: its gain and NF ( $\sim 9$  dB and  $\sim 5$  dB, respectively, under  $50 \Omega$  input and output loads) decrease the NF of the overall down-converter.

The low-noise frequency conversion is confirmed by measurements of Fig.5, where  $NF_{dsb}$  reaches a value of 6.3 dB, for a conversion gain of 14.5 dB, when the LO power exceeds 0 dBm. If we compare with all other published W-band mixers (Table I), these characteristics are quite attractive.

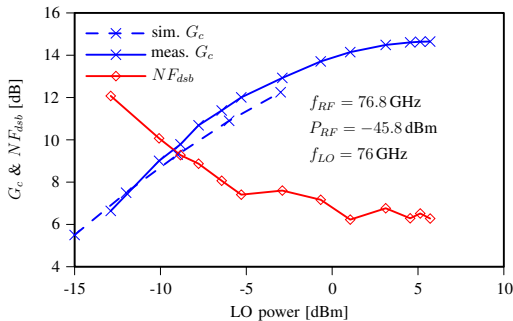


Fig. 5. Measured down-converter conversion gain and noise figure.

#### IV. CONCLUSION

This letter investigates the optimization of a cold-biased NMOS resistive ring mixer. The geometry of NMOS transistor is widely discussed regarding conversion losses as well as

TABLE I  
W-BAND MIXERS REPORTED WITH A LOW NF

Ref.	This work	[1]	[2]	[3]
Technology	130 nm SiGe BiCMOS			65 nm CMOS
Mixer topology	Resistive	SB* active	Gilbert cell	
$P_{DC}$ ** [mW]	76	N/A	40	6
$f_{RF}$ [GHz]	76.8	77	73.8	76
$G_c$ [dB]	14.5	20	8.5	-1.5
$OP_{1dB}$ [dBm]	-10***	+4.3	N/A	-9.5
$NF_{dsb}$ [dB]	6.3	9.8	10.2	8.3

\*SB is for Single-Balanced, \*\* LO buffer excluded, \*\*\*+5 dBm using optimized IF-amp.

linearity. Rules are derived that allow the mixer operation nearby the cut-off frequency of mixing devices. A double-balanced resistive mixer is then demonstrated in the 77 GHz range using a  $0.13 \mu\text{m}$  BiCMOS SiGe process. Simulated and measured results demonstrate that millimeter-wave Si-based resistive ring mixers can compete against their III-V-based equivalents in terms of linearity. In addition, a low noise figure is possible according to the measured NF of 6.3 dB. To the authors' knowledge this result is the best ever reported at such high frequency using a Si-based technology.

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