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Effect of Electrical Stresses on the Susceptibility of a Voltage regulator

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Abstract – Analog circuits such as linear voltage regulators are very sensitive to electromagnetic interferences which induce voltage offset on their outputs. In harsh environments, the aging of this component can be accelerated and could lead to an increase of the effect of electromagnetic interferences. This paper proposes an original study about the drift of the susceptibility level of a low dropout voltage regulator submitted to electrical stresses. Some analyses based on CAD simulations are proposed to explain the experimental observations.

Keywords: analog circuits, electromagnetic interferences, susceptibility, accelerated-ageing, reliability, CAD simulation

I. INTRODUCTION

During their lifetime, electronic systems are exposed to harsh conditions (high temperature, moisture, thermal cycling, overvoltage...) which contribute to accelerate the aging process. Several sources have reported that typical EMC mitigation techniques are affected by harsh conditions [1] [2]. Recently, some research works have shown experimentally or by simulation the potential impact of the aging of integrated circuits on susceptibility to electromagnetic interferences (EMI) [3] [4] [5].

Analog circuits such as linear voltage regulator are very susceptible to EMI. The low dropout (LDO) voltage regulator is widely used in modern electrical systems with severe EMC problems. Various papers have described the failure mechanisms of LDO regulators under conducted EMI, which are linked to the operational amplifier (op-amp) [6] [7] or bandgap circuit cell [8]. Research focuses mainly on the analysis of EMC failure mechanisms and low susceptibility design techniques, but little attention is given to the LDO's real application environment and its effect on susceptibility.

This article describes an original study on the change in LDO susceptibility after aging accelerated by electrical stress. In order to provide a better insight into the impact of intrinsic LDO circuit degradation, experimental characterizations of the susceptibility of a LDO voltage regulator are combined with electrical stresses in order to give the time dependent variations on its electromagnetic behavior. Moreover, SPICE simulations are used to clarify the origins of variations of susceptibility level of the LDO device after aging. Section II presents the

device under test and gives a general description of the typical failure induced by EMI in this circuit. Section III details the susceptibility measurement set-up and conditions for accelerated ageing. Susceptibility measurements before and after stress are presented in section IV. Finally, section V proposes analyses based on simulation in order to clarify the origins of the measured decrease of susceptibility level.

II. IMMUNITY OF LDO VOLTAGE REGULATOR TO ELECTROMAGNETIC INTERFERENCES

A. Test chip description

The LDO regulator under test was implemented in a test chip designed with the Freescale CMOS 90 nm process, and aims to provide a regulated power supply voltage to a small digital core. Fig. 1 illustrates the internal structure of the LDO voltage regulator which contains a Kuijk bandgap [9] reference circuit and an output amplifier designed to work with a +3.3 V supply, applied on terminal V_{IN} . The nominal voltage of the bandgap reference voltage is +1.25 V and given by equation (1). The gain of the output amplifier is 1. Bandgap reference circuit and regulator outputs are monitored through the terminals V_{REF} and V_{OUT} .

$$V_{REF} = V_{BE1} + \frac{R_2}{R_3} \frac{kT}{q} \ln \left(N \frac{R_2}{R_1} \right) \quad (1)$$

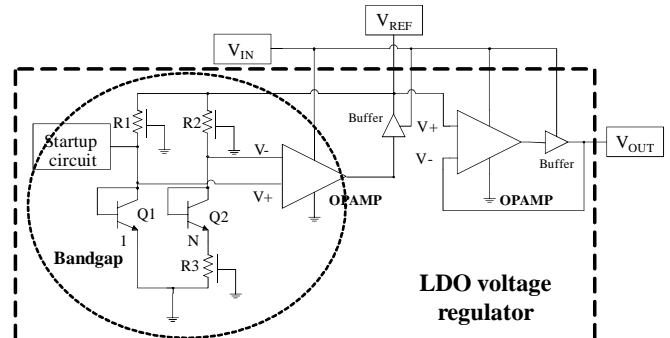


Figure 1. LDO structure and general setup of input/output terminals

B. EMI-induced failure description

RF noise coupled to the power supply pin of a LDO voltage regulator leads to a common failure of analog circuits: the EMI-induced offset [7]. This type of failure is linked to the non-linear operation of the circuit which induces an offset on the regulated output voltage by rectification effect. This failure is very harmful because it cannot be filtered once it has been generated. In our LDO voltage regulator, DC offset can be induced at bandgap and regulator outputs. Two well-known mechanisms can be responsible of the circuit DC shift:

- First, a rectification phenomenon involving the bipolar transistors of the bandgap cell [8]
- Secondly, a distortion phenomenon at the differential input pairs of the op-amps of the bandgap cell and the output follower amplifier [10].

In our test chip, the second mechanism is the more relevant because of the weak coupling between the power supply net and the polysilicon resistor of the bandgap, which prevents from a significant RF noise coupling to the base terminal of both bipolar transistors. Fig. 2 presents an equivalent circuit of the differential input pairs of op-amp when RF noise is coupled to the power supply net. A part of this incoming disturbance can also be coupled on inverting and non inverting input of the differential pair. The PMOS transistors of the differential pair operate in saturation regime and we suppose that voltage fluctuations are sufficiently small to prevent the transistor differential pair from switching off.

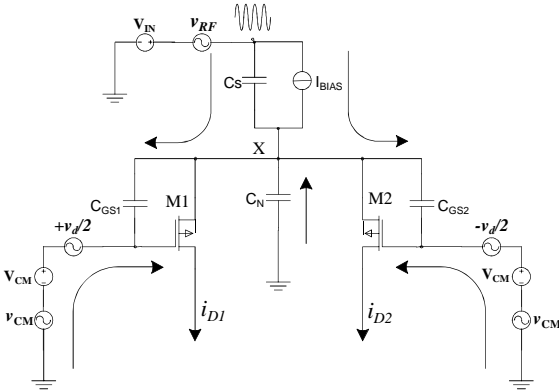


Figure 2. Input PMOS differential pair under interference from power pin and differential pair inputs

Any RF voltage coupled to the gate or source terminals of differential pair transistors causes a DC shift in the differential current, because of the non linear relationship between gate-to-source voltage and drain current of MOS transistor in saturation mode. Three paths for disturbance coupling exist in the bandgap op-amp: one from V_{IN} to the common node "X" of the PMOS differential pair via the parasitic capacitors C_S (C_S represents the parasitic capacitance between V_{IN} and X) and C_{GS} (gate-to-source capacitance of M1 and M2); one from the output to the inverting and non-inverting inputs via the feedback circuit and C_N (C_N represents the parasitic capacitance between "X" and the substrate) offers a possible path for disturbance to be coupled from the substrate. For the op-amp in the regulator output, the first path is the same from

V_{IN} . The non-inverting input couples the disturbance coming from the bandgap output and non-inverting input the noise from the follower amplifier output.

The output offset voltage is calculated in the presence of an RF signal (v_{RF}) with differential (v_d) and common-mode (v_{cm} and V_{CM}) components. The RF noise is coupled to the PMOS source and the differential and common-mode noise are injected into the PMOS gate. M1 and M2 are in the saturation region and of the same size (assume $W=W_1=W_2$, $L=L_1=L_2$). The differential drain current of M1 and M2 is Δi_D which is established as follows:

$$\Delta i_D = \frac{\mu_p C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 - \frac{\mu_p C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 \quad (2)$$

$$= \mu_p C_{ox} \frac{W}{L} v_d (v_{cm} - v_x) + v_d g_m$$

where v_x is the voltage at the common-source node of the differential pair. Let's assume $C_{GS}=C_{GS1}=C_{GS2}$, $C_T=C_S+C_N$ and $g_m=g_{m1}=g_{m2}$:

$$v_x = \frac{s(2C_{GS}) + 2g_m}{s(2C_{GS} + C_T) + 2g_m} v_{cm} + \frac{sC_S}{s(2C_{GS} + C_T) + 2g_m} v_{RF} \quad (3)$$

$$\Delta i_D(s) = v_d(s)g_m + \mu_p C_{ox} \frac{W}{L} v_d(s)Y(s)\{C_T v_{cm}(s) - C_S v_{RF}(s)\} \quad (4)$$

Where

$$Y(s) = \frac{s}{s(2C_{GS} + C_T) + 2g_m} \quad (5)$$

$$|g_m| = \sqrt{I_{BIAS} \mu_p C_{ox} \frac{W}{L}} \quad (6)$$

The differential pair output current average dc offset $\Delta i_{D|avg}$ can be used to calculate the voltage offset on the op-amp inputs $\Delta V_{IN|diff}$ using the transconductance amplification factor g_m of the differential pair stage.

$$\Delta V_{IN|diff} = -\frac{\Delta i_{D|avg}}{g_m} \quad (7)$$

$$|\Delta V_{IN|diff}| = \left| \frac{\mu_p C_{ox}}{2} \frac{W}{L} v_{d, pk} \frac{\omega}{g_m \sqrt{4g_m^2 + \omega^2 (2C_{GS} + C_T)^2}} A \right| \quad (8)$$

Where

$$A = [C_T v_{cm, pk} \cos(Ph(\phi_{d-cm}) + Ph(Y(j\omega))) - C_S v_{RF, pk} \cos(Ph(\phi_{d-RF}) + Ph(Y(j\omega)))] \quad (9)$$

As there is negative feedback on both op-amps, the feedback forces the differential current to cancel out; hence an offset is created on the output voltage. The output voltage of the regulator V_{OUT} can be described as per Eq. (9) below with an offset of ΔV_{OUT} :

$$V_{OUT} = V_{REF} + \Delta V_{OUT1} + \Delta V_{OUT2} = V_{REF} - \left(1 + \frac{R_2}{R_3}\right) \Delta V_{IN1|diff} - \Delta V_{IN2|diff} \quad (10)$$

Where ΔV_{OUT1} and ΔV_{OUT2} are the voltage offset on both op-amp outputs, and $\Delta V_{IN1|diff}$ and $\Delta V_{IN2|diff}$ are the distortion caused by the voltage offsets on both op-amp inputs.

offset increases about 1 or 2 dB after 7 days. Although the circuit is still functional, it becomes less and less robust to EMI.

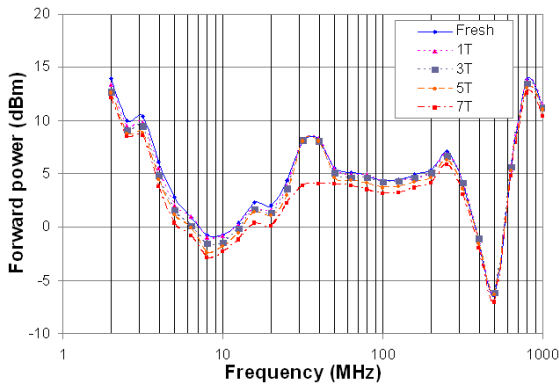


Figure 6. Evolution of measured susceptibility level of the regulator

V. ANALYSIS OF THE EVOLUTION OF THE SUSCEPTIBILITY LEVEL OF THE VOLTAGE REGULATOR

A. Proposed methodology for the analysis

A quantitative prediction of the effect of aging on susceptibility relies on the identification of critical transistors (e.g. based on electrical simulations or functional analysis) and the extraction of variation laws of transistor electrical parameters vs. stress conditions and time. In this case study, the absence of characterization of transistor degradations prevents from an accurate prediction of susceptibility level drift. In spite of the absence of experimental characterization, we can attempt to use CAD simulations to propose and consolidate assumptions about the origins of susceptibility increase. From CAD simulations on the circuit netlist, different scenarios of transistor degradation can be tested: the location of degraded transistors and device parameters affected by degradation mechanisms can be changed in order to observe the impact of the degradations of a specific transistor on the whole circuit susceptibility.

First, an electrical model of the voltage regulator has to be built in order to simulate both the impact of degradation at transistor level and the susceptibility to conducted interferences. Then, the most likely scenarios of transistor degradation have to be set, i.e. propose the location of degraded devices and device parameters affected by degradation mechanisms. Reliability publications report that transistor degradation mechanisms such as Negative Bias Temperature Instability (NBTI) or Hot Carrier Injection (HCI) can have a significant impact on circuit performances by increasing transistor threshold voltage V_{TH} and altering carrier mobility U_0 and drain current [12]. In the following analysis, we assume that threshold voltage and mobility are the only model parameters affected by aging. From SPICE simulations done on circuit netlist, reasonable assumptions about the location of degraded transistors can be done. From the simulation of voltage applied on the different nets of the circuit, we can deduce if one transistor is in a condition that can accelerate a degradation mechanism. For example, a large drain to source voltage accelerates HCI and leads to a reduction of mobility

and an increase of threshold voltage. A large negative gate to source voltage in PMOS transistor accelerates NBTI and leads to an increase of threshold voltage.

Finally, the different degradation scenario can be tested: the circuit netlist is updated from the assumptions about degradation location and modifications of threshold voltage and mobility. SPICE simulations are launched to simulate the impact on the susceptibility level of the LDO voltage regulator. If the simulation predicts similar changes of susceptibility level than those observed in measurements, the assumptions about the origin of susceptibility drift are relevant.

B. Susceptibility modeling of the LDO voltage regulator

A SPICE model of the regulator disturbed by conducted interference according to DPI standard has been developed and validated by comparison with measurements. The voltage regulator model is derived from the circuit transistor netlist. Parasitic elements such as junction capacitors of differential pairs of op-amps, polysilicon-substrate capacitors of poly-resistors are added in the circuit model. The models of the circuit package, external passive devices and printed circuit board interconnects have been fitted with S-parameters measurements. Fig. 7 presents the comparison between the measured and simulated RF voltage sensitivity of the LDO voltage regulator. The simulation result shows a relative good matching over the measurement frequency range. The inaccuracies of the model are linked to the limitations of PCB and circuit substrate models. Nevertheless, as the general susceptibility level of the regulator is simulated correctly, the model is reused to study the impact of electrical stress on susceptibility.

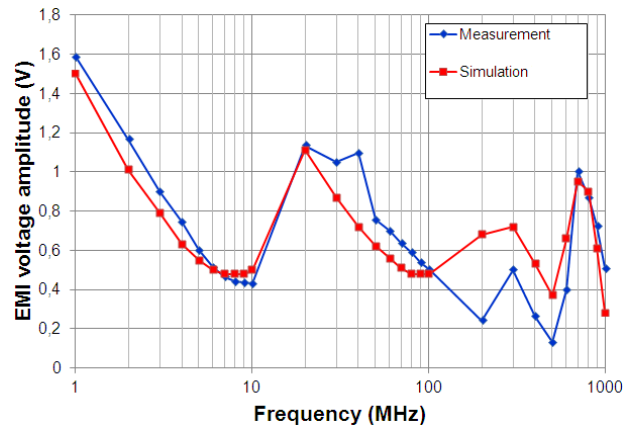


Figure 7. Comparison between DPI measurement and simulation of LDO voltage regulator

SPICE simulations confirm the major role of differential input pairs of op-amps in the generation of DC offset by EMI coupling. Other part of the voltage regulator such as the output buffer has a negligible impact on susceptibility of the device. In the following parts, our attention will be focused on op-amp. The following assumption is made: the susceptibility drift of the LDO voltage regulator is associated to a change in the generation mechanism of DC offset in the differential input pair, and thus to the degradation of op-amp transistors.

C. Identification of the transistors degraded by electrical stress

In order to propose reasonable location of degraded transistors in op-amp, operating point simulations are done to compute the voltage applied on each terminal of the transistors of op-amp under electrical stress condition applied on the power supply pin. Fig. 8 details the electrical schematic of the op-amp. The transistors in voltage conditions which can accelerate degradation mechanisms are highlighted.

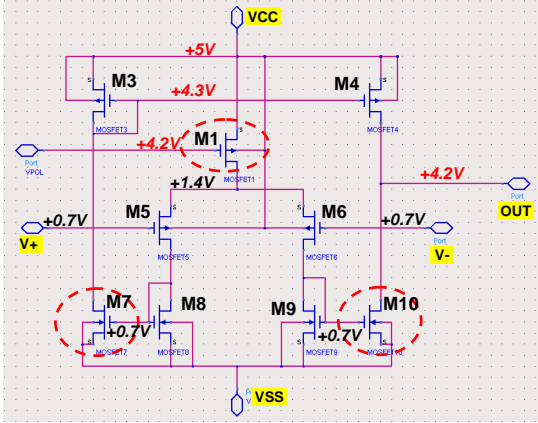


Figure 8. Op-amp schematic and location of transistors degraded by electrical stress conditions in op-amp

Although the differential pair occupies a central position in the EMI-induced offset generation, operating point simulation shows that stress conditions are not applied across terminals of the transistors of the differential pair (M5 and M6). They are certainly not responsible of the observed susceptibility drift. However, three other transistors are placed in stress conditions: the bias current transistor M1 and the output transistors of the current mirror loads M7 and M10. Do these degradations explain a change of the EMI-induced DC offset generation? According to equations (5) and (7), any degradation on M1 contributes to a reduction of its drain current I_{BIAS} , which leads to reduction of the transconductance g_m of differential pair transistors and thus an increase of the EMI-induced offset. The combined degradation of M7 and M10 contributes to a decrease of the open-loop gain of the op-amp. It reduces the negative feedback below the op-amp unity gain frequency. These intuitive assertions can be verified by SPICE simulations.

D. Simulations of the impact of electrical stress on the susceptibility level of the voltage regulator

Several degradation scenarios are tested with SPICE simulations. First, the impact of the degradation of the bias current transistor M1 is tested. Several simulations of the susceptibility of the voltage regulator are performed when the threshold voltage V_{TH} of M1 transistors of both op-amps are increased. Fig. 9 presents the evolution of the susceptibility level of the LDO voltage regulator for different values of V_{TH} . The simulation results show that the sensitivity to RF voltage fluctuations increases constantly over all the frequency range when V_{TH} increases. This non frequency dependent behavior is similar to the measured susceptibility level drift so this degradation scenario is certainly realistic.

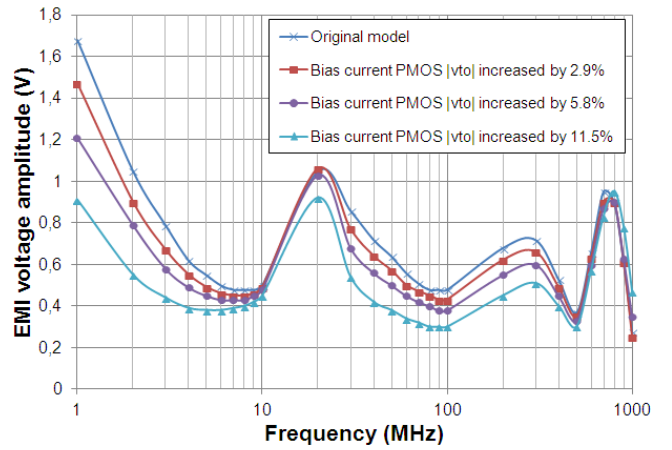


Figure 9. Simulation of the effect of bias current transistor (M1) degradation on the LDO voltage regulator susceptibility

Secondly, the impact of the combined degradations of transistors M7 and M10 on the susceptibility level is tested, as shown in Fig. 10. The threshold voltage is increased in both transistors symmetrically. The susceptibility level of the regulator is affected seriously in low frequency, i.e. below the op-amp unity gain frequency. It confirms the previous assertion about the impact of M7 and M10 degradations. However, this degradation scenario is unlikely since the measured susceptibility level increase is not more important at lower frequency.

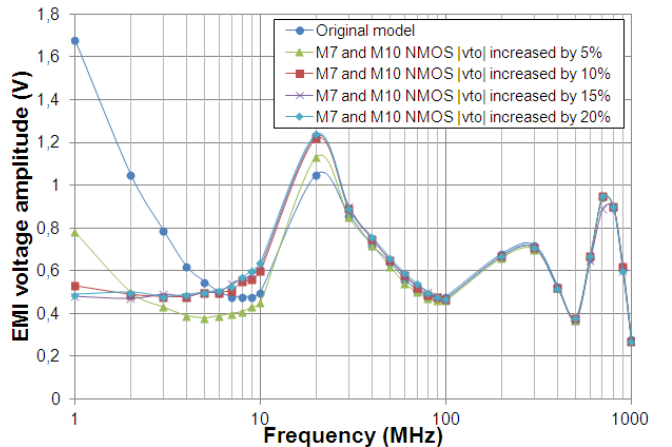


Figure 10. Simulation of the effect of the combined degradations of transistors M7 and M10 on the LDO voltage regulator susceptibility

VI. CONCLUSION

This paper has presented an original study of the impact of aging induced by electrical stress on the conducted susceptibility of a low dropout voltage regulator. This type of analog circuit is sensitive to radiofrequency interferences coupled to the power supply which induce voltage offsets at the output, mainly due to rectification effects at the differential inputs of internal operational amplifiers. The experimental results have shown that the aging accelerated by electrical stress leads to a general increase of the susceptibility to electromagnetic interferences conducted along the power supply. In other word, a given voltage offset arises on the

regulator output for a smallest amount of disturbance. Analyses based on CAD simulations have confirmed that this reduction of susceptibility level can be activated by intrinsic degradation mechanisms at transistor level. One degradation scenario can explain the broadband increase of the susceptibility level of the voltage regulator: the electrical stress applied on the power supply tends to deteriorate the bias current transistor of operational amplifiers. As the EMI-induced offsets in operational amplifier are directly linked to the bias current, this internal degradation leads to an increase of the DC offset generation. Further studies combining susceptibility measurements after electrical stresses and CAD simulations will be done to validate this hypothesis and clarify the impact of aging on the immunity to electromagnetic interferences.

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