Analysis Study of Sensitive Volume and Triggering Criteria of SEB in Super-Junction MOSFETs

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Abstract

Power MOSFETs are more and more used in atmospheric and space applications. Thus, it is essential to study the influence of the natural radiation environment (NRE) on the electrical behavior of standard and Super-Junction (SJ) MOSFETs. 2D numerical simulations are performed to define the sensitive volume and triggering criteria of SEBs (Single Event Burn-out) for standard and superjunction MOSFETs for different configurations of ionizing tracks. The analysis of the results allows a better understanding of the SEB mechanism in each structure and allows the behaviour and robustness comparison for these two technologies under heavy-ion irradiation.

Keywords: Power MOSFET, Super-Junction MOSFET, SEB, sensitive volume, SOA, TCAD simulations, triggering criteria.

1. Introduction

Power MOSFET is a very important device in many power-electronics applications, widely used in space and atmospheric applications. Its reliability is limited by the effect of natural radiation environment (NRE). This environment is composed of particles of various nature and energy such as heavy ions which can cause the destruction of this device. In order to protect against NRE effects, many studies have been carried out to understand the failure modes. Single Event Burnout (SEB) is one of the catastrophic effects which could cause power devices failure in space systems. Heavy-ions induced destructive failures in power MOSFETs have been extensively studied and are related to the existence of a parasitic bipolar junction transistor (BJT) inherent to the device [1-2]. Destructive electrical failures have already been observed in IGBTs [3], and those induced by heavy ions were highlighted in 1992 and 1993 by Rockwell and Boeing Company [4]. The first adopted triggering criterion was only a critical LET (Linear Energy Transfer) before the influence of the ion penetration depth was investigated. Experimental observation of SEB in high voltage devices such MOSFET and IGBT was reported in [5], demonstrating that avalanche conditions are not needed to trigger the IGBT, a heavy ion being able to induce latchup contrarily to power MOSFETs. SEGR (Single Event Gate Rupture) and SEB testing have been carried out by P.T. McDonald et al [6] on three types of commercial 600-1200V planar IGBTs. These devices are all sensitive to SEB and SEGR but measurements at a reduced V_{CE} value, from 330V to 270V indicated a significant reduction in both measured SEB/SEGR sensitivity allowing their use for space applications.

Currently, the trend is to use rather long ranges, able to cross the epitaxial layer of the classic VDMOS planar-type. S. Liu, however, investigated the range effect on both SEB and SEGR phenomena [7] and recommends the use of light and short-range ions, not to be confused with the appearance of SEGR during SEB tests. Test results carried out on 600 V prototypes show no significant effect of the range on the SEB safe operating area (SOA) (for ranges from 30 to 300 µm), together with Marec et al. who suggest that the criteria is a critical deposited charge in the epitaxy, the latter also defining the sensitive volume [8]. On the other hand, A. Luu et al. show an influence of the ion range in commercial MOSFETs [9]: they define the epitaxial layer as the sensitive volume. We also have reported on the effect of the ion range on 400V- IGBTs [10]. Few works are related to SJ-MOSFET. Huang et al showed that the presence of a horizontal electric field and a smaller vertical electric field in the SJ-device significantly reduce its vulnerability to SEB and SEGR compared to standard power MOSFETs [11]. N.Ikeda et al showed experimentally that there was not much difference in SEB tolerance between the two. However, a better SEB tolerance is obtained by decreasing the die size while maintaining a low on-resistance for SJ-MOSFET and by applying the hardening technique for the standard power MOSFET structure [12]. In 2009 Marina et al. [13] propose a new structure, the 3.3 kV semi-Superjunction Insulated Gate Bipolar Transistor (semi SJ IGBT). Using 2D simulations, these devices show high immunity against cosmic radiations compared to standard FS Trench IGBTs, although they are not used in industry.

In this context, using 2D Synopsis TCAD tools, a simulation work has been conducted to define the sensitive volume and the criteria for SEB triggering induced by heavy ions in standard MOSFET and SJ-

MOSFET devices. The first part of this paper presents the 2D simulation results for the definition of the sensitive volume defined by the minimum LET triggering a SEB, according to the range and depth of ion generation. The analysis of these results also allows comparing the electric behaviour of these cells for different configurations of ionizing tracks. In the second section, the drain voltage has been varied for different ranges in order to define the SOA of these devices**.** Finally, the broad range of temperatures that may occur on a board system necessitates an investigation of the temperature dependence of the SEB mechanism in each component.

2. Simulation tool and test vehicle

Simulations were carried out with 2D Sentaurus simulator using the heavy-ion model. The physics models used are:

•Mobility models: Electrical field, doping and carrier-carrier scattering effects.

•Generation /Recombination models: Auger generation and recombination, SRH and Impact Ionization models.

•Electronic Band structures: Band gap narrowing effects, Intrinsic density and Fermi stats.

Structures under study are standard MOSFET (VDMOS) and SJ-MOSFET power devices as shown in Figure 1: they are based on a flexible technology developed at LAAS laboratory and are rated for a breakdown voltage of 700~800 V. Figure 1 shows a cross-section of the half-cell structures.

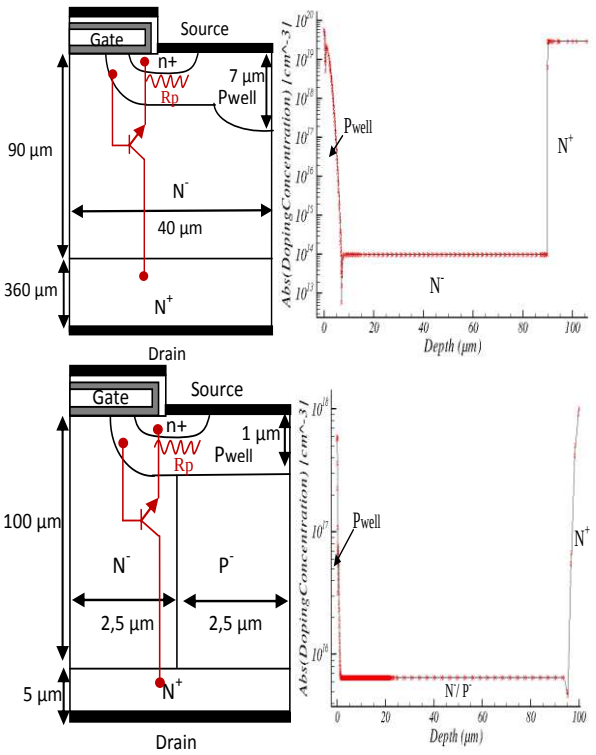

Fig. 1. Standard (top), SJ (bottom) MOSFETs half cell layout and doping profile of each cell (right).

Conditions of simulations

In a first step, all traces of ionization are generated vertically in the half-cell structure from different positions (x), in order to determine the most sensitive one along the x axis.

In a second step we studied the case of ions generated vertically in the volume of the half-cell of standard and SJ MOSFETs with track lengths of 10 µm generated from different depths within the epitaxial region (see Fig 2.a). The objective is to locate the sensitive volume.

In a third step, we simulated the impact of ions penetrating from the front side with different track lengths (see Fig 2.b). The aim is to see from which LET value SEB triggering is initiated for each range and how each component behaves for different range values. Initially, for easier comparison of the results, all simulations are performed at the same drain polarization of 400 V in blocking state. The horizontal x-position of the generation is the one defined in the first simulation step (in this kind of studies the word "range" indicates the track length).

In a fourth step, we simulated these structures with different drain voltages (100 V, 200 V, 300 V and 400 V) for various ranges (10 µm, 30 µm and 60 µm) while keeping the same conditions defined in the preceding second simulation step.

Finally, the temperature dependence of the model is taken into account to simulate the structures with a temperature rise from 300 K to 400 K.

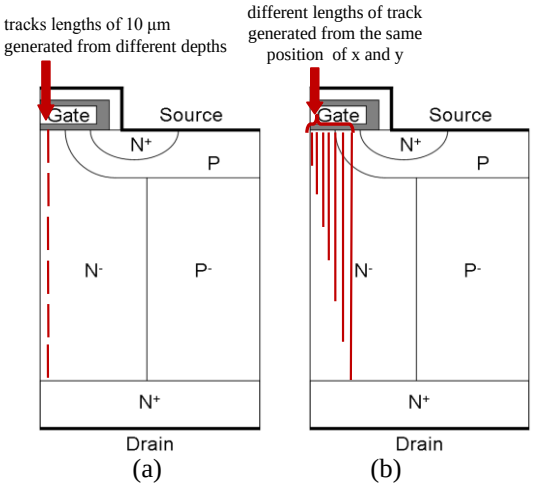

Fig. 2. Schematic of ionizing tracks impacting on normal incidence on the device front side

3. Sentaurus-TCAD simulation results and discussion

3.1. Determination of the Sensitive Volume in each device

For both MOSFET structures and a 400V bias, figure 3 shows the minimum LET triggering a SEB for ions generated from different impact positions along the x axis (see arrows position).

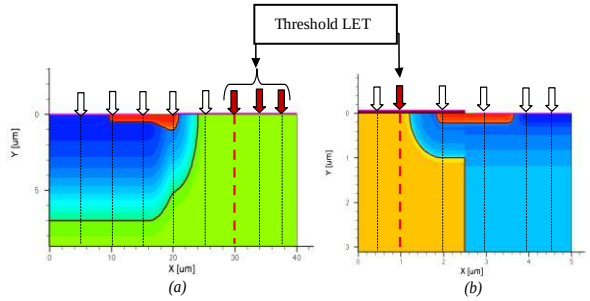

Fig. 3. Minimum LET triggering a SEB in VDMOS (a) and SJ-MOSFET (b) for various impact position (x = variable, y = 0, range = 10µm, V_{DS} = 400 V)

In both cases, the most sensitive areas are generally located in the intercellular region, more specifically between 30 and 38 µm in VDMOS and at 1µm in the SJ-MOSFET (see the positions of colored arrows in Figure 3). These regions are the main areas of the base current for the parasitic vertical transistor. The P+ region having a large capacity of charge collection, the sensitivity of the highly doped region decreases. These simulation results are consistent with those obtained in various studies as much for simulations as experiments [2, 11, 14 and 15]. According to our previous simulations, we have fixed the impact positions at 30 µm for the VDMOS and 1 µm for the SJ-MOSFET (see the dashed line location for each structure in Figure 3).

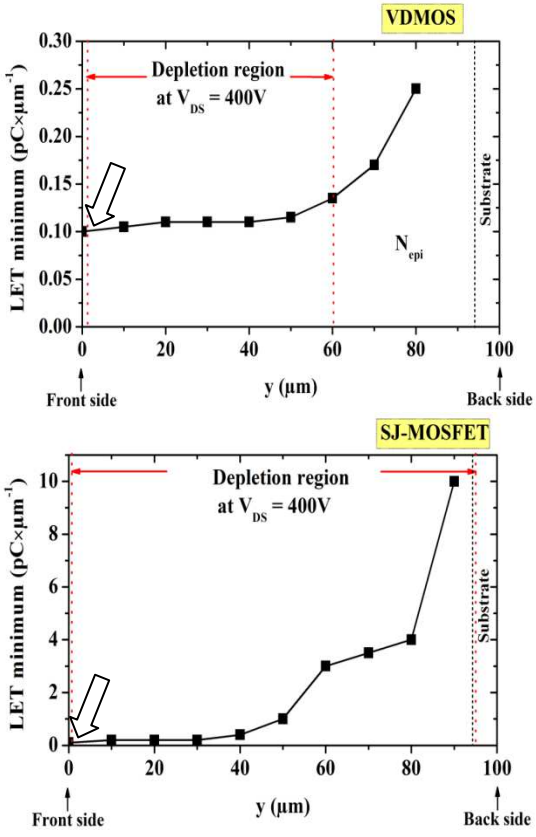

Fig. 4. Minimum LET triggering a SEB of the ion coming from the front side in normal incidence generated from different depths in the epitaxial region with (range=10 µm, Vds=400 V) for standard (top) and SJ (bottom) MOSFETs

Considering a track length of 10 µm separately, for a 400 V bias, the space charge region expands across less than 50 µm. Figure 4 clearly shows that the tracks located inside this area require lower LET values and they vary relatively little between each depth. For the standard MOSFET, the tracks positioned outside the space charge region require a much larger LET. Indeed, in this case, a single type of carrier (holes) is at the origin of the multiplication through the electric field area (see Figure 5- top) and the charges need more time to recombine before reaching the electric field region. As a result, there are likely fewer holes and electrons available to begin the impact ionization cascade.

For SJ-MOSFET, all traces are located within the space charge region that extends horizontally and which occupies the entire cell. Electrons and holes are at the origin of the impact multiplication phenomena in crossing the electric field zone whatever the depth (see Figure 5 bottom).

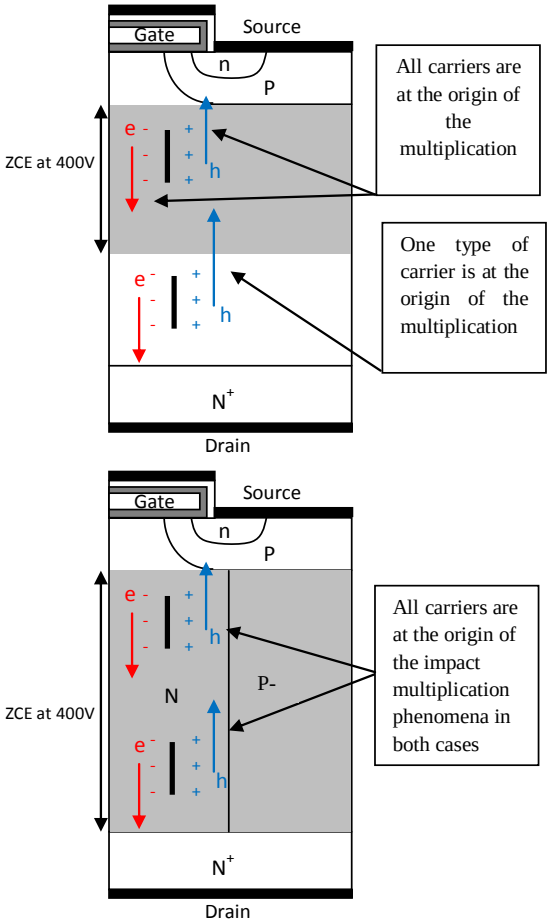

Fig. 5. Traces positioned at two different depths in a VDMOS (top) and SJ-MOSFET (bottom)

One can see, from the analysis of these results, that the most efficient way to trigger a SEB in standard MOSFET is to deposit a quantity of charges into the space charge region. In the SJ-MOSFET the sensitive volume is located in the top half of the epitaxial region. In this case, the electric field is distributed

homogeneously along the vertical PN junction, and the sensitive volume can be independent of its effect. We remind that electrons and holes are collected at drain and source contacts respectively. Generally, in order for the carrier density to be multiplied by the impact ionization mechanism, carriers need to cover a certain distance to acquire the required energy for creating an electron–hole pair [16]. The more carriers travel into the space charge region, the more they are multiplied. Moreover, in SJ-MOSFET all carriers are at the origin of the impact multiplication phenomena in crossing the space charge region. But the tracks positioned in the bottom half of the epitaxial region require a much larger LET since the holes generated in this depth have more time to recombine before reaching the ground via the lateral p-base region.

Figure 6 shows the minimum LET triggering a SEB as a function of the ion range for both components. The simulations show that the LET required for SEB initiation decreases with increasing ion range in the N-epitaxial region. A minimum LET saturation exists for 50 µm in planar MOSFET and 80 µm in SJ-MOSFET. These ion range values correspond to the depth of the space charge region at 400 V for both cells. A high range allows the generation of carriers by avalanche in the space charge region and therefore requires a low LET. Conversely, a small range requires a large LET since the path of charges deposited in the space charge region is lower and there is less generation by the avalanche phenomenon. Therefore, the sensitive case of SEB triggering is when the ion penetrates a great part of the space charge region. A minimum charge exists for ranges lower than 50 µm in planar MOSFET, 20 µm and 80 µm in SJ-MOSFET. With a same LET whatever the increase in range, minimum charges triggering a SEB are systematically deposited within the space charge region thus explaining the LET saturation in standard MOSFET. This is not the case for the SJ-MOSFET wherein there is no LET saturation since the space charge region expands completely into the structure. However in SJ-MOSFET, values of minimum LET vary relatively little between each range, excepted for the 10µm-range. Therefore, the range has a little effect in SJ-MOSFET compared with the standard one.

The SEB mechanism is linked to the avalanche and the forward biasing of the parasitic bipolar transistor, both providing charges to each other. For the SEB phenomenon to become irreversible, the avalanche and conduction mechanisms of the bipolar transistor must be maintained so that the avalanche has to be supplied by the electron current provided by the bipolar transistor and the parasitic transistor has to be supplied by the hole current coming from the avalanche mechanism. For a better understanding, the basic mechanisms involved in the SEB triggering are detailed, for example, in [17] for the standard power MOSFET and in [18] for the SJ-MOSFET.

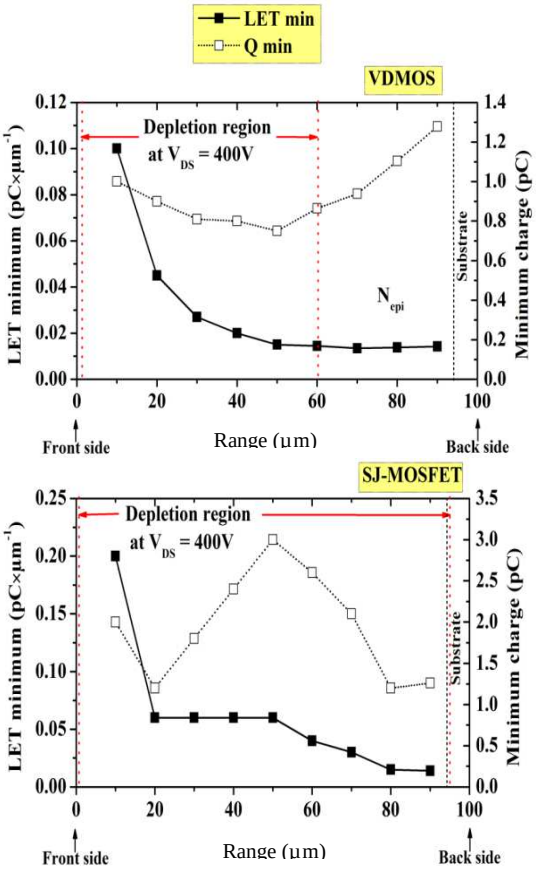

Fig. 6. Minimum LET and quantity of charges triggering a SEB depending on the penetration depth of the ion coming from the front side in normal incidence (Vds=400 V) for standard (top) and SJ (bottom) MOSFETs

Figure 7 illustrates a systematic observation of the simulated electric field evolution following a burnout, showing that the electric field is always maximum at the P^+ body/ N^- drift junction at the end of the simulation whatever the range in the standard MOSFET. This is due to the highly localized current in the right side of each structure i.e. most of the current flows through the inherent parasitic npn transistor (n^+ cathode/p^- body/ n^- drift). The electric field is also maximum at the homo-junction (n^- drift/n^+ substrate) at the end of the simulation whatever the range in the planar and SJ-MOSFETs. This allows the establishment of a strong avalanche rate since the ionization coefficients are exponentially related to the electric field. The currents thus generated lead to thermal runaway and burnout [9].

The displacement of the electric field peak and its increase at the junction in each case, as shown in Figure 7,-are due to the Kirk effect [19, 20] and the build-up of a negative space charge region. Thus, a track with high range will be more susceptible to the Kirk effect for the establishment of a current than a limited and localized charge deposition. For standard MOSFET the slopes of the electric field are different between the two range values due to the collection of charges deposited in each case. While for SJ-MOSFET, the electric field level decreases before the t_{final} only along the trace. The

modification of the electric field compared to the evolution of the injection is described by the Poisson's equation:

VDMOS

$$\frac{dE}{dx} = \frac{q}{\varepsilon}(N_d - n(x)) = \frac{q}{\varepsilon}\left(N_d - \frac{J_n}{qv_n}\right) \qquad \textit{Eq-1}$$

SJ – MOSFET

$$\begin{cases} \dfrac{dE}{dy} = \dfrac{q}{\varepsilon}(N_d - n(y)) = \dfrac{q}{\varepsilon}\left(N_d - \dfrac{J_n}{qv_n}\right) \\ \dfrac{dE}{dx} = 0 \end{cases} \qquad \textit{Eq-2}$$

These equations can explain the observations in Figure 7, i.e. the inverse of the slope of the electric field and the displacement of the peak of the P/N_{epi} junction to the N_{epi} / substrate junction. Indeed, with the contribution of the trace, the carrier density J_n increases as the term J_n/qv_n becomes greater than the N_d doping layer of N_{epi}. In the standard MOSFET, the electric field will rapidly become maximum at the N_{epi}/substrate junction for a track crossing a large part of the epitaxial region (Figure 7, VDMOS range = 70 microns):an important range is more favorable to the Kirk effect for the establishment of a current J_n than a deposit of punctual charges compared to low penetrations. For the SJ-MOSFET structure, the Kirk effect can only occur horizontally (y) because there is no variation of the electric field in the direction of the ion penetration (x), which explains the minor effect of the range in this case. Overall, for these two structures, the influence of the range can be explained only by the Kirk effect: in the case where carriers increase regeneratively until their concentrations, the displacement of the electric field (see Figure 7) with the current density flowing through the space charge region become much higher than the doping of the epitaxial region [9], [21].

For short ranges, the electric field peak moves from the P-body/N-drift junction to the substrate side. However, this does not extend to the case of long ranges where the electric field peak appears at the N-drift/substrate junction since the beginning. So the avalanche (arrow 1 in figure. 8) and burnout triggering (arrow 2 in figure. 8) appear rapidly after the first current peak (schematized by the vertical dotted line in figure. 8) for the higher penetration, while the shorter tracks take more time after this peak.

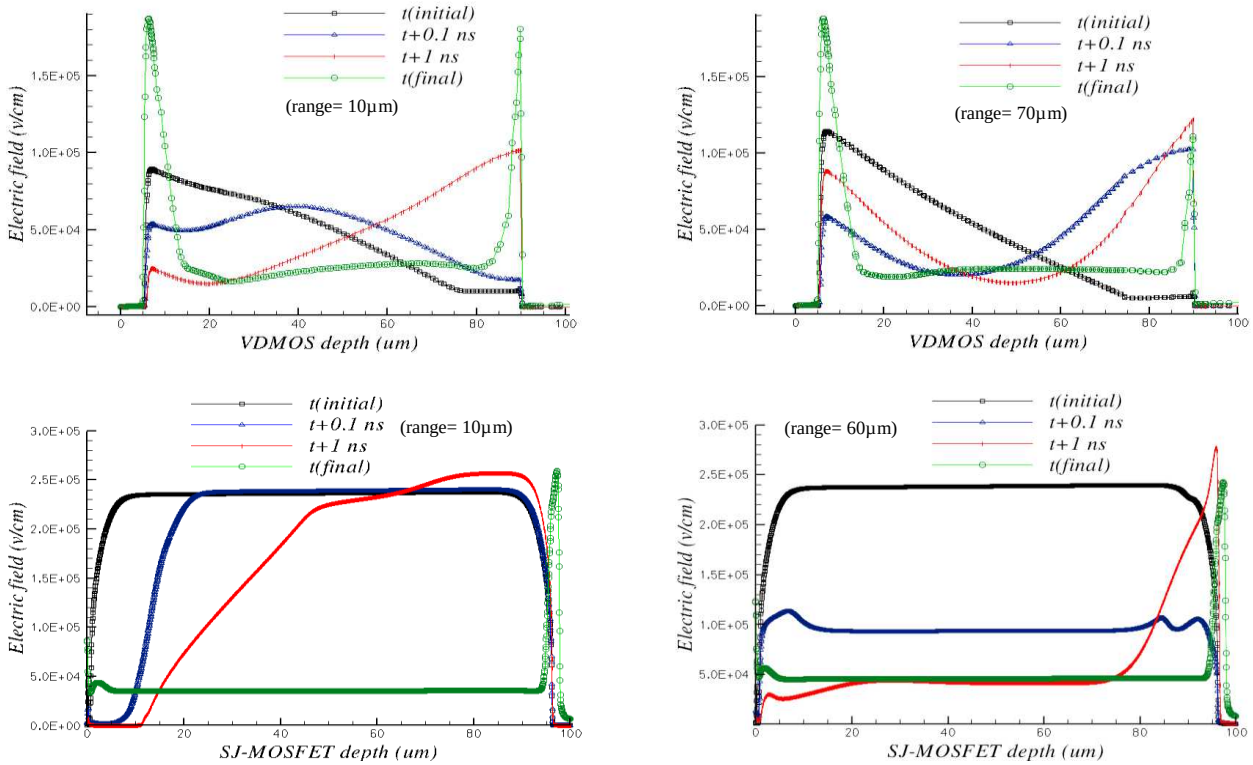

Fig. 7. Evolution of the electric field following a vertical ionizing impact with a high range (left) and small range (right) in each half cell biased at 400 V.

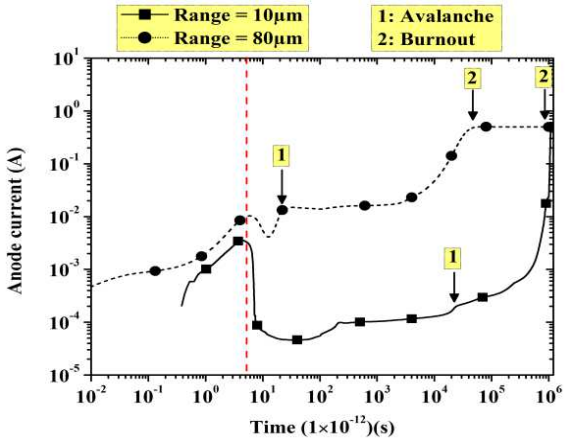

Fig. 8. Evolution of the I_{DS} current as a function of the time following an ion strike at 3 ps for short and long ranges

3.2. Results analysis for different drain-source biases

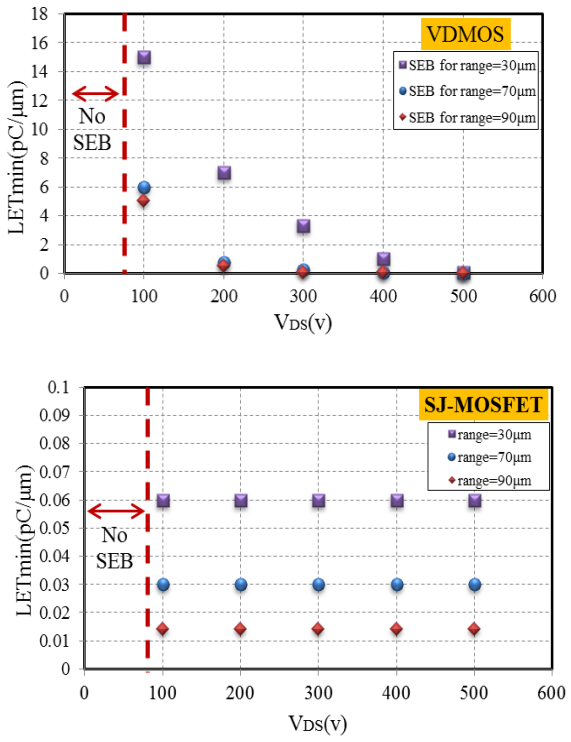

Fig. 9. Minimum LET triggering a SEB at different Vds and various ranges for the ion coming from the front side in normal incidence for standard (top) and SJ (bottom) MOSFETs

Simulation results concerning the minimum LET triggering a SEB for different drain-source biases (100 V, 200 V, 300 V and 400 V) and for three ranges (10 µm, 30 µm and 60 µm) are reported on figure 9. In these cases, the space charge region proportionally extends to each bias. The threshold LET decreases accordingly with the bias increase in the standard MOSFET while the minimum LET triggering a SEB is independent of the bias voltage value for the SJ-MOSFET. Some of the observations previously made are confirmed: LET decreases with the range increase whatever the bias voltage value. For standard MOSFET, the bias voltage increase proportionally extends the space charge region within the cell thus reducing the LET discrepancy between the various ranges. However for the SJ-MOSFET, the LET discrepancy is the same regardless of the bias voltage since as we said previously, the electric field is distributed homogeneously along the vertical PN junction and the space charge region expands completely in the cell.

There is no important difference in the SEB threshold voltage as shown in figure 9. The SJ-MOSFET has a same SOA than the standard one that is consistent with the fact that these structures have the same parameters such as "Rp", the P-well resistance under the source, which is the crucial factor for increasing the SEB threshold voltage.

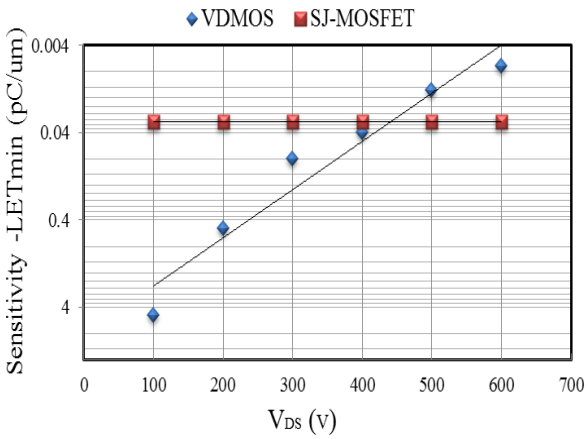

Fig. 10. Comparison of minimum LET triggering a SEB at different V_{DS} for a range of 70µm

Figure 10 summarizes the sensitivity variation for the two structures for an ion penetrating 70 µm into the epitaxial region. The sensitivity evolution depends on the applied bias voltage:

- Under a low bias voltage (<400 V), SJ-MOSFET is more sensitive than the standard one;
- At 400 V, the sensitivity is similar for both devices;

- Under high bias voltage (>400V), the standard MOSFET is more sensitive than the SJ-MOSFET.

This may be the reason why S. Huang et al. In [11] found that the SJ-MOSFET is less vulnerable to the SEB than the standard one. But N. Ikeda et al [12] demonstrated that there was no structural advantage in SEB tolerance for the SJ-MOSFET and there was not much difference in SEB tolerance between the two technologies.

3.3. Results Analysis for different temperature values

Figure 11 clearly shows that the minimum LET required to generate a SEB decreases as the temperature increases: the most critical case is found at low temperature that is consistent with previous works [22].

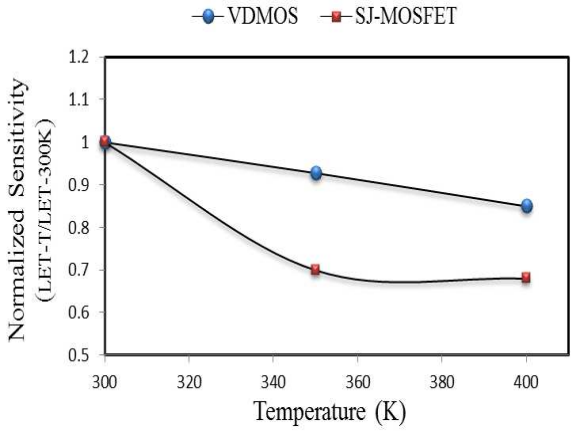

Fig. 11. Comparison of the sensitivity at different temperature value (minimum LET (T)/LET (T°)) with ion range=70µm

For both devices, the impact ionization rate (number of electron-hole pairs generated per unit path length) decreases with increasing temperature [23]. This is attributed to the shorter mean free path of the carriers. Since the impact ionization rate is used explicitly in the solution to the Poisson equation, the generated avalanche hole current density decreases with increasing temperature for the same injected electron current density and applied drain-source bias.

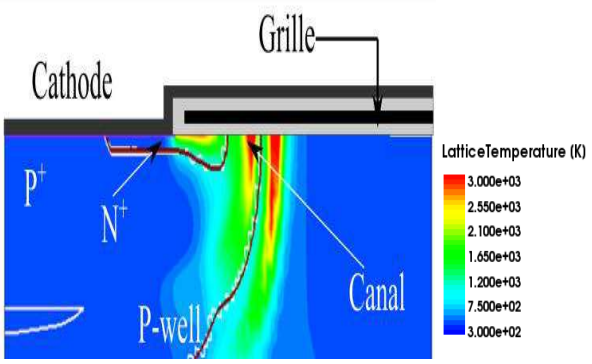

Fig. 12: Temperature distribution after SEB

In both cases the area of the fusion is located at the canal where the temperature can exceed 3000 K, because of the very high current density in this region and the high thermal resistivity of the oxide. Figure 12 shows the temperature distribution following a SEB in the end of simulation for a standard structure.

4. Conclusion

The sensitive volume of SEB for standard and SJ MOSFETs has been defined by delimiting its depth and thickness using 2D electrical simulations. The most critical case for triggering a SEB at 400V in standard MOSFET is related to an ion crossing the entire space charge region. However for SJ-MOSFET, the lowest LET triggering a SEB is obtained for an ion crossing the entire epitaxial region. The ion range has a little effect in SJ-MOSFET compared with the standard one. We also determined the threshold voltage of sensitivity for each structure. SOA is the same for the two studied devices, but there is a significant difference of behaviour and sensitivity as a function of the applied bias voltage. This can be an advantage for the SJ-MOSFET SEB tolerance only at high voltage. Finally, we have shown the influence of the temperature on the sensitivity revealing that the most critical case is found at low temperature in both cases.

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