



**HAL**  
open science

## Analysis study of sensitive volume and triggering criteria of SEB in super-junction MOSFETs

Moustafa Zerarka, Patrick Austin, Frédéric Morancho, Karine Isoird,  
Houssam Arbess, Josiane Tasselli

### ► To cite this version:

Moustafa Zerarka, Patrick Austin, Frédéric Morancho, Karine Isoird, Houssam Arbess, et al.. Analysis study of sensitive volume and triggering criteria of SEB in super-junction MOSFETs. International Seminar on Power Semiconductors (ISPS 2012), Aug 2012, Pragues, Czech Republic. 6 p. hal-01005688

**HAL Id: hal-01005688**

**<https://hal.science/hal-01005688>**

Submitted on 13 Jun 2014

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# Analysis Study of Sensitive Volume and Triggering Criteria of SEB in Super-Junction MOSFETs

M. Zerarka<sup>1,3</sup>, P. Austin<sup>1,2</sup>, F. Morancho<sup>1,2</sup>, K. Isoird<sup>1,2</sup>, H. Arbess<sup>1,3</sup>, J. Tasselli<sup>1,3</sup>

<sup>1</sup>CNRS, LAAS, 7 avenue du colonel Roche, F-31400 Toulouse, France

<sup>2</sup>Univ de Toulouse, UPS, LAAS, F-31400 Toulouse, France

<sup>3</sup>Univ de Toulouse, LAAS, F-31400 Toulouse, France

## Abstract

*Power MOSFETs are more and more used in atmospheric and space applications. Thus, it is essential to study the influence of the natural radiation environment (NRE) on the electrical behavior of standard and Super-Junction (SJ) MOSFETs. 2D numerical simulations are performed to define the sensitive volume and triggering criteria of SEBs (Single Event Burn-out) for standard and superjunction MOSFETs for different configurations of ionizing tracks. The analysis of the results allows a better understanding of the SEB mechanism in each structure and allows the behaviour and robustness comparison for these two technologies under heavy-ion irradiation.*

**Keywords:** Power MOSFET, Super-Junction MOSFET, SEB, sensitive volume, SOA, TCAD simulations, triggering criteria.

## 1. Introduction

Power MOSFET is a very important device in many power-electronics applications, widely used in space and atmospheric applications. Its reliability is limited by the effect of natural radiation environment (NRE). This environment is composed of particles of various nature and energy such as heavy ions which can cause the destruction of this device. In order to protect against NRE effects, many studies have been carried out to understand the failure modes. Single Event Burnout (SEB) is one of the catastrophic effects which could cause power devices failure in space systems. Heavy-ions induced destructive failures in power MOSFETs have been extensively studied and are related to the existence of a parasitic bipolar junction transistor (BJT) inherent to the device [1-2]. In IGBTs, destructive electrical failures have already been observed [3], and those induced by heavy ions were observed in 1992 and 1993 by Rockwell and Boeing Company [4]. The first adopted triggering criterion was only a critical LET (Linear Energy Transfer) before the influence of the ion penetration depth was investigated. Experimental observation of SEB in high voltage devices MOSFET and IGBT was reported in [5], demonstrating that avalanche conditions are not needed to trigger the IGBT, a heavy ion being able to induce latchup contrarily to power MOSFETs. SEGR (Single Event Gate Rupture) and SEB testing have been carried out by P.T. McDonald et al [6] on three types of commercial 600-1200V planar IGBTs. They found that they are all sensitive to SEB and SEGR but measurements at a reduced  $V_{CE}$  value, from 330V to 270V indicated a significant reduction in both measured SEB/SEGR sensitivity allowing to use them in space applications.

Currently, the trend is to use rather long ranges, able to cross the epitaxial layer of the classic VDMOS planar-type. S. Liu, however, investigated the range effect on both SEB and SEGR phenomena [7] and recommends the use of light, short-range ions, not to be confused with the appearance of SEGR during SEB tests. The test results carried out on 600 V prototypes show no significant effect of the range on the SEB safe operating area (SOA) (for ranges from 30 to 300  $\mu\text{m}$ )-, together with Marec et al. in [8] which suggest that the criteria is a critical deposited charge in the epitaxy, the latter defining also the sensitive volume. On the other hand, A. Luu et al. in [9] show an influence of the ion range in commercial MOSFETs; they define the epitaxial layer as the sensitive volume. We also have reported on the effect of the ion range on 400V- IGBTs [10]. Few works are related to SJ-MOSFET. Huang et al showed that the presence of the horizontal electric field and the smaller vertical electric field in the SJ-device reduce its vulnerability to SEB and SEGR significantly compared to the standard power MOSFET [11]. N. Ikeda et al showed experimentally that there was not much difference in SEB tolerance between the two. However, SJ-MOSFET could have better SEB tolerance by decreasing the die size while maintaining low on-resistance and applying the hardening technique for the standard power MOSFET structure [12].

In this context, using 2D Synopsis TCAD tools, a simulation work has been conducted to define the sensitive volume and the criteria for SEB triggering induced by heavy ions in standard MOSFET and SJ-MOSFET devices. The first part of this paper presents the 2D simulation results for the definition of the sensitive volume defined by the minimum LET triggering a SEB, according to the range and depth of ion generation. The analysis of these results also allows

comparing the electric behaviour of these cells for different configurations of ionizing tracks. In the second section, the drain voltage has been varied for different ranges in order to define the SOA of these devices. Finally, the broad range of temperatures that may occur on a board system necessitates an investigation of the temperature dependence of the SEB mechanism in each component.

## 2. Simulation tool and test vehicle

Simulations were carried out with 2D Sentaurus simulator using the heavy-ion model. The physics models used are:

- Mobility models: Electrical field, doping and carrier-carrier scattering effects.
- Generation /Recombination models: Auger generation and recombination, SRH and Impact Ionization models.
- Electronic Band structures: Band gap narrowing effects, Intrinsic density and Fermi stats.

Structures under study are standard MOSFET (VDMOS) and SJ-MOSFET power devices as shown in Figure 1: they are based on a flexible technology developed at LAAS laboratory and are rated for a breakdown voltage of 700~800 V. Figure 1 shows a cross-section of the half-cell structures.

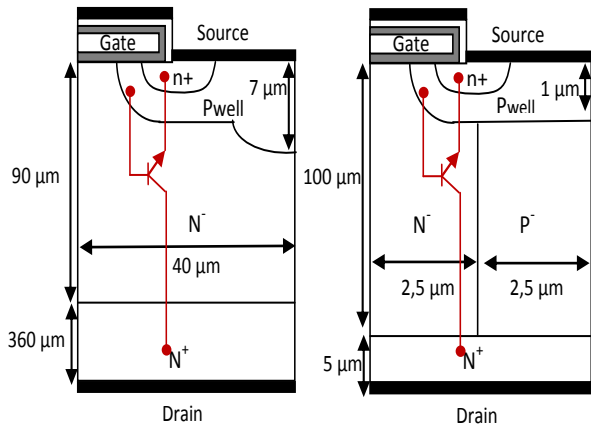


Fig 1. Standard and SJ MOSFETs half cell layout.

### Conditions of simulations

Throughout these simulations, all ionization traces are only generated in the intercellular region right next to the channel. This position is the most sensitive as shown in previous works [5-7]. In a first step, we studied the case of ions generated vertically in the volume of the half-cell of standard and SJ MOSFETs with track lengths of 10 μm generated from different depths within the epitaxial region (see Fig 2.a). The objective is to locate the sensitive volume.

In a second step, we simulated the impact of ions penetrating from the front side with different track lengths (see Fig 2.b). The aim is to see from which value of LET SEB triggering is initiated for each range and how each component behaves for different values of

range. Initially, for easier comparison of the results, all simulations are performed at the same drain polarization of 400 V in blocking state. The horizontal x-position of the generation is the one defined in the first step simulation (range is the word used in this type of studies to indicate the track length).

In a third step, we simulated these structures with different drain voltages (100 V, 200 V, 300 V and 400 V) for various ranges (10 μm, 30 μm and 60 μm) while keeping the same conditions defined in the preceding second step simulation.

Finally, the temperature dependence of the model is taken into account to simulate the structures with a temperature rise from 300 K to 400 K.

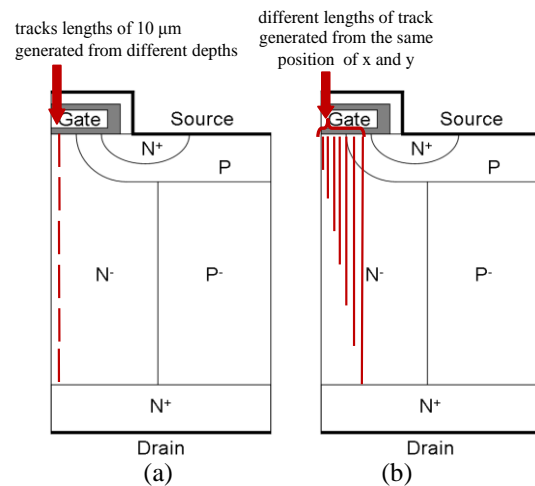


Fig 2. Schematic of ionizing tracks impacting on normal incidence on the device front side

## 3. Sentaurus-TCAD simulation results and discussion

### 3.1. Determination of the Sensitive Volume in each device

Considering a track length of 10 μm separately, for a 400 V bias, the space charge region expands across less than 50 μm. Figure 3 clearly shows that the tracks located inside this area require lower values of LET and they vary relatively little between each depth. Outside the space charge region, the tracks require a much larger LET since only one type of carrier, holes, is at the origin of the impact multiplication phenomena within the electric field zone. Moreover, the charges located outside the depletion region need more time to recombine before reaching the electric field region. As a result, there are likely fewer holes and electrons available to begin the impact ionization cascade.

One can see, from the analysis of these results, that the most efficient way to trigger a SEB in standard MOSFET is to deposit a quantity of charges into the space charge region. In the SJ-MOSFET the sensitive volume is located in the top half of the epitaxial region. In this case, the electric field is distributed homogeneously along the vertical PN junction, and the sensitive volume can be independent of its effect. We

remind that electrons and holes are collected at drain and source contacts respectively. Generally, in order for the carrier density to be multiplied by the impact ionization mechanism, carriers need to cover a certain distance to acquire the required energy for creating an electron–hole pair [13]. The more carriers travel in the space charge region, the more they are multiplied. Moreover, in SJ-MOSFET all carriers are at the origin of the impact multiplication phenomena in crossing the space charge region. But the tracks positioned in the bottom half of the epitaxial region require a much larger LET since the holes generated in this depth have more time to recombine before reaching the ground via the lateral p-base region.

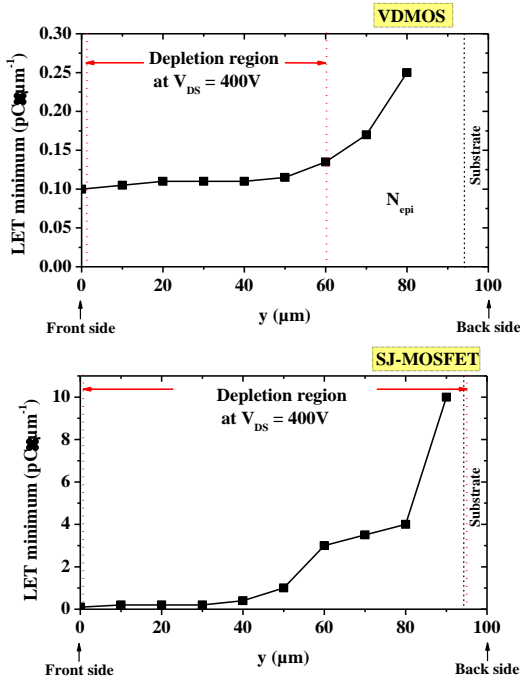


Fig. 3. Minimum LET triggering a SEB of the ion coming from the front side in normal incidence generated from different depths in the epitaxial region with (range=10  $\mu\text{m}$ ,  $V_{\text{ds}}=400\text{ V}$ ) for planar (top) and SJ (bottom) MOSFETs

Figure 4 shows the minimum LET triggering a SEB as a function of the ion range for both components. The simulations show that the LET required for SEB initiation decreases with increasing ion range in the N-epitaxial region. A minimum LET saturation exists for 50  $\mu\text{m}$  in planar MOSFET and 80  $\mu\text{m}$  in SJ-MOSFET. These ranges correspond to the depth of the space charge region which width is 50  $\mu\text{m}$  and 80  $\mu\text{m}$ , respectively, at 400 V for both cells. An important range allows the generation of carriers by avalanche in the space charge region and therefore requires a low LET. Conversely, a small range requires a large LET since the path of charges deposited in the space charge region is lower and there is less generation by the avalanche phenomenon. Therefore, the sensitive case of SEB triggering is when the ion penetrates a great part of the space charge region. A minimum charge exists for ranges lower than 50  $\mu\text{m}$  in planar MOSFET, 20  $\mu\text{m}$  and 80  $\mu\text{m}$  in SJ-MOSFET. It is clear that with the same LET whatever the increase in range, minimum charges triggering a SEB are

systematically deposited minimum charges triggering a SEB are systematically deposited within the space charge region which explains the saturation of LET in standard MOSFET. This is not the case for the SJ-MOSFET wherein there is no saturation of LET since the space charge region expands completely into the structure. However in SJ-MOSFET, values of minimum LET vary relatively little between each range excepted for the 10 $\mu\text{m}$ -range. Therefore, the range has a little effect in SJ-MOSFET compared with the standard one.

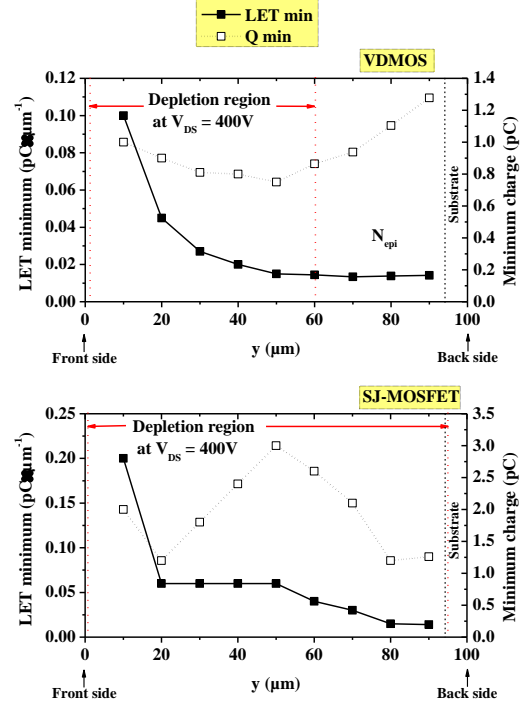


Fig. 4. Minimum LET and quantity of charges triggering a SEB depending on the penetration depth of the ion coming from the front side in normal incidence ( $V_{\text{ds}}=400\text{ V}$ ) for planar (top) and SJ (bottom) MOSFETs

The track range influence on the SEB phenomenon can be explained by the following. The SEB mechanism is linked to the avalanche one and the forward biasing of the parasitic bipolar transistor which provides charges to each other. For the SEB phenomenon to become irreversible, the avalanche and conduction mechanisms of the bipolar transistor must be maintained so that the avalanche has to be fed by the electron current provided by the bipolar transistor and the parasitic transistor has to be fed by the hole current coming from the avalanche mechanism. Figure 5 illustrates a systematic observation of the electric field in the simulated structures following a burnout showing that the electric field is always maximum at the  $\text{P}^+$  body/ $\text{N}^-$  drift junction at the end of the simulation, whatever the range in the standard MOSFET. This is due to the highly localized current in the right side of each structure i.e. most of the current flows through the inherent parasitic npn transistor ( $\text{n}^+$  cathode/ $\text{p}^+$  body/ $\text{n}^-$  drift). The electric field is also maximum at the homo-junction ( $\text{n}^-$  drift/ $\text{n}^+$  substrate) at the end of the simulation, whatever the range in the planar and SJ-MOSFETs. This electric field allows the establishment of a strong avalanche rate since the

ionization coefficients are exponentially related to the electric field. The currents thus generated lead to thermal runaway and burnout [9].

The displacement of the electric field peak and its increase at the junction in each case as shown in Figure 5 are due to the Kirk effect [14, 15] and the build-up of a negative space charge region. Thus, a track with high range will be more susceptible to the Kirk effect for the establishment of a current than a limited and localized

charge deposition. Observations show also that in the case of low range, the electric field peak moves from P<sup>-</sup> body junction to the substrate junction. However, this does not extend to the case of high range hence the maximum reached by the electric field at the n-drift/substrate junction appears from the outset. This explains the rapidity of SEB triggering in the case of high range after each first current peak, the low range taking more time after this latter.

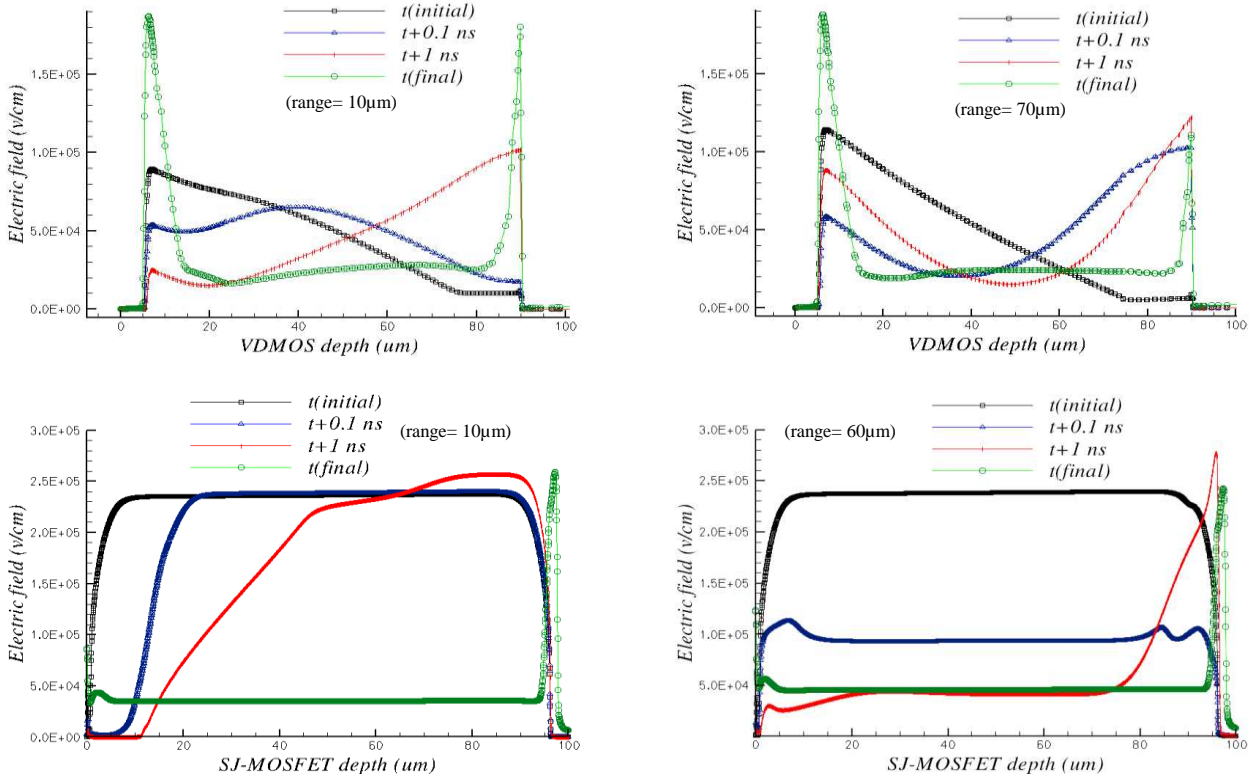


Fig. 5. Evolution of the electric field following a vertical ionizing impact with a big range (left) and small range (right) in each half cell biased at 400 V.

### 3.2. Results analysis for different drain-source biases

Figure 6 presents the simulation results for different drain-source biases (100 V, 200 V, 300 V and 400 V) and for three ranges (10 μm, 30 μm and 60 μm). In these cases, the space charge region proportionally extends to each bias. It is clear that the threshold LET decreases accordingly with the bias increase in the standard MOSFET. On the other hand, the minimum LET triggering a SEB is fixed whatever the bias voltage value for the SJ-MOSFET. Some of the observations previously made are confirmed: LET decreases with the range increase whatever the bias voltage value. However, increasing the bias voltage proportionally extends the space charge region within the cell that reduces the existing differences of LET between the various ranges in the case of standard MOSFET. However for the SJ-MOSFET, the differences of LET between the various ranges is the same regardless of the bias voltage since as we said previously, the electric field is distributed homogeneously along the vertical PN

junction and the space charge region expands completely in the cell.

There is no important difference in the SEB threshold voltage as shown in figure 6. The SJ-MOSFET has a same SOA than the standard one that is consistent with the fact that these structures have the same parameters such as “Rp”, the resistance of the P-well under the source which is the crucial factor for increasing the SEB threshold voltage. Figure 7 summarizes the sensitivity variation for the two structures for an ion penetrating 70 μm into the epitaxial region. The sensitivity evolution depends on the bias voltage applied:

- Under a low bias voltage (<400 V), SJ-MOSFET is more sensitive than the standard one;
- At 400 V, the sensitivity is similar for both devices;
- Under high bias voltage (>400V), the standard MOSFET is more sensitive than the SJ-MOSFET.

This may be the reason why S. Huang et al. In [11] found that the SJ- MOSFET is less vulnerable to the SEB

compared to the standard one. But on the other side N. Ikeda et al [12] demonstrated that there was no structural advantage in SEB tolerance for the SJ-MOSFET and there was not much difference in SEB tolerance between the two technologies.

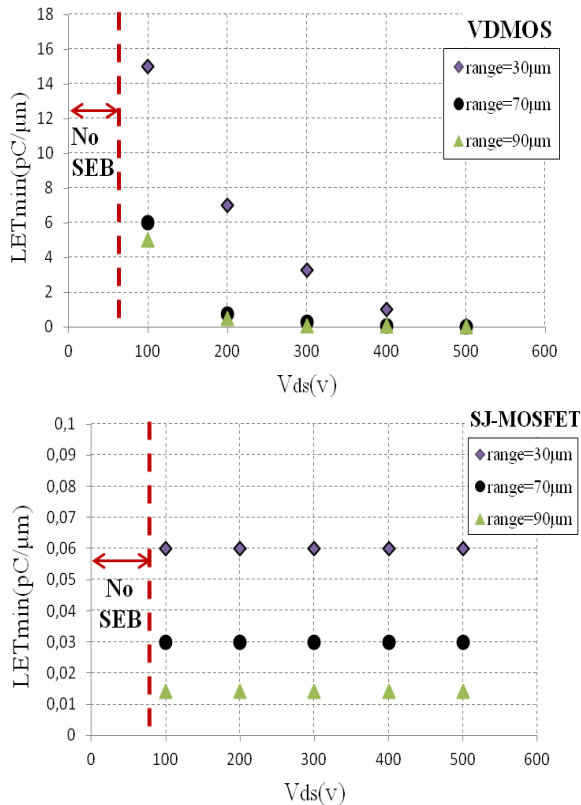


Fig. 6. Minimum LET triggering a SEB at different Vds and various ranges for the ion coming from the front side in normal incidence for standard (top) and SJ (bottom) MOSFETs

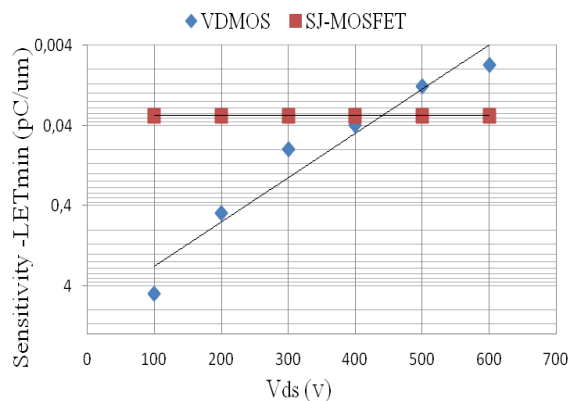


Fig. 7. Comparison of minimum LET triggering a SEB at different Vds for a range of 70μm

### 3.3. Results Analysis for different temperature value

Figure 8 clearly shows that the minimum LET required to generate a SEB decreases as the temperature increases. This is to say, the most critical case found at low temperature which is consistent with previous works [16].

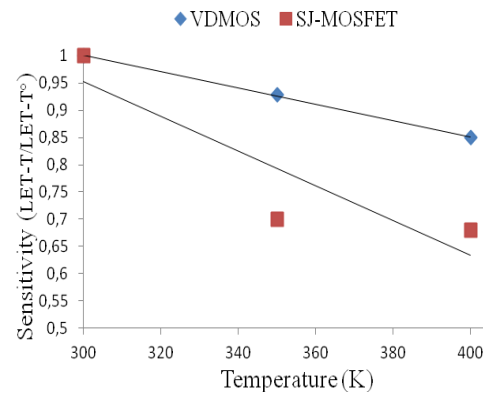


Fig. 8. Comparison of the sensitivity at different temperature value (minimum LET (T)/LET (T°)) with ion range=70μm

For the standard and SJ MOSFETs, the impact ionization rate (number of electron-hole pairs generated per unit path length) decreases with increasing temperature [17]. This is attributed to the shorter mean free path of the carriers. Since the impact ionization rate is used explicitly in the solution to the Poisson equation, the avalanche generated hole current density decreases with increasing temperature for the same injected electron current density and applied drain-source bias.

## 4. Conclusion

The sensitive volume of standard and SJ MOSFETs has been defined by delimiting the depth and thickness of this volume using 2D electrical simulations. The most critical case for triggering a SEB at 400V in standard MOSFET is related to an ion crossing the entire space charge region. However for SJ-MOSFET, the range has a little effect compared with the standard one. SOA is the same for the two studied devices, but there is a significant difference of behaviour and sensitivity depending on the applied bias voltage. This can be an advantage for the SJ-MOSFET SEB tolerance only at high voltage.

## Acknowledgements

This work has been sponsored by Fondation de Recherche pour l'Aéronautique et l'Espace (<http://www.fnrae.org/>) within the framework of EPOPE project.

## References

- [1] J. A.A. Keshavarz, T.A. Fischer, W.R. Dawes and C.F.Hawkins, "Computer Simulations of Ionizing Radiation Burnout in Power MOSFETs", IEEE Trans. Nucl. Sci., vol. 35, No 6, pp 1422-1427, December 1988.
- [2] F. Roubaud, C. Dachs, J.M. Palau, J. Gasiot and P. Tastet, "Experimental and 2D simulation Study of the Single Event Burnout", IEEE Trans. Nucl. Sci., vol. 40, NO 6, pp 1952-1958, eceember 1993.
- [3] N. Iwamuro, et al, "Numerical Analysis of Short-circuit Safe Operating Area for P-channel and N-channel IGBTs", IEEE Elec. Dev. Vol. ED-38 n02, pp. 303-309, feb. 1991.
- [4] D. K. Nichols, et al, "Observations of Single Event Failure in Power MOSFETs", IEEE Data Workshop Record, pp

41-54, July 1994.

- [5] Lorfèvre, E.; Dachs, C.; Detcheverry, C.; Palau, J.-M.; Gasiot, J.; Roubaud, F.; Calvet, M.-C.; Ecoffet, R.; , "Heavy ion induced failures in a power IGBT," IEEE Transactions on Nuclear Science, , vol.44, no.6, pp.2353-2357, Dec 1997
- [6] McDonald, P.T.; Henson, B.G.; Stapor, W.J.; Harris, M.; , "Destructive heavy ion SEE investigation of 3 IGBT devices," Radiation Effects Data Workshop, 2000 , vol., no., pp.11-15, 2000
- [7] S. Liu, J. L. Titus, C. DiCienzo, H. Cao, M. Zafrani, M. Boden, and R. Berberian, "Recommended test conditions for SEB evaluation of planar power DMOSFETs," IEEE Trans. Nucl. Sci., vol. 55, no. 6, pp. 3122–3129, Dec. 2008.
- [8] R. Marec, P. Calvel, and M. Mélotte, "Methodology to predict the SEE rate in vertical MOSFET with deep charge collection," presented at the QCA Days Conf., Villigen, Switzerland, Jan. 2009.
- [9] A. Luu, F. Miller, P. Poirot, R. Gaillard, N. Buard, T. Carriere, P. Austin, M. Bafleur, and G. Sarabayrouse, "Sensitive Volume and Triggering Criteria of SEB in Classic Planar VDMOS" IEEE Trans. Nucl. Sci., vol. 55, no. 4, pp. 2166–2173, Aug. 2008.
- [10] M. Zerarka, P. Austin, M. Bafleur "Comparative study of sensitive volume and triggering criteria of SEB in 600 V planar and trench IGBTs" Microelectronics Reliability, vol. 51, pp. 1990–1994 (2011)
- [11] S. Huang, G. A. J. Amaratunga, Member, IEEE, and F. Udrea, Member, IEEE "Analysis of SEB and SEGR in Super-Junction MOSFETs" IEEE Trans. Nucl. Sci., vol. 47, no. 6, december 2000
- [12] Naomi Ikeda, Satoshi Kuboyama, and Sumio Matsuda "Single-Event Burnout of Super-Junction Power MOSFETs" IEEE Trans. Nucl. Sci., vol. 51, no. 6, december 2004
- [13] S. Kuboyama, N. Ikeda, T. Hirao, and S. Matsuda, "Improved model for single-event burnout mechanism," IEEE Trans. Nucl. Sci., vol. 51, no. 6, pp. 3336–3341, Dec. 2004.
- [14] J. K. Hohl and G. H. Johnson, "Feature of the triggering mechanism for single event burnout of power MOSFETs," IEEE Trans. Nucl. Sci., vol. 36, no. 6, pp. 2260–2266, Dec. 1989.
- [15] G. H. Johnson, J. M. Palau, C. Dachs, K. F. Galloway, and R. D. Schrimpf, "A review of the techniques used for modeling single event effects in power MOSFETs," IEEE Trans. Nucl. Sci., vol. 43, pp. 546–560, 1996.
- [16] G.H. Johnson, Temperature dependence of single-event burnout in NChannel Power MOSFETs, IEEE Trans. Nuc. Sci, Vol 39, No 6, pp. 1605-1612, dec 1992.
- [17] C.R. Crowell and SM. Sze, "Temperature Dependence of Avalanche Multiplication in Semiconductors," Appl. Phys. Let.. vol. 9. pp. 242-244.1966.