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► **To cite this version:**

Loïc Théolier, Karine Isoird, Henri Tranduc, Frédéric Morancho, Jaume Roig Guitart, et al.. Switching Performance of 65 Volts Vertical N-Channel FLYMOSFETs. 8th International Seminar on Power Semiconductors (ISPS'06, Aug 2006, Prague, Czech Republic. pp.117-122. hal-01005674

**HAL Id: hal-01005674**

**<https://hal.science/hal-01005674>**

Submitted on 13 Jun 2014

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# Switching Performance of 65 Volts Vertical N-Channel FLYMOSFETs

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**Abstract :** In this paper, the switching performance of 65 Volts vertical N-channel FLYMOSFETs is investigated for the first time and compared to a conventional VDMOSFET. It is shown that measurements of the different capacitances and the gate charge of the two devices are comparable. A 2D simulation study of two equivalent structures (i.e. FLYMOSFET and VDMOSFET exhibiting the same breakdown voltage) confirms that floating islands did not cause parasitic or new phenomenon, in the case of weakly doped islands.

**Keywords:** capacitance modeling, gate charge, VDMOSFET, FLYMOSFET, power MOSFET.

## INTRODUCTION

In the power electronics field, semiconductor devices are switches operating between the off-state and the on-state. So the breakdown voltage and the on-resistance are two important characteristics of these devices. The P-Floating Islands MOS devices - FLIMOS [1], FLYMOS™ [2], Opposite Doped Buried Regions (ODBR) MOS [3] and FITMOS [4] for example – have recently caught the attention of many researchers because they can offer lower specific on-resistance values than conventional MOSFETs in medium voltage applications (around 600 Volts). It was also shown [1] that they are good challengers of Superjunction devices [5] under 600 Volts; furthermore, the “Floating Islands” concept is not based on the charge compensation principle unlike the Superjunction devices technology [2]. Although a superior FLYMOSFET static performance in comparison with power MOSFET was experimentally demonstrated in [2], no study about its dynamic performance has been done to date.

This work investigates the FLYMOSFET’s dynamic behaviour: in this way, simulations analysis are combined with experimental results to compare the novel device performance with the conventional power VDMOSFET’s one.

## FLOATING ISLANDS PRINCIPLE

Schematic cross-sections of the conventional VDMOSFET and the Vertical FLYMOSFET are shown respectively in Fig. 1-a and 2-a. The main difference is the introduction of a P-buried layer (called Floating

Island) in the N<sup>-</sup> epitaxial layer. In contrast to the conventional VDMOSFET, for which the breakdown voltage is supported at one location (Fig 1-b), the P-buried layer allows the division of the maximal electric field in two parts (Fig. 2-b). When the breakdown voltage is the same, the N<sup>-</sup> epitaxial layer doping concentration of the FLYMOSFET ( $N_{D2}$ ) can be increased compared to the VDMOSFET case ( $N_{D1}$ ), resulting in a reduction of the on-resistance. Nevertheless, the drawback of this increase in doping concentration is the impact that can be expected on the capacitance of the drain depletion layer beneath the gate oxide ( $C_{gddep}$ ) and on the drain-source capacitance ( $C_{ds}$ ) that is the capacitance of two PN junctions in series in the FLYMOSFET’s case (Fig. 2-a).

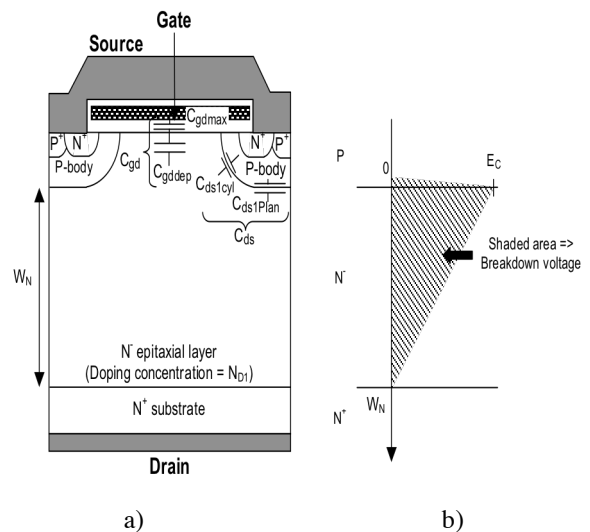


Fig. 1. Conventional VDMOSFET: a) schematic cross-section, b) theoretical electric field distribution at breakdown.

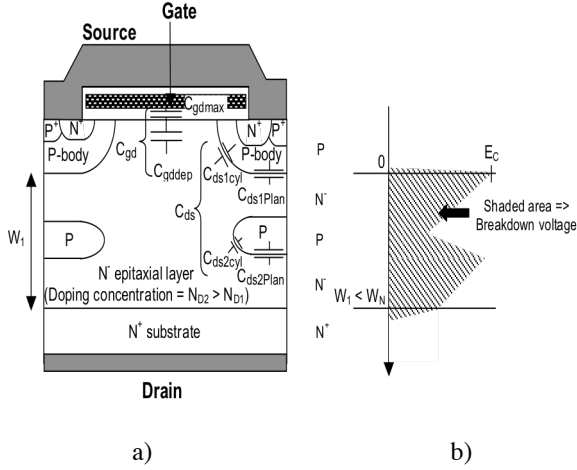


Fig. 2. Vertical FLYMOSFET: a) schematic cross-section, b) theoretical electric field distribution at breakdown.

## DEVICE STRUCTURE

The studied device is a 65V FLYMOSFET fabricated by Alves et al [2]. In previous works, 1D process simulation and crystalline revelation have allowed to reveal some qualitative representations of P-floating islands in order to understand their evolution [6]. But neither process simulation nor 1D physical characterization gave a clear and accurate representation of the islands. Thus, the purpose of creating a physical characterization tool by using Scanning Capacitance Microscopy (Fig. 3) is to determine precisely the shape and the dimensions of the Floating Island to quantify its impact on FLYMOSFET electrical characteristics.

Thanks to SCM, it is possible to quantify directly the 2D island forms and the Floating Island resulting picture exhibits a ball-like shape.

On the contrary to the first theoretical representation [1], in which the islands are thin and long, the SCM results show that islands capacitances are more cylindrical than plane.

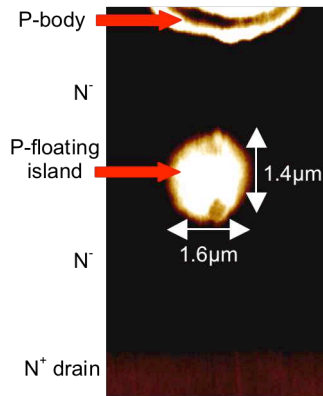


Fig. 3. SCM image of the 65V FLYMOSFET.

## CAPACITANCE EXPRESSIONS

The switching performance of the FLYMOSFET and the conventional VDMOSFET is strongly related to MOSFET capacitances, which are needed to charge and to discharge during switching. FLYMOSFET's capacitances exhibit the same expressions than those of a VDMOSFET; nevertheless, the Floating Islands play a part in drain-source capacitance. All these capacitances depend on geometric and technological parameters of the structure.

### Gate-Drain Capacitance ( $C_{gd}$ ) Modeling

The FLYMOSFET's gate-drain capacitance is comparable to the gate-drain capacitance of a VDMOSFET.

This capacitance is constituted by two capacitances in series: an oxide capacitance ( $C_{gdmax}$ ) and a depletion capacitance ( $C_{gddep}$ ).

- in the accumulation regime, i.e. when  $V_{dg} < 0$ ,  $C_{gd}$  is equal to the oxide capacitance  $C_{gdmax}$ .
- in the depletion (or weak inversion) regime, when  $V_{ds} > V_{gs}$ ,  $C_{gd}$  obeys the following relation:

$$\frac{1}{C_{gd}} = \frac{1}{C_{gdmax}} + \frac{1}{C_{gddep}} \quad (1)$$

where

$$C_{gdmax} = \frac{\epsilon_0 \cdot \epsilon_{ox}}{e_{ox}} \cdot S_1 \quad (2)$$

and

$$C_{gddep} = S_1 \cdot \sqrt{\frac{q \cdot N_D \cdot \epsilon_0 \cdot \epsilon_{si}}{2 \cdot \Phi_s}} \quad (3)$$

$S_1$  represents the inter-cellular total area beneath the gate ( $N^-$  region) and  $\Phi_s$  the voltage that is sustained by the space charge zone.

The main difference between a conventional VDMOSFET and its equivalent FLYMOSFET (i.e. same breakdown voltage and same gate oxide thickness) comes therefore from the doping concentration  $N_D$  of the  $N^-$  region (epitaxial layer) that influences  $C_{gddep}$  (depletion capacitance).

### Drain-Source Capacitance ( $C_{ds}$ ) Modeling

The drain-source capacitance of a VDMOSFET is due to the  $PN^-$  junction which is formed by the P body region and the  $N^-$  epitaxial layer. This junction is constituted by a plane junction ( $C_{ds1Plan}$ ) and a cylindrical junction in parallel ( $C_{ds1cyl}$ ). We can then consider that the analytic model of  $C_{ds}$  is:  $C_{ds} = C_{ds1Plan} + C_{ds1cyl}$ .

The analytical expressions of the  $C_{ds1cyl}$  capacitance is recalled [7]:

$$C_{ds1cyl} = \pi \cdot \epsilon_0 \cdot \epsilon_{si} \cdot z \cdot \left( \frac{V_{ac}}{\alpha \cdot V_{ds}} \right)^{0.426} \quad \text{if } \alpha \cdot V_{ds} > V_{ac} \quad (4)$$

$$C_{ds1cyl} = \pi \cdot \epsilon_0 \cdot \epsilon_{si} \cdot z \cdot \left( \frac{V_{ac}}{\alpha \cdot V_{ds}} \right)^{0.306} \quad \text{if } \alpha \cdot V_{ds} < V_{ac} \quad (5)$$

where  $\alpha$  is the voltage part sustained by the main junction "P-body/N" ( $\alpha = 1$  for the VDMOSFET) and  $z$  is the total "perimeter" of the channel with:

$$V_{ac} = \frac{q \cdot N_D \cdot r_j^2}{4 \cdot \epsilon_0 \cdot \epsilon_{si}} \quad (6)$$

The analytical expression of the cylindrical junction capacitance of the FLYMOSFET is identical to the VDMOSFET's one. The only difference could come from the doping concentration of the epitaxial layer.

Therefore, for a same breakdown voltage, the increase in the doping concentration of the epitaxial layer and  $\alpha$  will increase the value of the  $C_{ds1cyl}$  capacitance of the FLYMOSFET.

The analytical expressions of the  $C_{ds1Plan}$  capacitance is recalled:

$$C_{ds1Plan} = S_2 \cdot \sqrt{\frac{q \cdot N_D \cdot \epsilon_0 \cdot \epsilon_{si}}{2 \cdot \alpha \cdot V_{ds}}} \quad (7)$$

$S_2$  being the total plane surface beneath the P diffusion of channel.

The plane junction capacitance of the VDMOSFET also depend on the  $N^-$  doping concentration epitaxial layer. Concerning the FLYMOSFET, it appears two drift regions in series, due to the P-floating islands located under the plane junction. The expression of the plane capacitance beneath the island is:

$$C_{ds2Plan} = S_3 \cdot \sqrt{\frac{q \cdot N_D \cdot \epsilon_0 \cdot \epsilon_{si}}{2 \cdot (1-\alpha) \cdot V_{ds}}} \quad (8)$$

where  $S_3$  is the surface of the plane junction on top and beneath the island.

Here, the expression of the cylindrical junction is:

$$C_{ds2cyl} = 2 \cdot \pi \cdot \epsilon_0 \cdot \epsilon_{si} \cdot z \cdot \left( \frac{V_{ac}}{(1-\alpha) \cdot V_{ds}} \right)^{0.426} \quad (9)$$

if  $(1-\alpha) \cdot V_{ds} > V_{ac}$

$$C_{ds2cyl} = 2 \cdot \pi \cdot \epsilon_0 \cdot \epsilon_{si} \cdot z \cdot \left( \frac{V_{ac}}{(1-\alpha) \cdot V_{ds}} \right)^{0.306} \quad (10)$$

if  $(1-\alpha) \cdot V_{ds} < V_{ac}$

A higher doping concentration  $N_D$  for the FLYMOSFET must imply a more important value of  $C_{ds1Pdiff}$  compared to the VDMOSFET's one. In compensation, the capacitance  $C_{ds2}$  in series with  $C_{ds1diff}$  would allow a reduction of the resulting capacitance  $C_{ds}$  of the FLYMOSFET in relation to the VDMOSFET.

However, the analytic expressions presented in this paragraph allow to give the switching performance tendencies of the FLYMOSFET. This is not enough to

quantify the evolution of the  $C_{gd}$  and  $C_{ds}$  capacitances precisely. In the continuation, the quantitative evolutions of these two capacitances will be presented.

## RESULTS AND DISCUSSION

The measurements presented in this article have been done on a conventional 45V VDMOSFET and a 65V FLYMOSFET, using the same doping concentration of the  $N^-$  epitaxial layer (around  $10^{16} \text{ cm}^{-3}$ ) but having different active area geometries and different gate oxide thicknesses. The impedancemeter was a HP4284, used at 100 kHz. This frequency allows to free to the model of representation of the complex impedance seen by the impedancemeter.

The temporal and dynamic physical 2D simulations were performed with the ISE TCAD (Integrated Systems Engineering) software. The comparison between simulation and measurements is important in order to validate the models of dynamic behavior and to verify the software performance for these type of structures.

### Gate-Drain Capacitance

Figure 4 presents the gate-drain capacitance measurements for the two structures and the 2D simulation of the FLYMOSFET's gate-drain capacitance.  $C_{gdmax}$  capacitance expression depends essentially on the oxide thickness at reverse bias drain-gate configuration. We have chosen to not represent them on Figure 4. Besides, the weak difference between the curves of the VDMOSFET and the FLYMOSFET seems to be due to the difference of doping concentration of the  $N^-$  epitaxial layer. Indeed, a difference in the doping concentration of the drift zone influences on the depletion of the structure - expression (3) -. So, the comparison of the curves shows that the insertion of a floating island modifies lightly the gate-drain capacitance.

2D simulations of the FLYMOSFET are in good agreement with measurements: we can validate our simulations with these models and the mesh used in our simulations.

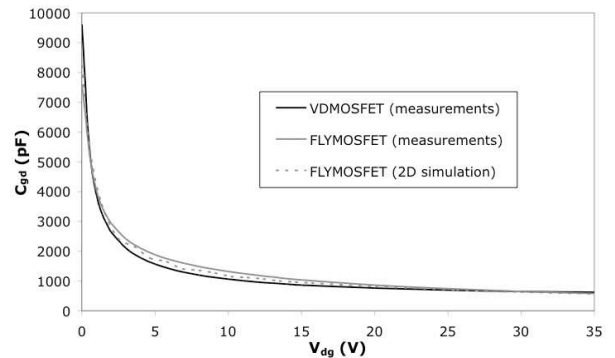


Fig. 4. Gate-drain capacitance variations vs applied voltage.

## Drain-Source Capacitance

Figure 5 presents the drain-source capacitance measurements for the two structures and drain-source capacitance simulation of the FLYMOSFET. The drain-source capacitance of the FLYMOSFET seems to be proportional to  $1/\sqrt{V_{ds}}$ , as the VDMOSFET and as analytically predicted. The  $C_{ds}$  capacitance improvement is confirmed. Nevertheless, because of some differences in the design of the two structures (different gate oxide thicknesses for instance), it is difficult to do an accurate comparative study between the VDMOSFET and the FLYMOSFET.

Differences between simulated and experimental results is mainly due to the approximations of the simulation. Indeed, the structure was simulated in 2D in cylindrical coordinates, which results in a difference of volume between the cubic shape base-cell and the simulated cylinder. The “missing surface” is a part of the “P-body/N<sup>+</sup> epitaxy”: it is a non-negligible part of the drain-source capacitance (Fig. 5), whereas it did not influence the gate-drain capacitance (Fig. 4).

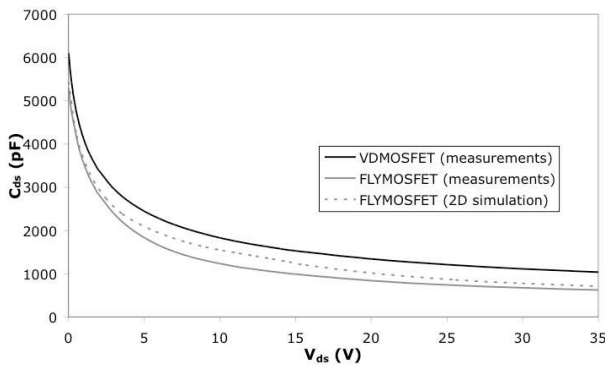


Fig. 5. Drain-source capacitance variations vs applied voltage.

Saito *et al* [8] showed a two phases decrease in the capacitance for a Floating Islands Schottky diode. A rupture occurs when the depletion zone under the P-body reaches the island. Because of the small size and the weak doping level of our P-floating islands, the same phenomenon is not observed in our measurements.

## Gate Charge

The principle of the gate charge is to inject a constant current on the gate to charge it to a reference voltage. The charge to provide to the device input to turn it on is proportional to the time. Drain current is limited by a resistance and the source current is ordered by a pulse generator cutting the energy as soon as the voltage of reference is obtained, thus avoiding an internal warm-up of the device (Fig. 6).

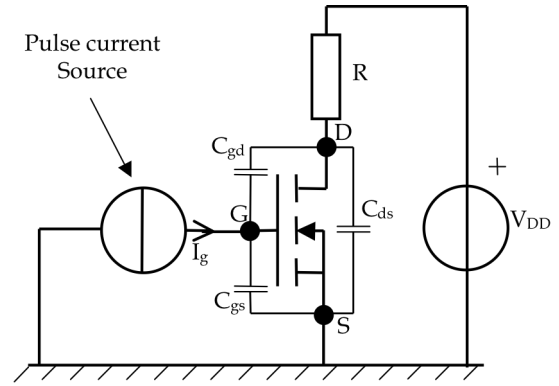


Fig. 6. Schematic of the measurement of the gate charge with  $R = 2\Omega$  and  $I_g = 2mA$ .

Figure 7 presents gate charge measurements of the two structures (VDMOSFET and FLYMOSFET) and gate charge simulation of the FLYMOSFET. The three fundamental phases of the gate charge are observed:

- 1) the charge of the input capacitance  $C_{iss}$  ( $C_{gdmin} + C_{gs}$ ) before the threshold voltage is reached,
- 2) the “plateau” due to the Miller effect,
- 3) the charge of the new value of  $C_{iss}$  ( $C_{gdmax} + C_{gs}$ ).

Differences in gate charge measurements ( $Q_g$ ) between the two structures are due to the difference of the gate oxide thicknesses. While comparing the two measurements more finely, one can notice that the “Miller plateau” is less flat in the FLYMOSFET’s case. Nevertheless, it is not proved to date that this phenomenon is due to the insertion of the floating island in the drift zone.

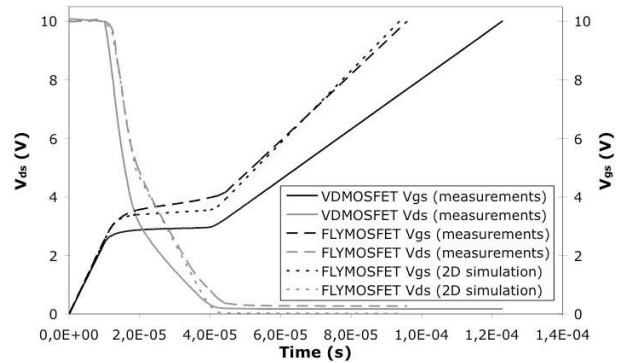


Fig. 7. Gate charge waveforms:  $Q_g = 192\text{ nC}$  (FLYMOSFET) and  $246\text{ nC}$  (VDMOSFET).

According to FLYMOSFET’s gate charge simulation, the main difference between measurements and simulation is the “Miller plateau”: simulation displays a nearly flat “plateau” whereas measurements present a slope that is not negligible.

## Predictive Simulations

The good match between simulations and measurements validates the used models and the good behavior of our simulations performed with ISE in dynamics and temporal.



To complete our analysis, it is good to compare this 65V FLYMOSFET with its equivalent in technology VDMOSFET (same breakdown voltage, same active area and same gate oxide thickness). Knowing that simulations match with the measurements, this comparative study may be made by mean of 2D cylindrical simulations. Table 1 gives the main parameters of the simulated structures.

Table 1 : Main device parameters of simulated conventional VDMOSFET and FLYMOSFET.

	65 Volts VDMOSFET	65 Volts FLYMOSFET
N <sup>-</sup> epitaxial layer thickness ( $\mu\text{m}$ )	4.0	5.35
N <sup>-</sup> epitaxial layer doping concentration ( $\text{cm}^{-3}$ )	$7 \times 10^{15}$	$1.1 \times 10^{16}$
P-floating layer maximum doping concentration ( $\text{cm}^{-3}$ )	–	$3.5 \times 10^{16}$

Figure 8 shows the gate-drain capacitance variations versus the drain-gate bias. No significant difference in the  $C_{gd\text{max}}$  values is observed because the gate oxide thickness is identical. The  $C_{gd\text{min}}$  values are also close because depletion capacitances ( $C_{gd\text{dep}}$ ) are relatively weak at high drain-gate voltages and, therefore, comparable - expression (3) -. The only difference concerns the difference of depletion that depends on the doping concentration of the N<sup>-</sup> epitaxial zone: in this “intermediate part”, the  $C_{gd}$  capacitance of the FLYMOSFET is lightly higher than the VDMOSFET’s one. Simulation confirms therefore that the FLYMOSFET technology lightly damages the input capacitance.

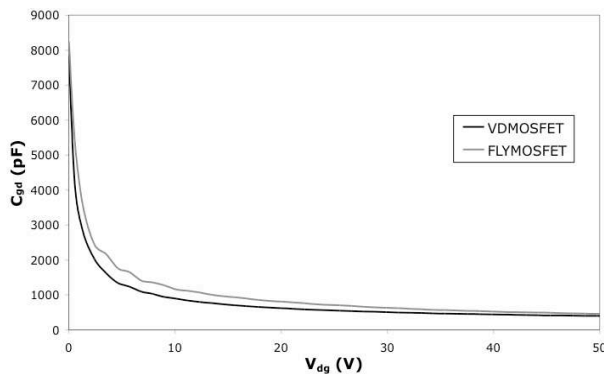


Fig. 8. Simulated gate-drain capacitance variations vs applied voltage for equivalent VDMOSFET and FLYMOSFET.

Concerning the gate charge simulation (Figure 9), a light deterioration of the FLYMOSFET is observed compared to the VDMOSFET. This is due to the length of the “Miller plateau”, that is longer in the FLYMOSFET’s case. The difference in the  $Q_g$  charge is assigned in totality to this length. The  $V_{ds}$  slope depends on the speed of the depletion zone reduction in the drift zone. This difference could come from the insertion of the island or from the difference in the N<sup>-</sup> epitaxial layer doping concentration.

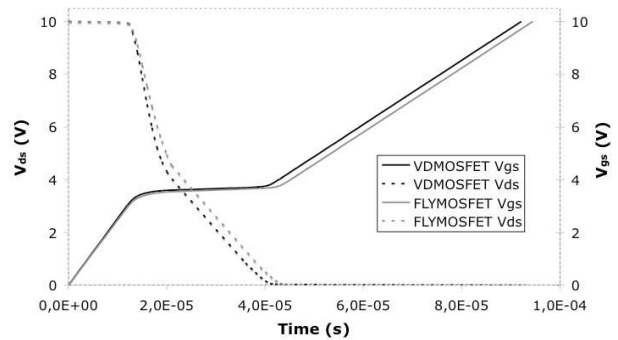


Fig. 9. Simulated gate charge waveforms for equivalent VDMOSFET and FLYMOSFET.  $Q_g = 184 \text{ nC}$  (VDMOSFET) et  $189 \text{ nC}$  (FLYMOSFET).

## CONCLUSION

In this work, the switching performance of a 65V FLYMOSFET has been investigated for the first time and its performance has been compared to the conventional VDMOSFET’s one. Measurements allow to note that the different capacitance behaviours were almost the same. The good match between measurements and simulations, performed with a 2D structure described in cylindrical coordinates, has allowed the validation of our simulations. Finally, the 2D simulated 65V FLYMOSFET and its equivalent VDMOSFET have been studied permitting a more accurate comparison of the two structures.

The FLYMOSFET is therefore an excellent power switch since he displays low losses in the on-state in compared to a conventional VDMOSFET [2] and nearly the same switching behavior. Besides, the dynamic models of ISE software have been validated, in order to go on doing predictive simulations of this type of structures.

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