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# Analysis and optimization of a Novel High Voltage Striped STI-LDMOS Transistor on SOI CMOS Technology

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## Abstract

*This paper analyses the static and dynamic characteristics of a novel n-type lateral-double-diffused MOS (LDMOS) with a striped Shallow Trench Isolation (STI) structure – called Striped STI-LDMOS – for switching applications in the 100-150 voltage range by means of 3D TCAD numerical simulations. The proposed structure based on a 0.18 $\mu\text{m}$  SOI CMOS technology and defined with STI strips and gate field plate fingers located on top of the defined STI, exhibits much lower gate-to-drain ( $C_{GD}$ ) capacitances and gate charge ( $Q_g$ ) and a better electrical safe operating area (SOA) as compared with a conventional STI-LDMOS counterpart.*

**Keywords:** LDMOS transistor, Shallow Trench Isolation, safe operating area, gate-to-drain capacitance, SOI, TCAD simulations.

## INTRODUCTION

In smart power technology, where power devices are associated with CMOS and analogic circuits on the same chip, LDMOS transistors have proven to be the best suited power switch thanks to their ease of integration and isolation with CMOS technology [1]. For lithography resolution of 0.25 $\mu\text{m}$  and lower, the LOCOS oxidation has evolved to more precise shallow trench isolation (STI) oxidation, leading to the development of new designs of LDMOS transistors [2]. The gain enhancement in CMOS technology due to lithography size reduction is difficult to reach in power LDMOS due to the presence of the drift region, also called lightly doped drain (LDD) region, necessary for high voltage specificity. Static characteristics, such as breakdown voltage ( $V_{BR}$ ) and specific on-state resistance ( $R_{on-sp}$ ) are specially linked to the drift region length ( $L_{LDD}$ ), in the well known  $V_{BR}/R_{on-sp}$  trade-off. Several techniques have been proposed so far to improve this trade-off, such as RESURF effect [3] or the superjunction concept [4]. As for dynamic characteristics, the LDMOS switching performance is not only limited by its specific on-state resistance ( $R_{on-sp}$ ), but also by the gate charge ( $Q_g$ ) and inter-electrode capacitances for a given  $V_{BR}$  value. However, other electrical characteristics, such as the safe operating area (SOA) have to be taken into account during the optimization of LDMOS transistors, because device geometrical and technological parameters, especially those concerning the channel/STI region definition, have a direct influence on the device ruggedness [5]. Hence, both reliability and switching performance should be optimized at the same time.

Different LDMOS transistors with STI in the LDD region (STI-LDMOS) have previously been extensively analyzed by numerical simulations [6, 7] and experimentally [7]. However, their dynamic characteristics are quite limited because of their inherent gate capacitances. The use of lateral gates and field plate on top of STI strips [8], successfully demonstrated on medium voltage LDMOS ( $V_{BR} < 40\text{V}$ ), can highly reduce these parasitic capacitances. Nevertheless, based on the authors' knowledge, this kind of structure has never been optimized for high voltage applications. In this sense, this work is addressed to analyze a new 150V voltage class power LDMOS design structure in terms of  $V_{BR}/R_{on-sp}$  trade-off,  $R_{on} \times Q_g$  figure of merit (FOM), gate capacitance evolution and safe operating area by means of 3D TCAD simulations.

## STRUCTURES DESCRIPTION

Figure 1 shows the schematic cross section of the LDMOS transistors investigated in this paper: the proposed Striped STI-LDMOS (a) and the conventional STI-LDMOS (b), which are based on a 0.18 $\mu\text{m}$  smart power technology on thin-SOI substrate. All the analyzed LDMOS structures have the same thin-SOI substrate with a SOI layer ( $T_{SOI}$ ) and buried oxide ( $T_{BOX}$ ) thickness of 1.6 $\mu\text{m}$  and 1 $\mu\text{m}$ , respectively. The same  $L_{LDD}$  of 7 $\mu\text{m}$  for a total cell length ( $L_{cell}$ ) of 11.5 $\mu\text{m}$  is also considered. Both LDMOS structures require a previously formed STI block in the drift region before the P-well and N-well implantation definition. A STI length ( $L_{STI}$ ) of 4 $\mu\text{m}$  which partially and totally covers the  $L_{LDD}$  and the device width

( $W$ ), respectively, is considered in conventional structure (see figure 1 (b)) Unlike the conventional STI-LDMOS, the STI strips in the novel structure (see Figure 1 (a)) are defined partially covering the device width ( $W$ ). Hence, the cell width of the Striped STI-LDMOS can be described as the addition of the region covered by the STI ( $W_{STI}$ ) and the region not covered by the STI ( $W_{Si}$ ). It is also noticeable the STI extension along the P-well diffusion. Hence, the poly-gate block, deposited only on the top of the STI strips, defines not only the gate electrode but also the field plate above the N-drift region. The total poly-gate length over the STI is then described as the addition of the poly-gate length covering the P-well diffusion where the inversion channel is formed ( $L_{channel}$ ) and the poly gate covering the N-drift region which acts as a gate field plate ( $L_{FP}$ ).

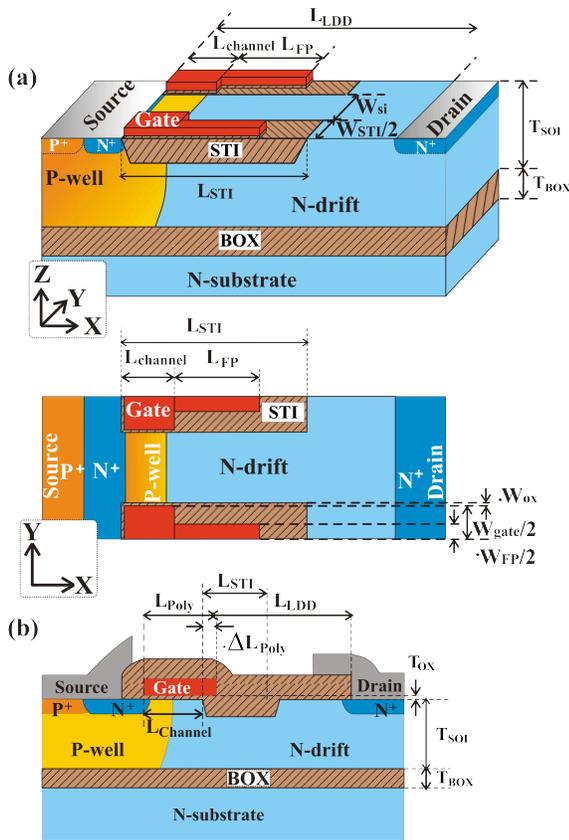


Figure 1: Schematic cross section of the (a) proposed striped STI-LDMOS and (b) conventional STI-LDMOS structures

A simulation result of the electron concentration distribution in the channel region of the striped STI-LDMOS is plotted in figure 2. As clearly observed, the channel inversion layer is laterally formed along the sidewall of the STI/P-well interface. The distance between poly-gate and STI edge ( $W_{ox}$ ) determines the effective gate oxide thickness and consequently the threshold voltage of this analyzed structure. On the other hand, the main portion of the inversion layer is mainly present on the top surface of the STI sidewall thanks to the higher

permittivity of the nitride spacer [9], but also on the sidewall and, in a lesser extend, in the bottom of the STI.

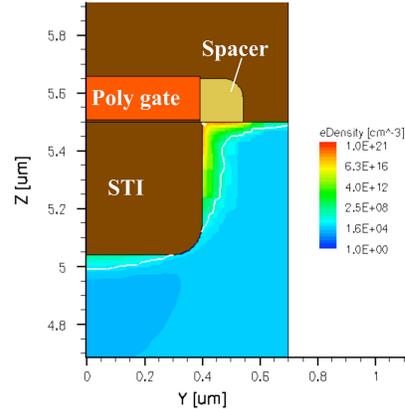


Figure 2: Electron distribution in the channel region of the striped STI-LDMOS

## TCAD SIMULATIONS RESULTS

### $V_{BR}/R_{on-sp}$ trade-off

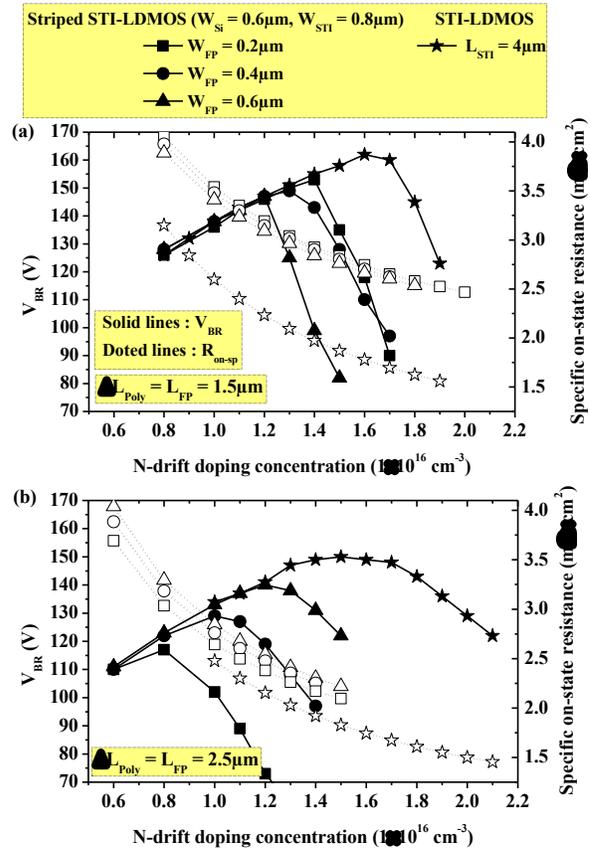


Figure 3:  $R_{on-sp}/V_{BR}$  trade-off as a function of the N-drift doping concentration and  $W_{FP}$  values considering different  $\Delta L_{Poly}$  and  $L_{FP}$  values of (a)  $1.5\mu m$  and (b)  $2.5\mu m$  in the STI-LDMOS and Striped FP-LDMOS, respectively.

Figure 3 shows the  $V_{BR}/R_{on-sp}$  trade-off comparison between both analyzed LDMOS structures as a function of the N-drift doping concentration, where different values of the gate field plate width ( $W_{FP}$ ) and length ( $L_{FP}$ ) are considered in the case of the Striped STI-LDMOS. The lower  $R_{on-sp}/V_{BR}$  trade-off results exhibited by the Striped STI-LDMOS structure compared to the conventional structure is derived by the high electric field reached at the end of the channel, which limits  $V_{BR}$ , and by the worse gate drift current transition, which limits the  $R_{on-sp}$ . The  $W_{FP}$  parameter, which does not affect the  $R_{on-sp}$  characteristics, has a strong influence on  $V_{BR}$  evolution. The observed degradation of  $V_{BR}$  as  $W_{FP}$  increases is due to the increase in the electric field along the STI/silicon interface because of the reduction of the STI width not covered by the poly field plate. On the other hand, the increase of  $L_{FP}$  will reduce the  $R_{on-sp}$  thanks to an enhanced field effect action in the N-drift region. It leads, however, to a degradation of the  $V_{BR}$  because of the worse electric field distribution in the drift region.

The effective gate oxide, corresponding to the combination of the gate oxide thickness ( $T_{ox}$ , see figure 1 (b)) and the spacing distance between poly gate and STI edge ( $W_{ox}$ ) leads to a higher threshold voltage ( $V_T$ ) in the Striped STI-LDMOS, as represented in the transfer function of figure 4. Hence, the  $V_T$  increase, along with the lower area for the inversion layer path and the bad gate to drift current transition, contributes to the worse  $R_{on-sp}$  results as compared with the conventional structure, specially at low  $V_{gs}$  values as observed in figure 4. However, the better linearity of the transfer characteristics make the striped STI-LDMOS a good candidate for radio-frequency applications.

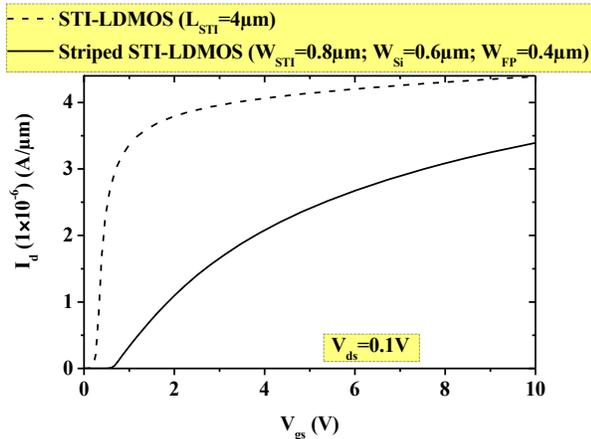


Figure 4: Drain current as a function of  $V_{gs}$  for both analyzed STI-LDMOS structures.

### Dynamic performance

The gate charge of power MOS transistors is representative of their switching losses. As a consequence,

the gate charge value ( $Q_g$ ) has then to be reduced in order to improve the switching performances. The figure 5 represents the gate voltage evolution as a function of gate charge of both LDMOS optimized in terms of  $V_{BR}/R_{on-sp}$  trade-off. The simulations have been carried out with the transistor switching on a resistive load and with its gate connected to a current generator. Consequently the charge  $Q_g$  is proportional to the switching time.

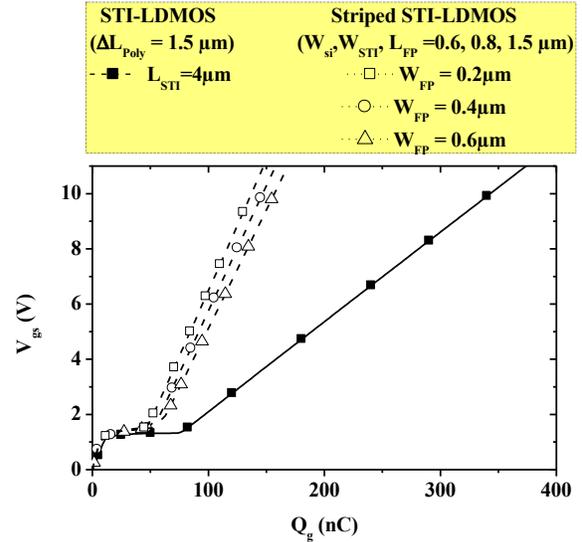


Figure 5: Gate voltage versus gate charge and  $R_{on-sp} \times Q_g$  FOM

As observed in figure 5, in spite of the higher  $R_{on-sp}$  values (see figure 3 and 4), lower  $R_{on-sp} \times Q_g$  FOM can be obtained in the analysed in the Striped STI-LDMOS (see table 1) due to lower poly-gate interaction with the P-well region surface.

	Parameter value	$R_{on-sp} \times Q_g$
STI-LDMOS	$\Delta L_{Poly} = 1.5 \mu m$	0.552
Striped STI-LDMOS	$L_{FP} = 0.2 \mu m$	0.397
	$L_{FP} = 0.4 \mu m$	0.421
	$L_{FP} = 0.6 \mu m$	0.462

Table 1:  $R_{on-sp} \times Q_g$  FOM comparison for different parameter values

Other important indicator is the comparison of the  $C_{gd}$  evolution as a function of the applied  $V_{gd}$  by means of small-signal simulations, illustrated in figure 6 where a  $C_{gd}$  peak value five fold lower than the conventional structure is achieved in the Striped STI-LDMOS. As a consequence, a significantly reduction of  $Q_g$  and  $C_{gd}$  can be obtained, so that better switching performance is reached in the Striped STI-LDMOS structure. Moreover, considering that the  $R_{on-sp}$  is independent of the  $W_{FP}$  parameter, an improvement of  $R_{on-sp} \times Q_g$  FOM can be achieved with the reduction of  $W_{FP}$ .

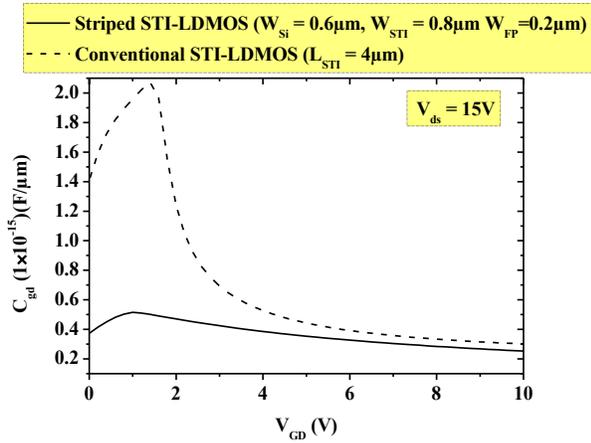


Figure 6:  $C_{gd}$  as a function of  $V_{gd}$  for both LDMOS structures

### Safe operating area (SOA)s

The body current ( $I_{body}$ ) evolution vs  $V_{gs}$  at high applied  $V_d$  values is a good indication for the evaluation of the safe operating area of the LDMOS structures [10, 11]. Then, in order to determine the  $I_{body}$ , a separated body contact is placed in all the simulated structures. The comparison of the simulated results from figure 7 shows the typical  $I_{body}$  vs  $V_{gs}$  characteristics curve in LDMOS transistors, where a first  $I_{body}$  peak at low  $V_{gs}$  values is observed. This  $I_{body}$  peak is specially related with the increase of  $e^-/h^+$  pairs generated by impact ionization at the P-well/N-well junction in the channel region. This peak is proportional to the applied  $V_{ds}$  [10]. According to figure 7,  $W_{FP}$  plays an important role in on the  $I_{body}$  first peak in Striped STI-LDMOS. On the other hand, the  $I_{body}$  peak is followed by an  $I_{body}$  valley characteristic due to the reduction of the electric field at the P-well/N-well junction region as  $V_{gs}$  increases. Finally, beyond the valley, the curve exhibits a  $I_{body}$  positive slope up, which is more related to the Kirk effect at high  $V_{gs}$  values [10, 11].

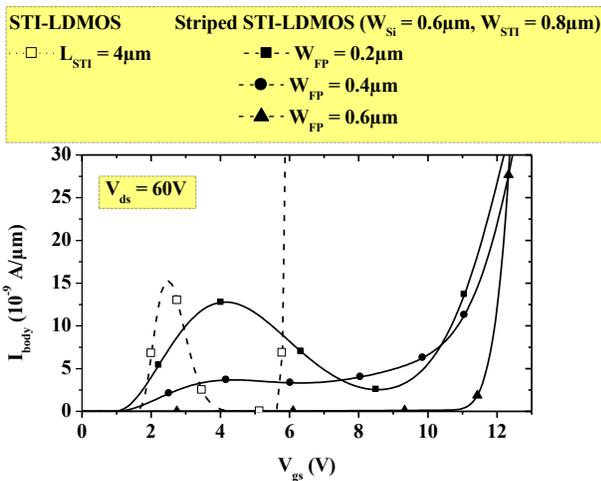


Figure 7:  $I_{body}$  characteristics vs  $V_{gs}$  for both LDMOS structures at high applied  $V_{ds}$  of 60V

The electric field distribution and impact ionization generation along the STI/silicon interface of the Striped STI-LDMOS at three  $V_{gs}$  values, corresponding to the first  $I_{body}$  bump ( $V_{gs}=4V$ ), the  $I_{body}$  valley ( $V_{gs}=8.4V$ ), and the current slope-up ( $V_{gs}=15V$ ) are plotted in figures 8 and 9, respectively.

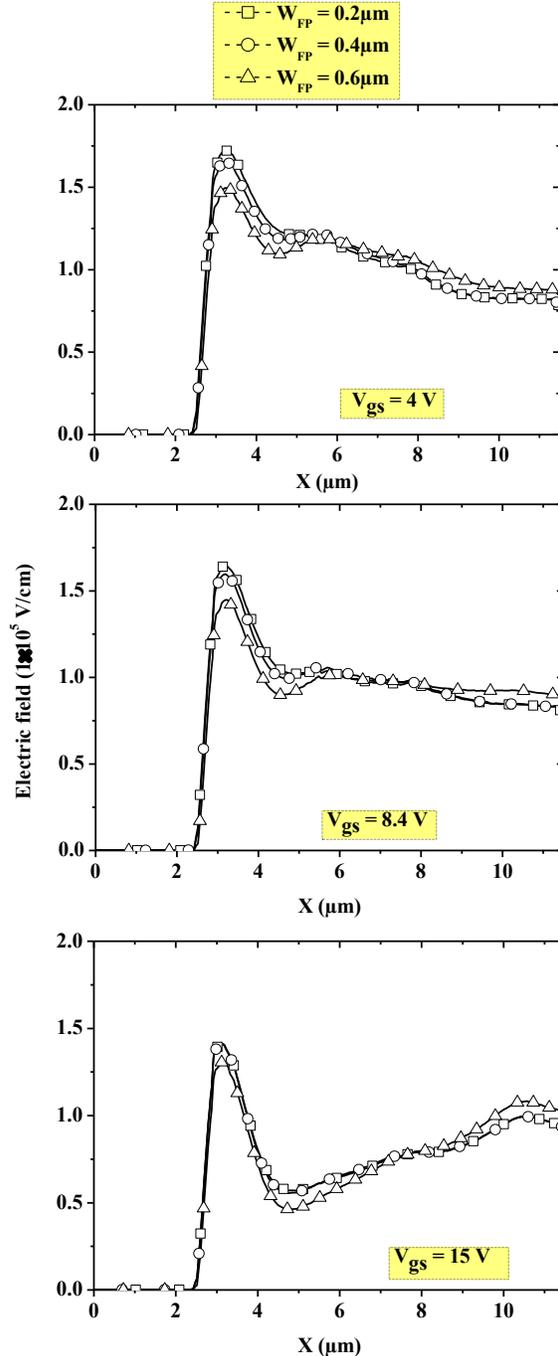


Figure 8: Electric field distribution along the STI/SOI interface for different values of the  $W_{FP}$  at three different  $V_{gs}$  in the Striped STI LDMOS transistor

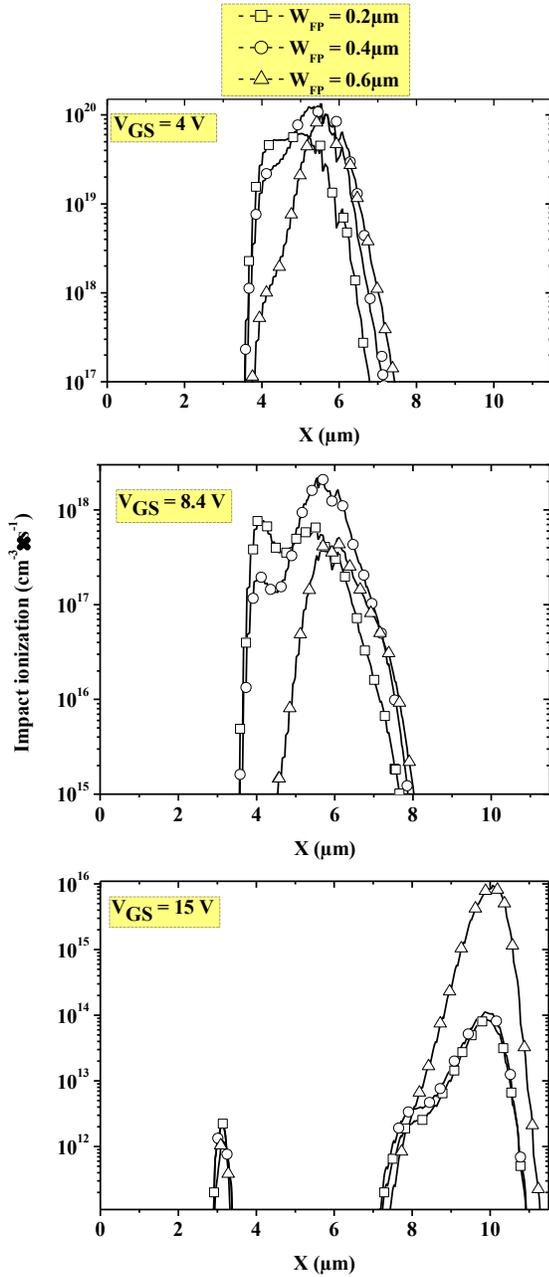


Figure 9: Impact ionization along the STI/SOI interface for different values of the  $W_{FP}$  at three different  $V_{gs}$  in the striped STI LDMOS transistor

The electric field peak at  $X = 3.5\mu\text{m}$  in figure 8 at low  $V_{gs}=4\text{V}$ , is located just at the transition between the poly-gate used to form the inversion layer and the poly-gate used as a field plate. This high electric field, combined with high impact ionization, (see figure 9), could lead to higher possibility of hot-electron being injected into the oxide region, which results in hot-carrier degradation [12]. With the increase in  $W_{FP}$ , this obtained electric field peak and the electron/hole pair generation can be reduced, thus obtaining a more uniformly electric field distribution, which explains the lower  $I_{\text{body}}$  peak in the figure 7. On the

other hand, the high avalanche generation at the  $N^+$  drain ( $X=10\mu\text{m}$ ) when high  $V_{gs}$  of 15V is applied, is specially noticeable for the larger  $W_{FP}$ . This fact could explain the more abrupt  $I_{\text{body}}$  slope-up observed in figure 7.

Consequently, special care with the gate field-plate design is required since a trade-off between  $V_{BR}/R_{\text{on-sp}}$ , dynamic characteristics and electrical SOA have been observed.

### Process variability

Taking into account that the effective gate oxide is formed by the positioning of the poly-gate with the STI oxide, the mask misalignment could affect the electrical characteristics of the Striped STI-LDMOS transistor. Figure 10 represents the effect of a misalignment between the poly gate and the STI on their relative positioning in the Y axis direction ( $\Delta Y$ ) and figure 11 shows variability of  $R_{\text{on-sp}}$  and  $V_t$  with the defined  $\Delta Y$  parameter.

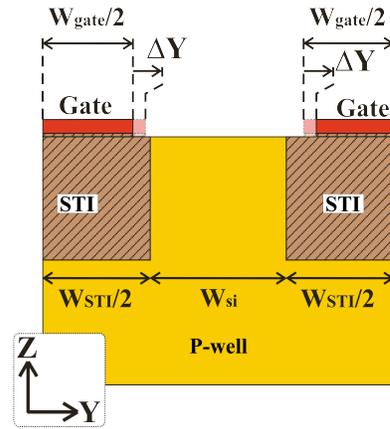


Figure 10: Cross section detail (through the P-well/STI Y axis) of a Striped STI-LDMOS cell showing the possible mask misalignment between the poly gate and the STI indicated by the parameter  $\Delta Y$ .

The results of figure 11 shows that a misalignment of the poly-gate mask will lower the threshold voltage of the striped STI-LDMOS since either the left or the right poly-gate will move closer to the STI/Silicon interface for positive or negative values of  $\Delta Y$ . Beside, due to the structure symmetry, the possible increase of the channel resistance due to the higher effective gate oxide in one side of the Striped STI block is compensated by the resistance reduction on the opposite side, thus leading to an even lower  $R_{\text{on-sp}}$  variation.

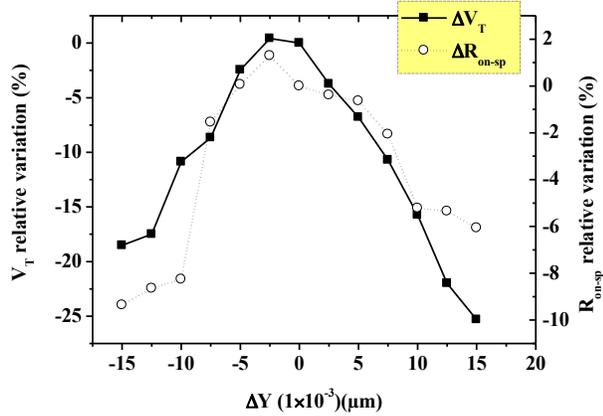


Figure 11: Relative variation of the  $R_{\text{on-sp}}$  and  $V_t$  as a function of the  $\Delta Y$  parameter.

## CONCLUSION

In this paper, a novel striped STI-LDMOS transistor ( $V_{\text{BR}} > 120$  V) based on a  $0.18\mu\text{m}$  CMOS SOI technology has been analyzed by means of TCAD numerical simulations. The lower  $V_{\text{BR}}/R_{\text{on-sp}}$  trade-off results compared to a conventional STI-LDMOS structure are compensated with a better  $R_{\text{on}} \times Q_g$  figure-of-merit thanks to the much lower poly-gate/Silicon interaction, and better SOA performance. As for device optimization, special care with the gate field-plate design is required since a trade-off between  $V_{\text{BR}}/R_{\text{on-sp}}$ , dynamic characteristics and electrical SOA with the  $W_{\text{FP}}$  parameter is observed. Beside, possible misalignments in the poly-gate definition could highly affect the repetitivity of the electrical characteristics ( $R_{\text{on-sp}}$  and  $V_t$ ) of the device)

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