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Controlled epitaxial graphene growth within amorphous carbon corrals

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Structured growth of high quality graphene is necessary for technological development of carbon based electronics. Specifically, control of the bunching and placement of surface steps under epitaxial graphene on SiC is an important consideration for graphene device production. We demonstrate lithographically patterned evaporated amorphous carbon corrals as a method to pin SiC surface steps. Evaporated amorphous carbon is an ideal step-flow barrier on SiC due to its chemical compatibility with graphene growth and its structural stability at high temperatures, as well as its patternability. The amorphous carbon is deposited in vacuum on SiC prior to graphene growth. In the graphene furnace at temperatures above 1200°C, mobile SiC steps accumulate at these amorphous carbon barriers, forming an aligned step free region for graphene growth at temperatures above 1330°C. AFM imaging and Raman spectroscopy support the formation of quality step-free graphene sheets grown on SiC with the step morphology aligned to the carbon grid.

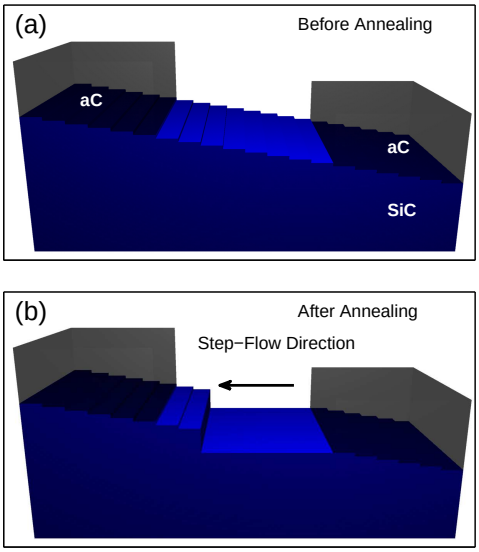

FIG. 1. aC step pinning process. Depicted in (a) are the SiC steps occuring before the graphene growth. In (b) the mobile steps have accumulated to the lower free energy configuration.

To be technologically viable, graphene must be grown in a well controlled manner. Beyond preparing well ordered 2-dimensional graphene films, growth needs to be tailored at the nanoscale to produce the desired devices at pre-defined locations. Epitaxial graphene on silicon carbide (EG) meets these criteria[1]. EG has excellent electronic transport properties, including record high frequency operation[2], long spin diffusion lengths[3], and room temperature ballistic transport[4]. Precise EG growth has been successful on tailored SiC substrates. Single layer nanoribbon growth has been produced on the SiC sidewalls of plasma etch steps[4,5] and EG thickness control was demonstrated on etched mesas[6]. Selective graphene growth was also achieved by capping flat SiC with a high temperature stable layer to prevent (or enhance) graphene formation[7–9]. Progress in graphene growth selectivity was shown using Chemical Vapor Deposited (CVD) methods, where an oxide barrier[10] provides better growth control on Cu and self-assembled nanoribbons on gold surfaces have been demonstrated.[11] Unlike CVD methods, however, the advantage of EG for technological development is to be scalable directly on a high quality semi-insulating production substrate. Further advantages of EG include its integration with silicon[12] and SiC electronics[13].

This Letter focuses on locally controlling the step bunching of SiC during EG growth. Although EG grows like an overlaying carpet on the stepped SiC surface, steps provide graphene nucleation sites[6,14,15] that need to be controlled. Furthermore, underlying SiC steps induce additional electronic scattering in graphene.[16] SiC step spacing depends on the miscut angle of the SiC crystal surface from the basal plane of the Si or C terminated faces, in addition to the thermodynamically favored

step height. The smallest miscut angle of commercially available SiC wafers is at most 0.1°, but it varies throughout the wafer and leads to variations in the step density and orientation. Preparation of well-defined SiC surfaces with regularly spaced steps, by hydrogen etching, can be preserved in a range of growth parameters[17] but generally leads to further step bunching at the graphene growth temperature (T>1300°C in the confinement controlled sublimation method[18] or higher under atmospheric pressure argon[19]). These methods, however, cannot provide a precise alignment of the steps. Another way is to get rid of the steps altogether by step flow at the edges of etched mesas[18].

On unpatterned EG on SiC, the steps tend to bunch into unit cell high steps[20], which is 1 nm high for 4H-SiC. Their spacing is determined by the local miscut angle, which for on-axis wafers is typically in the range 0.1° to 0.5°, giving step spacing of 600nm to 110nm. Under the proper H_2 etching and growth conditions higher step heights give correspondingly wider terraces, often around 1 μm wide.[17] However, a naturally formed surface cannot have an arbitrarirly determined step width, and in addition an arbitrarily determined step location and orientation. This means that given step spacings of this size, steps are likely to interfere with a graphene device.

To successfully tailor growth of EG on SiC requires placement of structures that are stable at EG growth temperatures on the SiC surface. Mesas[18] and trenches[21] etched into SiC are one solution. Generally, any surface configuration that would prevent step diffusion on SiC will successfully structure step bunching, including on other materials such as silicon[22,23]. Deeply etched grid features in these silicon samples enclose the step-flow[22,23].

Recognizing that graphene layers hinder step-flow[18], and that graphitic materials are also high temperature stable, we propose here to enclose the naturally occuring surface steps on SiC with evaporated amorphous carbon (aC). Compared with other refractory materials, amorphous carbon is completely compatible with graphene growth as it will not introduce additional chemical elements. Annealed aC forms nanocrystalline graphite[24] and is at least as structurally stable as graphene, such that it retains its patterned shape.

Creating a two-dimensional corral-like enclosure confines the diffusion of the atoms on the surface, such that any preferred step-flow direction will organize the steps into fewer larger steps bunched at one end of the enclosure. See Figure 1 for a schematic cutaway of the step bunching controlled growth. We choose a grid with dimensions that is comparable with the expected distance over which steps will bunch, which is typically a few microns.

This step-flow control method harnesses the surface free energy minimization such that step bunching is favored at one end of the enclosure. Mobile steps flow by surface diffusion or sublimation of the surface atoms. Step-flow on Si is mediated by evaporation of the Si atoms from the surface.[22,23]

However, with EG on SiC, the step-flow is a separate mechanism from the graphene growth.[15] If graphene is growing, additional step flow due to Si sublimation is possible. Note that unlike in silicon, the step flow on SiC before EG growth conserves mass. Steps accumulate at one end of an individual grid cell according the local miscut angle on the sample surface.

We prepared EG samples using research grade 4H SiC (0001) and $(000\bar{1})$ substrates cut to 3.5×4.5 mm^2 dimensions. These chips came from a nominally on-axis wafer from Cree corporation having a nominal miscut of 0°, with an actual miscut angle of up to 0.1°. The samples were ultrasonically cleaned for thirty minutes each in acetone and isopropyl alcohol. Three samples were studied: G1, which has monolayer graphene grown on the hydrogen etched Si-face, G2 which is multilayer graphene grown on the polished C-face (see supplemental for images of G2), and B1 which is buffer layer grown on chemical and mechanically polished Si-face. Sample G1 was hydrogen etched in a 40cc/s (3% H_2)/(97% Ar) flowing forming gas mixture at 1450° C at one atm. The hydrogen etching furnace is an inductively heated furnace with a tantalum sample holder. The hydrogen etched surface has well defined SiC steps before the step controlled graphene growth. As seen from Figure 2, the initial step height on the hydrogen etched sample is about 1nm, corresponding to 4 SiC unit cells.

Amorphous carbon (aC) is deposited using a Cressington 108A carbon deposition system modified for high vacuum use. Deposition occurs by resistively heating a graphite rod point contact junction to a temperature exceeding the temperature of graphite sublimation. A 3 Ω junction evaporates with a current 120 A. The aC was uniformly deposited at 10^{-6} mbar over all the sample surface. An in-situ quartz crystal monitors the deposited aC thickness, until a typical a thickness of 20nm is deposited.

The aC is then patterned into a 5×5 μm^2 square grid pattern using standard electron beam lithography. For this, MaN 2403 negative e-beam resist is spin coated onto the samples at 5000 RPM and baked for 60 seconds at 90° C on a hot plate. E-beam exposure occurs with a cumulative dose of 200 $\mu C/cm^2$. The resist is developed for 5 minutes in MF-319 (3% TMAH) developer. Oxygen plasma RIE etches the unmasked aC. The oxygen is flowed at 4 sccm and RF power of 16 W is applied to the reaction chamber. A typical etch time is 75 seconds. Once the aC is etched through, any overetch into the SiC will introduce a silicon oxide passivation layer to the SiC, which is maximally a few nanometers thick. The oxide layer thickness is self-limiting and is removed during an anneal step as part of the Confinement Controlled Sublimation (CCS) graphene growth process in the furnace[18].

Prior to growth, the samples are cleaned overnight at room temperature in an acetone solution

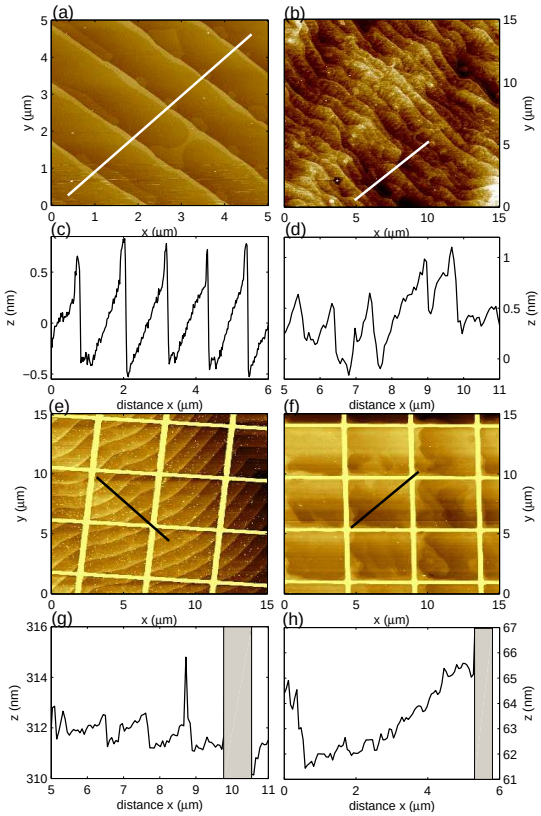

FIG. 2. AFM images of the surface of hydrogen etched SiC(0001) (a) before and (b) after graphene growth. The corresponding step profiles taken along the step flow (white line in figures (a) and (b)) (c) before and (d) after graphene growth. The AFM images (e) and (f) and corresponding profiles along step flow (g) and (h), respectively, depict the morphology before and after graphene growth using the amorphous carbon grid.

to dissolve the remaining resist, and then the samples are rinsed with isopropol alcohol. Samples are grown using Confinement Controlled Sublimation (CCS) in a graphite enclosure in an induction heated furnace.[18] The sample is annealed at 1150° C for 20 minutes to remove silicon dioxide, and then the graphene growth step proceeds.The Si-face graphene sample G1 was grown at 1600° C for 40 minutes and the buffer layer sample B1 was grown at 1350° C for 30 minutes.

Characterization of the surface topography at various stages of process was done using non-contact mode atomic force microscopy (AFM). Before the growth on the unetched surface, there is a nanometer scale roughness in the region within the aC enclosure.(Figure 2 and 3 part (e))This roughness does not remain after the graphene growth due to removal of the surface oxide layer. On Figure 2 part (e) and (f) note that the orientation of the steps is different in each sub figure. This is due to differing local wafer miscut throughout the sample surface.

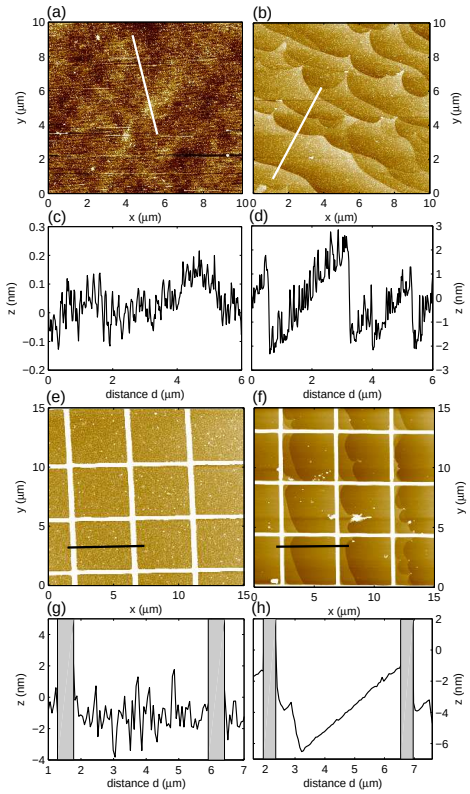

FIG. 3. As in Fig. (2) but here for sample B1. The SiC surface was chemically and mechanically etched prior to growth. The process of buffer formation without aC grid (a) before and (b) after buffer growth, corresponding profiles (c) and (d). The surface morphology using aC grid (g) before and (h) after buffer growth. Corresponding step profiles along the step flow are shown in figures (g) before and (h) after buffer growth.

See Figures 2 and 3 part (f) for the AFM topography after the sample growth. All samples indicate the step morphology aligns to the aC grid. Larger, nanometer sized aC particles from the aC deposition pin the steps seen in sample B1 away from the gridded area into a pinched shape(Figure 3 (b)). Nanometer sized aC particles are deposited in greater numbers as the carbon rod source is heated to higher temperatures.

Averaging the step widths from the AFM images indicates that the average step width before growth on sample G1 is 0.96 μm. (Figure 2, subfigures (a) and (c)) Away from the grid the average step width is 0.22 μm after growth, and within the grid the step width is increased to 1.9 μm. On sample B1 the average step width before growth is 0.2 μm. After growth the average step width away from the grid is 1.4 μm and within the grid the step width is 3.3 μm. In both hydrogen etched and non-hydrogen etched cases the presence of the step flow barrier increases the average

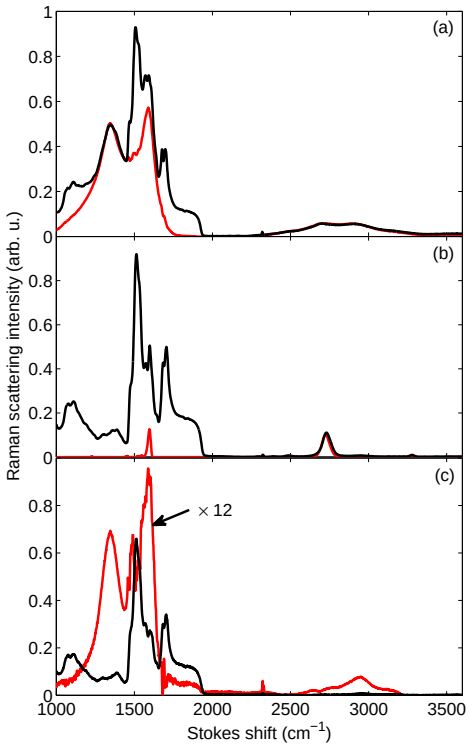

FIG. 4. Raman scattering spectra (using a $\lambda = 532$nm laser) of (a) in red: aC and in black: aC and SiC, (b) in red: Sample G1 single layer graphene and in black: graphene and SiC (c) in red: sample B1 buffer layer on a Si-face 4H-SiC, and in black: SiC and buffer.

step width.

Using Non-negative Matrix Factorization (NMF) spectral decomposition to separate the Raman spectra into its principle components[25], the Raman spectra of the graphene on sample G1 may be separated from the aC (see Figure 4). The principle component corresponding to the graphene indicates monolayer growth according to the intensity of the peaks. The principle component that corresponds to the aC indicates nanocrystalline graphite, where the ratio of the D to G peak intensity $\frac{I_D}{I_G} = 0.86$. This ratio corresponds to a graphitic crystallite size of 20 nm.[26] Nanocrystals form upon annealing the aC at graphene growth temperatures. Buffer layer Raman spectra, with a much weaker signal than graphene, is seen on sample B1.[27,28]

Understanding the role that the aC grid structure, growth temperature and SiC wafer miscut play is important for optimal step flow control. For instance, the step flow of the buffer sample B1 appears to be better organized than on the graphene sample G1. The reasons for this difference will require further experiments. We can nevertheless conclude firstly that the step flow indeed involves mass transfer within the aC enclosure only. This is because the total mass of SiC has been conserved

before and after graphitization as calculated (The volume of silicon carbide is calculated from step heights and positions before and after growth as well as the carbon contribution to graphene.) from the position of the steps in the AFM images of samples G1 and B1. This mass conservation includes the loss of silicon due to graphene growth (roughly 3 SiC bilayer are required to form one graphene layer). Secondly, the 5×5 μm^2 square grid also appears to be smaller than the distance over which steps will rearrange, particularly on sample B1, since one dominate bunched step is present after growth.

Further step-flow experiments suggested include modifying the aC grid, the wafer miscut, and the growth conditions. Different sized and oriented aC step flow enclosures are in principle possible in order to tailor the step orientation according to the boundary conditions set by the grid. Additionally, a suitable insulating alternative to aC, like oxides or diamond-like carbon, may make the step flow control even more desirable from a device perspective, since aC is conductive. Performing step flow control on vicinal cut wafers may yield more consistent step bunching, since the total miscut angle will not be as sensitive to the miscut angle uncertainty, unlike on-axis wafers. The step bunching is likely to be greater as well on vicinal cut wafers, thereby enhancing the step flow control.[20] Finally, by increasing the background pressure with an inert gas in the CCS furnace it is possible to raise the onset temperature of graphene growth[18]. This would increase the step flow rates to possibly reach lower surface free energy before graphene forms and therefore inhibits step-flow during graphitization. Lower surface free energy may also be attained by hydrogen etching the sample prior to patterning the grid[17]. It is possible to tune the growth and hydrogen etch procedures to have even larger or specifically tailored step-free areas, in addition to learning more about SiC surface kinetics and graphene growth.

In conclusion, we have shown that evaporated amorphous carbon is effective for structured EG growth and is completely compatible with the CCS growth method. We have demonstrated that SiC step bunching is pinned by an aC cap that acts as a step flow barrier. The step morphology is aligned to the aC grid. Single layer graphene is thereby grown on up to 4 μm wide step-free areas which locations are predefined by lithography. Further work ought to yield larger step free areas and the possibility of controlling the growth of sidewall graphene on the bunched steps. Careful measurements of step flow control ought to yield deeper information about the graphene growth process on SiC, including mass transport and graphene nucleation rates. Integration of graphene into nanoelectronic processes demands structured growth, such that location and morphology of the graphene are controlled.

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