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Scalable templated growth of graphene nanoribbons on SiC

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Excellent electronic properties notwithstanding, the use of graphene in field-effect transistors is not practical at room temperature without modification of its intrinsically semi-metallic nature to introduce a band gap.[1–4] Quantum confinement effects can create a band gap in graphene nanoribbons, but existing nanoribbon fabrication methods are slow and often produce disordered edges that compromise electronic properties.[2–4] Here we demonstrate the self-organized growth of graphene nanoribbons on a templated silicon carbide substrate prepared using scalable photolithography and microelectronics processing. Direct nanoribbon growth avoids damaging post-processing. Raman spectroscopy, high-resolution transmission electron microscopy, and electrostatic force microscopy confirm that nanoribbons as narrow as 40 nm can be grown at specified positions on the substrate. Our prototype graphene devices exhibit quantum confinement at low temperature (4 K), and an on-off ratio of 10 and carrier mobilities up to 2,700 $\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$ at room temperature. We demonstrate the scalability of this approach by fabricating 10,000 top-gated graphene transistors on a 0.24 cm^2 SiC chip, which is the largest density of graphene devices reported to date.

Epitaxial graphene on SiC, prepared by thermal decomposition of SiC with the same as a built-in electronics-grade substrate, is an exciting new electronic material that presents the possibility of room temperature ballistic devices.[1,5,6] Extremely high carrier mobilities, exceeding 250,000 $\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$ at room temperature, have been observed,[7] and it has been shown compatible with traditional top-down processing techniques.[8,9] Its linear band structure[10] allows ambipolar tuning of conduction and direct application to RF devices,[11,12] and, in addition to nanoribbon fabrication, band gaps have been introduced by selective chemical treatment.[13,14] The nanoribbon approach, which introduces a band gap inversely proportional to ribbon width,[15] is promising in that it has shown large gating effects.[2,4]

The morphology of epitaxial graphene on SiC is highly influenced by the underlying SiC structure. In well-controlled graphene growth conditions,[5,6,16–18] nominally on-axis SiC retains an ordered terrace structure that originates in the miscut angle of the SiC wafer. Many interpret these steps as being problematic,[19] but scanning tunneling microscopy measurements have consistently observed that the graphene lattice is continuous over such steps. This is true of 0.5 nm $4H$-SiC half-unit cell steps and few-nm steps where step bunching

occurs.[1,20] We find that this remains true at a much larger scale, over prepared SiC steps as large as 150 nm [see Fig. S1]. These observations help explain transport measurements in which underlying SiC steps appear to have little effect on mobility[5,21] or observation of the quantum Hall effect,[21] and suggest that this fact may be exploited to produce nanoribbons by novel fabrication methods.

It has long been known[22] that SiC{0001} surfaces exhibit step bunching in various environments. Recent systematic studies have found a greater propensity for step bunching on the (0001) face,[23–26] with vicinal miscuts toward $\langle 1\bar{1}00\rangle$ displaying bunching of parallel steps into $(1\bar{1}0n)$ "nanofacets" up to $4-5$ unit cells in height, oriented at an angle of $\sim 25°$ to the basal plane.[24,25] It has been suggested that such nanofacet formation may be understood as a minimization of surface free energy.[24,27] Steps perpendicular to the directions $\langle 1\bar{1}00\rangle$ are strongly favored on (0001), such that steps formed macroscopically toward $\langle 11\bar{2}0\rangle$ are microscopically zigzagged, with segments perpendicular to $\langle 1\bar{1}00\rangle$.[23–26] The $(000\bar{1})$ face, by contrast, seems to form steps without restriction on orientation.[25] Step-bunched nanofaceting has not been observed there previously,[25,26] but we find [see Fig. S1] that a $(1\bar{1}0n)$ facet is induced by pre-processing (see below). These results are qualitatively true of both $6H$- and $4H$-SiC polytypes.[25] It is perhaps expected that epitaxial graphene growth should proceed first on nanofacets, given the lesser bonding of Si atoms there, and this has been observed on etching-induced $(1\bar{1}0n)$[19] and $(11\bar{2}n)$[28] nanofacets.

We propose exertion of control over the natural step bunching mechanism to prepare a crystal facet for self-organized graphene growth [see Fig. 1]. Given the previous discussion, the best choice for this purpose may be $(1\bar{1}0n)$. Controlled facets are achieved by photolithographic definition of Ni lines on a SiC substrate perpendicular to the $\langle 1\bar{1}00\rangle$ direction; these lines are transferred into the SiC by a fluorine-based reactive ion etch (RIE), which, while relatively simple technologically, allows nm-precision in the etch depth. As depicted in Fig. 1, it is the etch depth that ultimately defines the width of nanoribbons prepared. 20 nm etch depths were readily achieved in this work [see Fig. 3], which resulting ribbon width (~ 40 nm) is sufficiently narrow to result in a sizable band gap at room temperature.[2–4] Much narrower widths should be reachable with further development. After removal of the Ni mask and cleaning, the crystal is heated to elevated temperatures (1200 – 1300 °C) at intermediate vacuum (10^{-4} Torr) for 30 min., inducing SiC step flow. The abrupt step relaxes to a $(1\bar{1}0n)$ facet, and the temperature is elevated to > 1450 °C within

1.5 min., maintained for 10 min. for graphene growth, then allowed to cool naturally, falling below 1300 °C within 0.25 min.[1,5,16]

This careful control of growth temperature, time, and atmosphere allows selective growth on the facet, as shown by Raman mapping in Fig. 2f. The intensity of the 2D Raman band (2700 cm^{-1}) characteristic of graphene is mapped over a 100 nm SiC step and adjacent (0001) faces. Little to no intensity is observed on the horizontal surfaces, but significant intensity is seen at the step edge, indicating presence of graphene there. Note that the lateral resolution of the Raman instrument, at $\sim 1\,\mu$m, is much larger than the facet width and the mapping grid spacing.

Cross-sectional high-resolution transmission electron microscopy (HRTEM) images (with slightly thicker graphene for visibility) [see Fig. 2g] confirm preferential growth and afford observation of the nanofacet. Graphene is observed on the facet, with only partial layers on the horizontal (0001) plane. The facet angle observed, 24°, is in agreement with atomic force microscopy (AFM) measurements (not shown) of $24 - 28°$ across multiple samples and locations, corresponding to the high-index SiC facet $(1\bar{1}0n)$ as expected, where $n \approx 8$. The precise facet obtained is dependent on processing temperature.[23] It must be noted that apparent imperfections in the graphene sheets may be introduced by the HRTEM specimen (thin slice) polishing process or the high energy electron beam during imaging.

Electrostatic force microscopy (EFM, related to Kelvin probe FM) allows observation of narrower epitaxial graphene nanoribbons, as shown in Fig. 3. This probing of the local relative work functions differentiates epitaxial graphene on the nanofacet from the surrounding substrate (this correlates to mapping of the 2D Raman line), highlighting self-organized nanoribbons as shown in Fig. 3c. Here, the SiC step is 20 nm, and observed graphene ribbon width is $\lesssim 40$ nm. Note the three-dimensional structure, with epitaxial graphene interconnects bridged by nanoribbons, all self-organized on the prepared template.

Ribbon samples formed on $(000\bar{1})$ [Figs. 4a, 5b] were prepared for electrical measurement by exposure to an extremely short directional O_2 RIE to remove any graphene fragments from the horizontal $(000\bar{1})$ surface. This was verified by Raman mapping as shown in Fig. 2d, and extensive electrical probing confirmed lack of measurable conductivity on the horizontal surfaces. As discussed above, on (0001) [Figs. 2e-g, 3, 4b], the selective graphene growth required no post-processing, and device yield was better than 90%. Metal contacts were deposited for four-terminal measurements without gate and two-terminal measurements with

top gates. In the latter case, the graphene surface was functionalized by NO_2,[29] followed by atomic layer deposition (ALD) of Al_2O_3 and lift-off of a metal gate [see Fig. 1].

Four-terminal measurements of prepared ribbons [see Fig. 3 and insets, Figs. 4a and 4b] yield sheet resistances of 180 – 1000 Ω/sq., values typically observed in as-grown planar graphene.[6] Fig. 4a shows a series of conductance vs. source-drain voltage curves taken between 77 K and 4 K. The behavior is metallic at high temperatures, but quantum confinement is clearly manifested in the nonlinearity observed at 4 K, indicating presence of a small band gap, as expected of this ~ 250 nm-wide ribbon and in agreement with previous reports.[5]

Top-gated two-terminal measurement of similar devices at room temperature is presented in Fig. 4b. Though the NO_2-functionalization, one of a handful of recent techniques for enabling adhesion of high-κ dielectrics to graphene, is known to dramatically degrade mobility, on-off ratio, and electron-hole symmetry,[30] we observe large field-effect mobilities, between $\mu_{\mathrm{FE}} = 900$ and $2{,}700\,\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$, which values are comparable to or better than those previously reported at room temperature for ribbons of this dimension.[8,11,12] The Dirac point (resistance maximum) is typically observed at $V_{\mathrm{g\ Dirac}} \approx -4\,\mathrm{V}$, corresponding to an electron density at $V_{\mathrm{g}} = 0\,\mathrm{V}$ of $3\times10^{12}\,\mathrm{cm}^{-2}$, in agreement with numerous measurements of the first graphene layer above the SiC interface.[1,5,6,9,12] This indicates that the first graphene layer is modulated by the top gate and the graphene channel is not more than a few layers in thickness. The gating efficiency further confirms the selectivity of the growth. Recently devised dielectric adhesion methods are expected to result in improved performance by reducing interaction between the graphene channel and dielectric stack.[30]

Room temperature four-terminal current vs. source-drain voltage measurement of narrow (width $\lesssim 40$ nm) ribbons [see Fig. 3] is shown in Fig. 4c. While near-linear response is expected[2] in this ungated device due to large intrinsic electron density as discussed above, non-linearity is observed. Conductance does not decrease appreciably at 77 K. Gated measurements of similar devices at room temperature and 4 K are shown in Fig. 4d. The on-off ratio is ~ 10 at room temperature, and > 25 at 4K, with excellent symmetry. The gate in this case is Au on graphene with inherently large contact resistance; further details will be published at a later date.

Photolithographic processing allows fabrication of a large number of devices at higher density. An array of top-gated graphene transistors prepared on the $(000\bar{1})$ face of a 4×6 mm

SiC chip with SiC etch depth 100 nm (ribbon width $\sim$ 250 nm) is shown in Fig. 5a. A single device (source, drain, channel, and gate, as illustrated in Fig. 1) occupies a $35 \times 65\,\mu$m area, so the 0.24 cm^2 chip accommodates more than 10,000 transistors. This density was limited primarily by the size of the probe tips used for electrical measurement, but it is, to our knowledge, the highest density of graphene devices achieved to date. The room temperature gating effect is plotted in Fig. 5b.

It should be noted that there are likely fundamental differences in graphene growth among the possible SiC facets, analogous to the dramatic differences in growth speed and layer orientation observed on the (0001) and $(000\bar{1})$ faces,[6,16] and the $(1\bar{1}0n)$ facet chosen here is possibly not the most desirable in terms of selectivity and quality of graphene produced. This is particularly true of facets prepared on the $(000\bar{1})$ surface, where there is apparently more freedom in facet choice. This is a topic of ongoing investigation.

These results demonstrate that graphene growth on non-traditional crystal faces is viable and useful in device fabrication, particularly for production of nanoribbons on a large scale, and fabrication of graphene transistors at a density greater than 40,000 per cm^2 represents a milestone in the development of graphene electronics. Refinement of this approach will come with further reduction of ribbon width, development of three-dimensional device structures, and optimization of dielectric and facet selection. Importantly, damage to ribbon edges by violent cutting processes such as O_2 etching has been eliminated by a coalescence of top-down and bottom-up lithographies. Pre-patterning of the SiC substrate is, in general, a new and promising direction in the development of epitaxial graphene electronics, as complex structures and applications are readily envisaged.

Methods

Substrates were nominally on-axis research-grade semi-insulating $4H$-SiC from Cree, Inc. Arrays of Ni lines were defined on the (0001) or $(000\bar{1})$ SiC crystal face by a standard photolithographic lift-off process, and transferred into the SiC by a 43% SF_6/23% O_2/33% Ar RIE operating at 30 mTorr. RF power was tuned to give a SiC etch rate of 8 Å/s, allowing fine control of the etch depth. Ultrasonic treatment in nitric acid removed Ni from the SiC surface, and further cleaning and graphene growth proceeded as described previously.[1,5,16] O_2 RIE operating at 100 mTorr was tuned to give a graphene etch rate of $\sim$ 1 Å/s, and etch time on $(000\bar{1})$ faces was several to a maximum of ten seconds. Samples were

mounted with $(1\bar{1}0n)$ facet parallel to ion flux. Contacts were defined by e-beam or photolithographic lift-off of 5 nm Pd/60 nm Au. Atomic layer deposition (ALD) of 39 nm Al_2O_3 was performed as described by Williams *et al.*[29] in a commercial Cambridge Nanosystems Savannah ALD system prior to lift-off of an Al top-gate. Al_2O_3 does not deposit uniformly without an adhesion layer, and NO_2 functionalization was used in this case. The Al_2O_3 dielectric constant as deposited is $\kappa = 6$. Raman mapping was performed with excitation wavelength 532 nm, lateral resolution $\sim 1\,\mu$m, and $0.25 - 0.5\,\mu$m grid spacing. 2D intensity was taken at 2D maxima near $2725\,\mathrm{cm}^{-1}$. HRTEM measurements were performed by Evans Analytical Group in Raleigh, NC, USA, with acceleration voltage 200 kV. EFM data were obtained on a Park XE-70 in enhanced non-contact EFM mode with 2 VAC at $\omega = 17$ kHz on the tip, sample floating, and ω response (pictured in Fig. 3) monitored by lock-in amplifier. Electrical transport measurements were performed at atmospheric pressure. Field-effect mobility is calculated according to $\mu_{\mathrm{FE}} = dG/dV_g\ LW/C$,[8,12] where G, L, W, and C are square conductance, channel length, width, and dielectric capacitance, respectively, after subtracting contact resistance determined by four-terminal measurement of the device [see Fig. S2].

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Author contributions

W.A.dH. and C.B. conceived the project, and W.A.dH., C.B., M.S., and M.R. designed the experiment. W.A.dH. supervised the project, with assistance in supervision from C.B. M.S., M.R., and C.B. performed the experiment. Y.H., J.H., and B.Z. helped with sample preparation, M.R.R. helped with Al_2O_3 deposition, and X.W. and J.H. assisted with low temperature measurement. M.S. and C.B. analyzed the data, and M.S. wrote the paper.

Additional information

The authors declare no competing financial interests. Supplementary information accompanies this paper at www.nature.com/naturenanotechnology. Reprints and permission information is available online at http://npg.nature.com/reprintsandpermissions/. Correspondence and requests for materials should be addressed to W.A.dH.

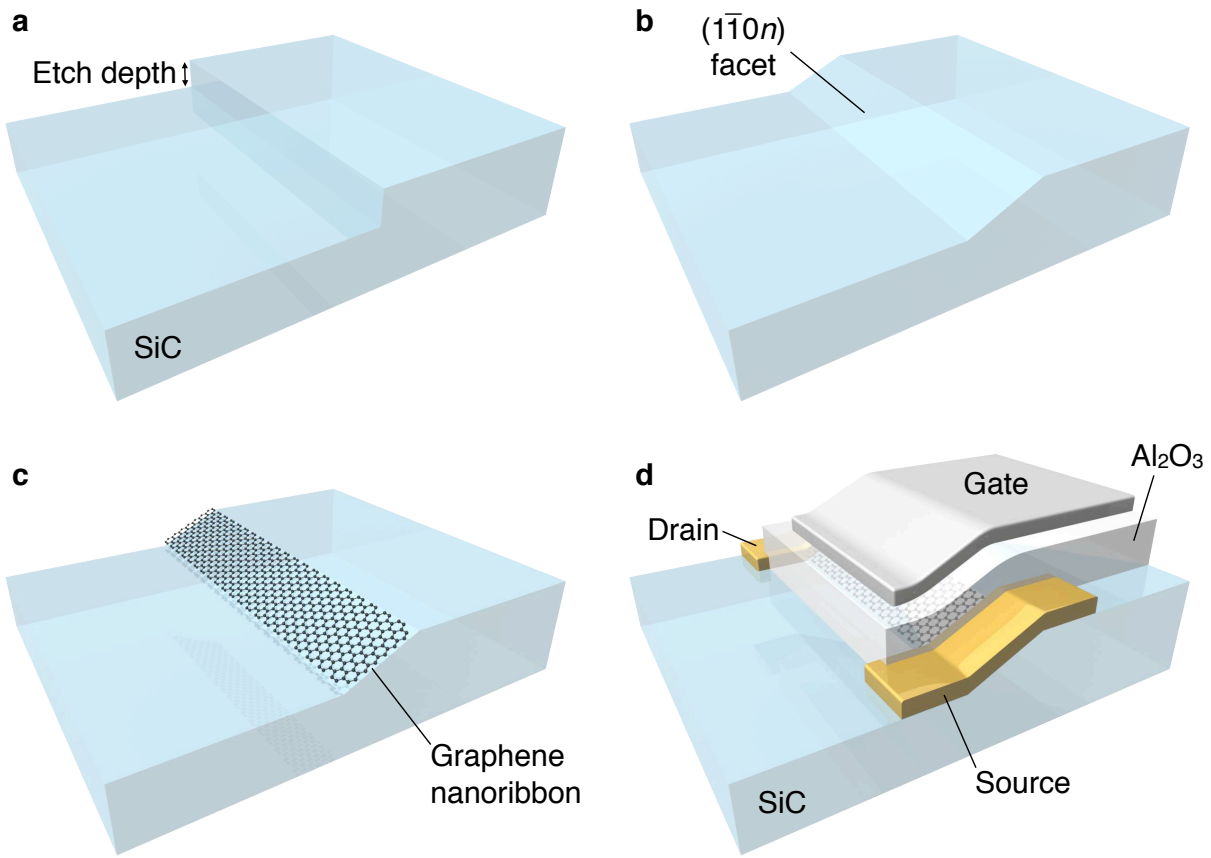

FIG. 1: Process for tailoring of the SiC crystal for selective graphene growth and device fabrication. (a) nm-scale step is etched into SiC crystal by fluorine-based RIE. (b) Crystal is heated to 1200 – 1300 °C (at low vacuum), inducing step flow and relaxation to the (1$\bar{1}$0n) facet. (c) Upon further heating to $\sim$1450°C, self-organized graphene nanoribbon forms on the facet. (d) Complete device with source and drain contacts, graphene nanoribbon channel, Al_2O_3 gate dielectric, and metal top gate, as pictured in Fig. 5b.

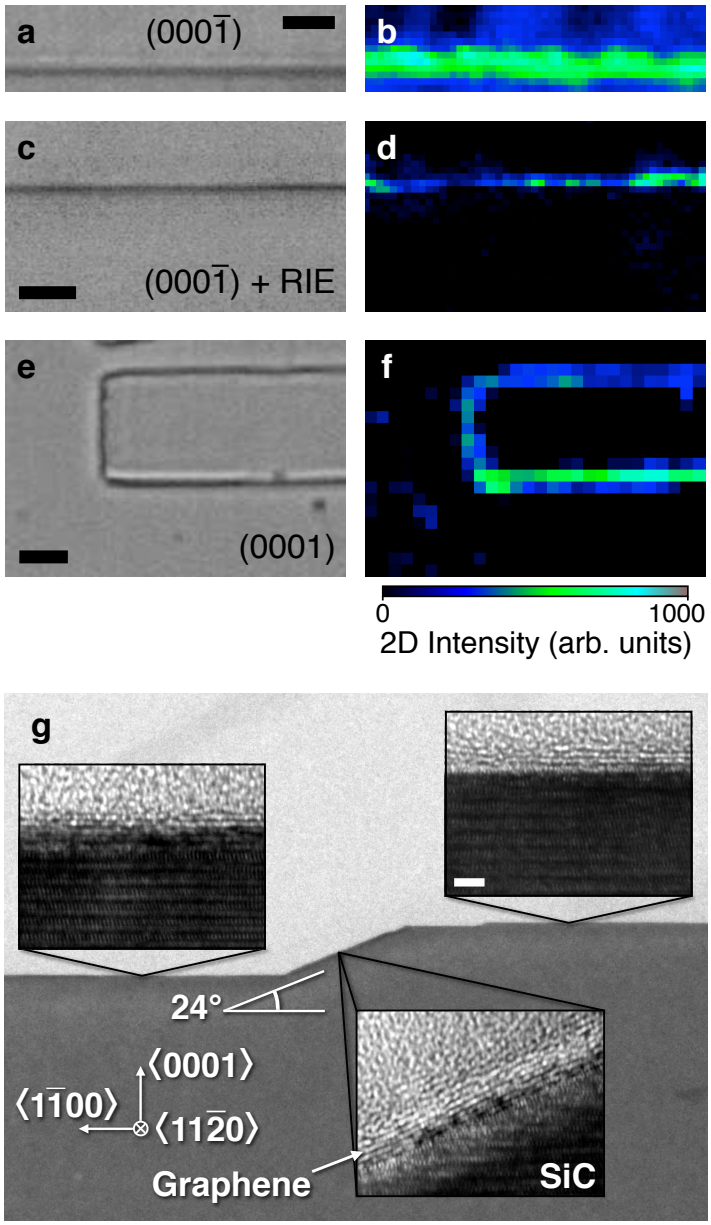

FIG. 2: Raman and TEM observations of graphene grown selectively on SiC nanofacet $(1\bar{1}0n)$ with $n \approx 8$. (a) Optical micrograph of pre-patterned 100 nm step on the SiC$(000\bar{1})$ face following graphene growth. Scale bars in (a, c, e) are 2 μm. (b) Raman map ($\sim$1 μm lat. res., 0.25 μm grid) of the 2D peak intensity at this location indicates preferential graphene growth on the $(1\bar{1}0n)$ facet. (c – d) Optical micrograph and Raman map of step on SiC$(000\bar{1})$ following exposure to directional O_2 RIE. (e – f) Optical micrograph and Raman map demonstrating fully selective growth on SiC(0001) without post-treatment. (g) HRTEM cross-sectional images of a similar step on (0001) confirm preferential growth on the $(1\bar{1}0n)$ facet. Scale bar is 2 nm, and applies to all insets.

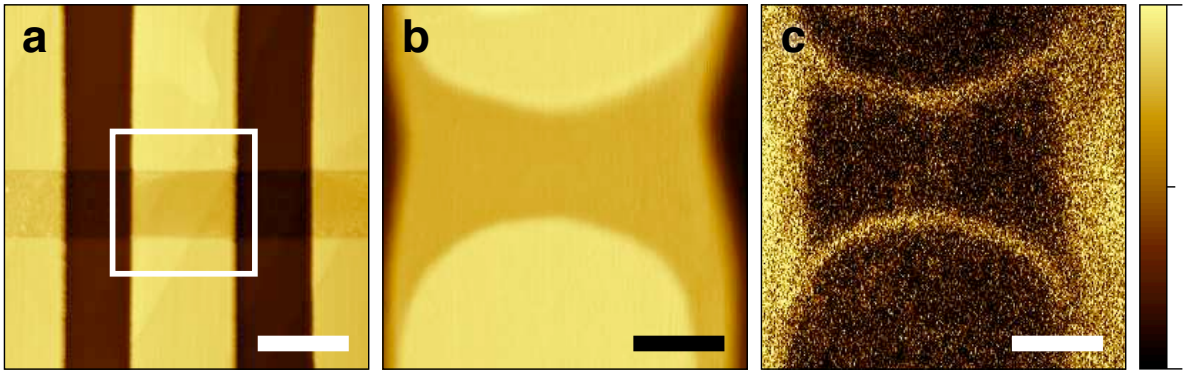

FIG. 3: AFM/EFM observation of self-organized epitaxial graphene nanoribbons of width $\sim 40\,\mathrm{nm}$. (a) AFM topography of patterned SiC structure on (0001) before graphene growth. Horizontal trench of depth 20 nm (to become the active device area) is flanked by trenches of depth 100 nm (to become interconnects). (b) AFM (topography) detail of white outlined area in (a) following graphene growth. SiC step bunching and step flow cause the patterned steps to become atomically flat semi-circular plateaus atop an atomically flat terrace. (c) Corresponding EFM amplitude (relative work function) detail highlights graphene nanoribbons on $(1\bar{1}0n)$ relative to surrounding substrate. Given finite size of the conducting probe tip ($\sim 20\,\mathrm{nm}$ radius), graphene nanoribbon width is estimated at $\lesssim 40\,\mathrm{nm}$. Wider interconnect-like graphene ribbons at left and right join the nanoribbon device to the larger circuit. Scale bars and color scales (far right) in (a), (b), and (c) are $1\,\mu\mathrm{m}$, $500\,\mathrm{nm}$, $500\,\mathrm{nm}$, $0-140\,\mathrm{nm}$, $0-87\,\mathrm{nm}$, and $3.7-4.4\,\mathrm{V}$, respectively. See electrical transport data in Fig. 4c.

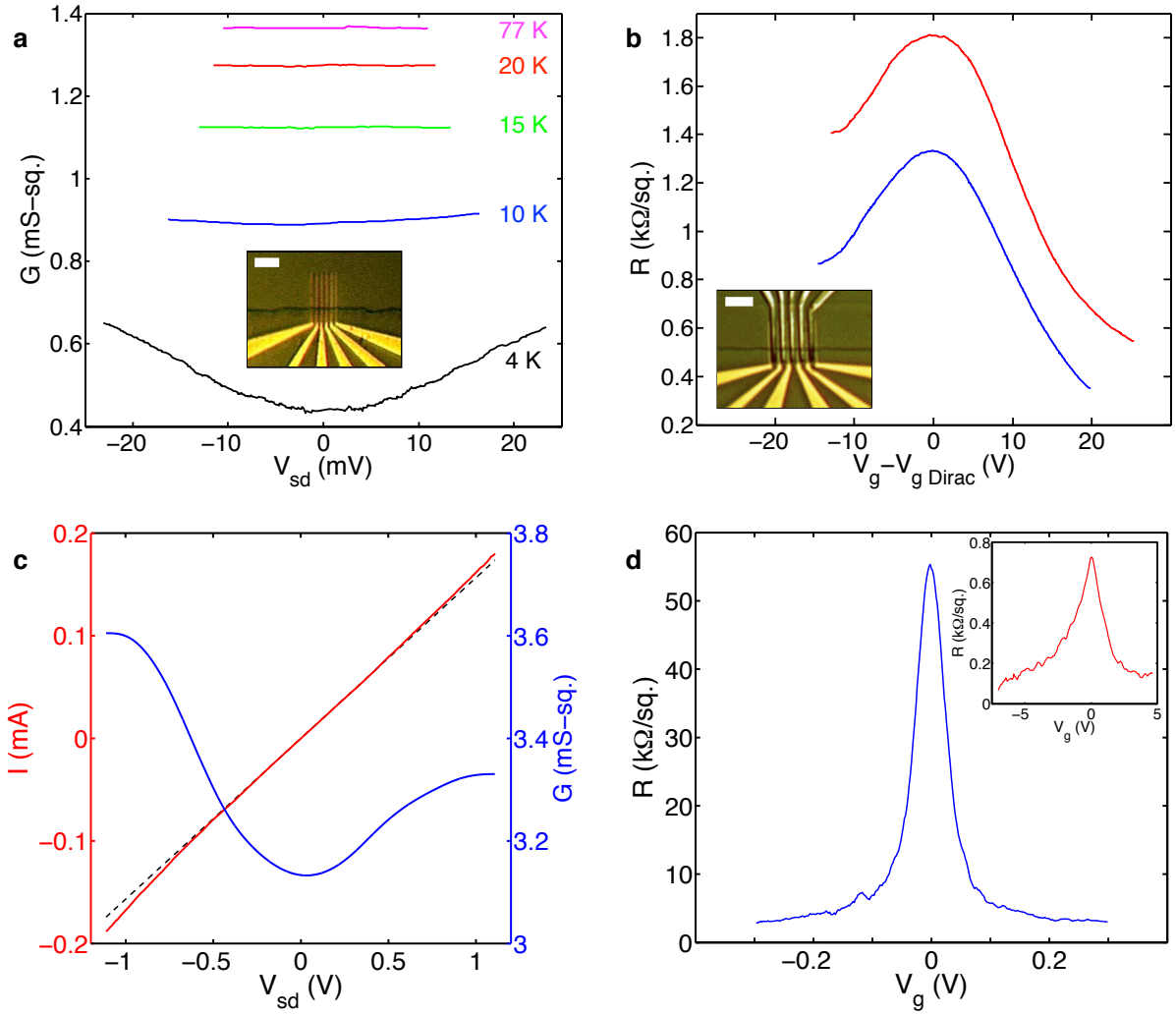

FIG. 4: Electronic transport measurement of graphene nanoribbons. (a) Conductance vs. source-drain voltage as a function of temperature. Band gap is observed at 4K as expected for a ribbon of this width (250 nm). Inset: optical micrograph of test structure. Scale bar is 15 μm; channel length is 3 μm. (b) Room temperature resistance vs. top-gate voltage, $V_{\rm g}$, relative to voltage at which Dirac point is observed, $V_{\rm g\ Dirac} \approx -4$ V, for two representative self-organized nanoribbons, red, and blue. Asymmetry and mobility degradation are due to interaction with NO_2 adhesion layer. Inset: optical micrograph of top-gated devices as studied here. Scale bar is 3 μm; gate length is 450 nm. (c) Room temperature current (red) and corresponding conductance (blue) vs. source-drain voltage for $\sim$ 40 nm-wide nanoribbon device shown in Fig. 3. Constant (minimum) conductance line, dashed black, is plotted for reference. Near-linearity is expected[2] in this ungated measurement due to large intrinsic electron density. (d) Gated measurements of $\sim$ 40 nm-wide nanoribbon devices at room temperature (inset) and 4 K.

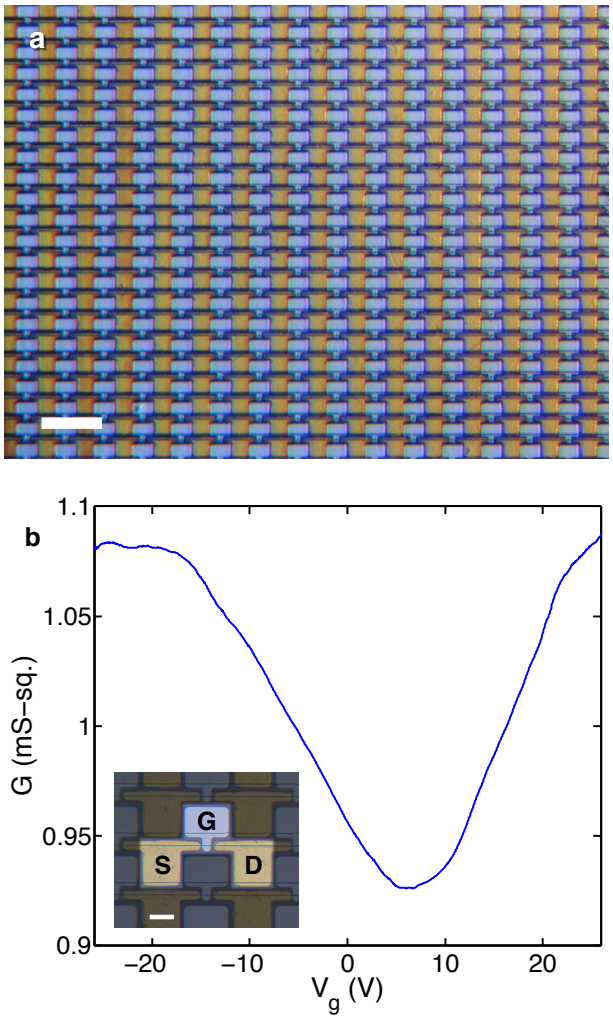

FIG. 5: Graphene transistor array with density 40,000 devices per cm^2 prepared on SiC(000$\bar{1}$). (a) Optical micrograph, scale bar 100 μm. (b) Room temperature ambipolar gating effect: conductance vs. gate voltage. Inset: an individual FET consisting of source (S), drain (D), graphene channel, and gate (G). Scale bar is 20 μm; channel length is 7 μm.