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# The DT-SJMOSFET: a new power MOSFET structure for high-voltage applications

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**Abstract:** New hybrid vehicles will probably use high voltage batteries (150 to 200 Volts). For these future automotive applications, the development of 600 Volts power MOSFET switches exhibiting low on-resistance is desired. The “Deep Trench SuperJunction” MOSFET (DT-SJMOSFET) is one of the new candidates. In this paper, a comparative theoretical study, using 2D simulations, shows that the DT-SJMOSFET should be a challenger to the conventional SJMOSFET in terms of “specific on-resistance / breakdown voltage” trade-off. Simulations of the DT-SJMOSFET breakdown voltage versus the technological parameters exhibit the difficulties to fabricate the device. Finally, an original edge cell is proposed that contains the peripheral potential.

**Keywords:** Power semiconductor devices, MOSFET, SuperJunction devices, Simulation.

## 1. Introduction

New hybrid vehicles will probably use high voltage batteries (150 to 200 Volts). For these future automotive applications, the development of 600 Volts power MOSFET switches exhibiting low on-resistance is desired.

Although, power MOSFET is commonly used in this voltage ranges, unfortunately its on-resistance ( $R_{ON.S}$ ) increases drastically with its breakdown voltage (BV). In fact due to the limitation of the maximum electric field, a high breakdown voltage requires the drift region to be lightly doped and thick, which then causes  $R_{ON.S}$  to be very high. The theoretical limit for the “ $R_{ON.S} / BV$ ” trade-off of conventional vertical power MOSFET is given by the relationship (1):

$$R_{ON.S}(\Omega.cm^2) = 8.3 \times 10^{-9} \times (BV)^{2.5} \quad (1)$$

The aim of this work is to address the rising need of this class of MOSFETs in future automotive applications, in which development of 600 Volts power MOSFETs exhibiting low on-resistance is desired.

Nowadays the Vertical Double diffused MOSFET structure — VDMOSFET — (Figure 1) is widely used as a power MOSFET. This structure is based upon the double diffusion of the P-body and  $N^+$  source regions using the edge of the polysilicon as a masking boundary. The voltage handling capability of this structure is given by the breakdown voltage of

the “P-body /  $N^-$  epilayer” junction, that is strongly dependent on the thickness and the doping concentration of the lower doped region (i.e. the  $N^-$  epilayer region in the case of N-channel VDMOS transistors) [1]. Today, advances in process technology have improved transistor’s packing density and consequently transistor’s specific on-resistance. However improvements in specific on-resistance have been limited by material and breakdown voltage, which required a relative thick and low doped epitaxial layer.

Recently, several MOSFET configurations have been proposed to reduce specific on-resistance while keeping a high breakdown voltage: the SuperJunction [2], [3] and semi-superjunction [4] devices. These devices recently attracted the attention of many researchers because they offer a good “specific on-resistance / breakdown voltage” trade-off around 600 Volts breakdown voltage [5], [6].

In this paper, a new 600 Volts vertical N-channel SuperJunction MOSFET called DT-SJMOSFT is proposed. These DT-SJMOSFET use a deep trench in the  $N^-$  drift layer as a new approach to form the vertical N and P pillars as oppose to the most widely reported technological fabrication of SJMOSFET that involves the repeated use of epitaxies and implantations in order to form these zones [2]. It will be shown that the DT-SJMOSFET exhibit an equivalent “ $R_{ON.S} / BV$ ” trade-off. Then an original edge cell will be proposed to contain the peripheral potential.

## 2. SuperJunction concept

### 2.1. Principle

Schematic cross-sections of the conventional Vertical DMOSFET (VDMOSFET), is shown in Figure 1. In the conventional structure, the  $N^-$  drift region is required to be lightly doped so that the depletion region sufficiently develops in the  $N^-$  drift region to sustain the blocking voltage. This lightly doped  $N^-$  drift region results in a high drift resistivity.

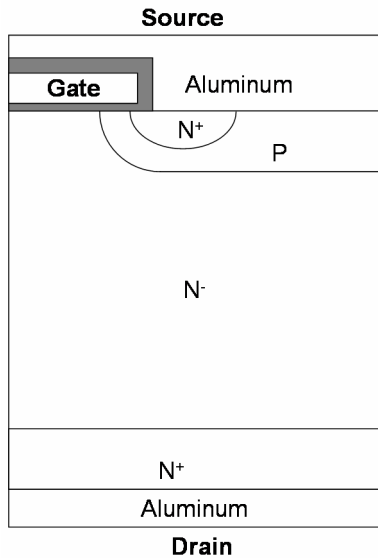


Figure 1: Schematic cross-section of a half-cell of a conventional VDMOSFET.

The SJ technology [3] is based on the charge compensation principle. The excess charge in the n-pillar is counterbalanced by the adjacent charges in the p-pillar (Figure 2). It allows the doping level of the n-pillars to be higher than that of the N<sup>-</sup> drift layer of the conventional MOSFET: then ultra low on-resistance below the Si-limit can be realized.

Considering both the lowest on-resistance and the highest breakdown voltage, P<sup>-</sup> and N<sup>-</sup> columns width and doping concentration are optimized in the way that the lateral and the vertical peak electric field are approximately equal.

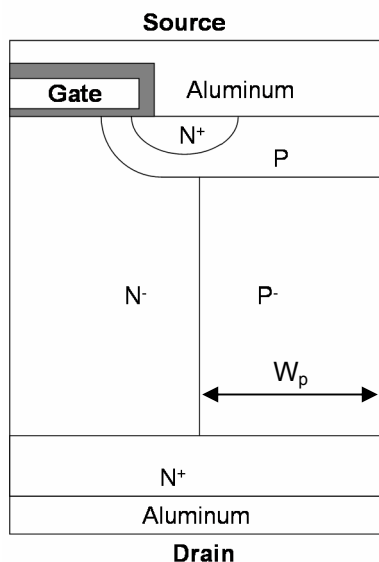


Figure 2: Schematic cross-section of a half-cell of a SJMOSFET.

The charge compensation principle, on the other hand, requires the precise control in the doping of P<sup>-</sup> and N<sup>-</sup> columns to realize low on-resistance and high

breakdown voltage because a small impurity imbalance between highly doped P<sup>-</sup> and N<sup>-</sup> columns causes large change of the electric field in the drift region and results in lower breakdown voltages. The relation between the doping concentration unbalance and the breakdown voltage has been published [7] to define critical process window for the P<sup>-</sup> and N<sup>-</sup> columns.

The newly DT-SJMOSFET concept (Figure 3), based on the VTR-DMOSFET [8], is a charge compensation structure like the SJMOSFET. The main difference with a SJMOSFET is the introduction of a deep trench in the N<sup>-</sup> epitaxial layer in order to realize the P-pillars necessary for the charge balance. These P-pillars are made by boron diffusion of a P<sup>++</sup> heavily doped polysilicon across a thin oxide in order to control the diffused dose. From a technological point of view, DT-SJMOSFET has some advantages. On one hand, it includes only one epitaxial growth step, compared to SJMOSFET. On the other hand, the oxide thickness and the thermal process enable an accurate control of the boron dose, compared to VTR-DMOSFET. Moreover, this structure can exhibit the same conduction area, compared to a SJMOSFET, because the area required by the P-pillars and the trench oxide in the DT-SJMOSFET ( $W_{\text{pox}}$ , Fig. 3) is approximately the same than the one required by the P-pillars in the SJMOSFET ( $W_p$ , Fig. 2).

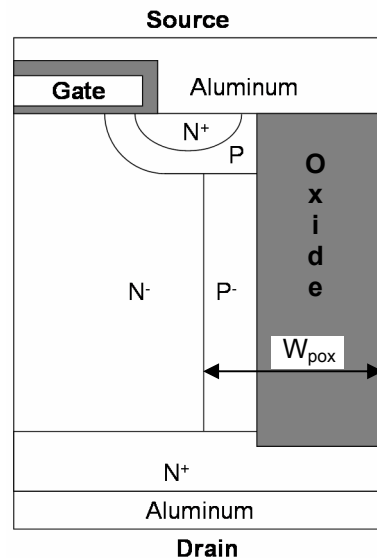


Figure 3: Schematic cross-section of a half-cell of a DT-SJMOSFET.

## 2.2. Device parameters

Conventional VDMOSFET, SJMOSFET and DT-SJMOSFET have been studied: Table 1 gives some important device parameters of these devices.

|   | Simulated Conventional VDMOSFET | Realized SJMOSFET [9]  | Simulated DT-SJMOSFET |
|---|---------------------------------|------------------------|-----------------------|
| N <sup>-</sup> epitaxial layer thickness (μm)                           | 51                              | 42                     | 50                    |
| N <sup>-</sup> epitaxial layer doping concentration (cm <sup>-3</sup> ) | 3 x 10 <sup>14</sup>            | 3.3 x 10 <sup>15</sup> | 3 x 10 <sup>15</sup>  |
| Central cell width (μm)   | 12                              | 12                     | 16                    |
| Breakdown voltage (V)   | 680                             | 680                    | 710                   |
| Specific on-resistance (mΩ.cm <sup>2</sup> )                            | 56                              | 15.5                   | 15.3                  |

Table 1: Main device parameters of the conventional VDMOSFET, a SJMOSFET and the DT-SJMOSFET.

Because of the voltage handling capability requirements (BV = 680 Volts), the N<sup>-</sup> epitaxial layer doping concentration required is 3 x 10<sup>14</sup> cm<sup>-3</sup> for conventional VDMOSFETs and 3.3 x 10<sup>15</sup> cm<sup>-3</sup> for a 12 μm width SJMOSFET [6]. The simulated DT-SJMOSFET parameters are a N<sup>-</sup> epitaxial layer with a doping concentration of 3 x 10<sup>15</sup> cm<sup>-3</sup> and a gaussian P-pillar with a boron peak concentration of 6 x 10<sup>16</sup> cm<sup>-3</sup> at the oxide/silicon interface. The total width of the trench is 4 μm for a depth of 50 μm. It is noteworthy that the boron peak concentration and the junction depth are chosen to fulfill the charge balance condition between the N and P-pillars.

### 3. Simulated static characteristics

This study concerns 600 Volts breakdown voltage DT-SJMOSFET device. In order to evaluate the structure, a simulated study was made on the central and edge cells on off-state and on-state.

#### 3.1. OFF-state behavior

##### Central cell

Concerning the OFF-state, 2D simulations of central cells of DT-SJMOSFET confirm what was expected: the maximal electric field is on the lateral P-pillar / N<sup>-</sup> epilayer junction.

The Figure 4 shows the electric field and net doping distribution, with the breakdown voltage applied between drain and source, in a half central cell of the DT-SJMOSFET. The breakdown voltage is determined by the vertical electric field in the SuperJunction structure. Under this condition the P-pillars and N<sup>-</sup> epilayer regions are completely depleted to sustain the voltage. Breakdown occurs in the P-pillar / N<sup>-</sup> epilayer junction and the electric field is constant along the entire junction. The oxide trench smoothes the lateral electric field but does not take part to the sustaining potential. These trenches need

to be the finest possible in order to keep a high width conduction area.

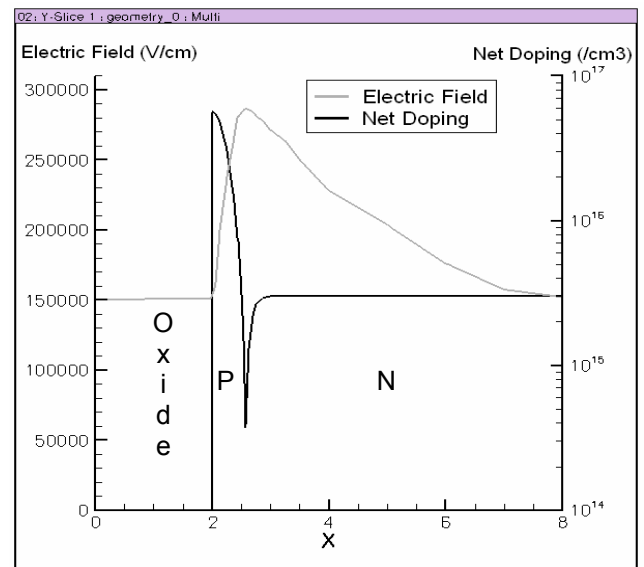


Figure 4: 1D lateral Electric Field distribution at breakdown in the middle of the trench.

##### Edge cell

A key issue in designing power devices is the breakdown termination (edge cell). An optimized and well-designed termination technique should shift the peak of the electric field from the surface to the bulk of the device. In the DT-SJMOSFET, the drawback of the increase in the N<sup>-</sup> epitaxial layer doping concentration is that the termination of the device has to be very efficient: actually, the higher doping concentration in DT-SJMOSFET implies that the conventional edge cell realized with planar guard rings or field plate are not sufficiently efficient and could induce a lower breakdown voltage. The proposed edge cell of the DT-SJMOSFET (Figure 5) includes a polysilicon field plate on top of an oxide trench (termination trench) that is larger than the one used in the central cell (8 μm). The principle of this termination is to contain all the potential in the last

oxide trench without additional process steps for the realization of the edge cell. This prevents aligning defects between the edge cell and the central cells, which secure the charge balance condition for the last base cell.

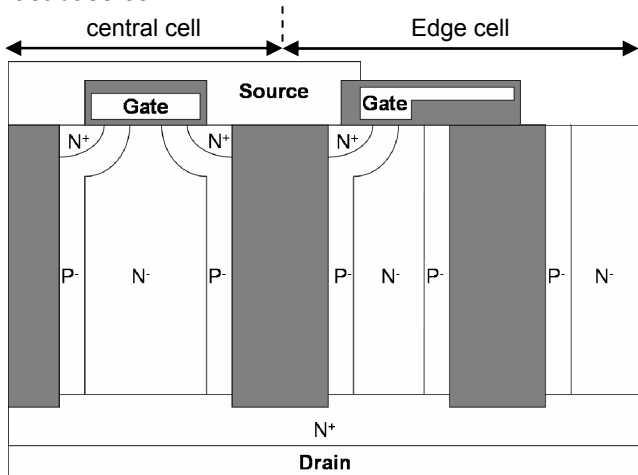


Figure 5: Schematic cross-section of the proposed termination.

The position of the edge trench needs to be optimized. The last central cell must polarize the floating P-pillars before reaching the critical electric field. The electrostatic potential distribution in the termination is presented in Figure 6. The drawback of this termination is that all the potential is sustained over the distance between the end of the field plate and the edge of the trench. It is necessary to optimize this distance in order to sustain the 600 Volts with the minimal width. The higher oxide critical electric field allows containing 91% of the central cell breakdown voltage in an 8  $\mu\text{m}$  width trench and 1  $\mu\text{m}$  between the end of the field plate and the edge of the tank.

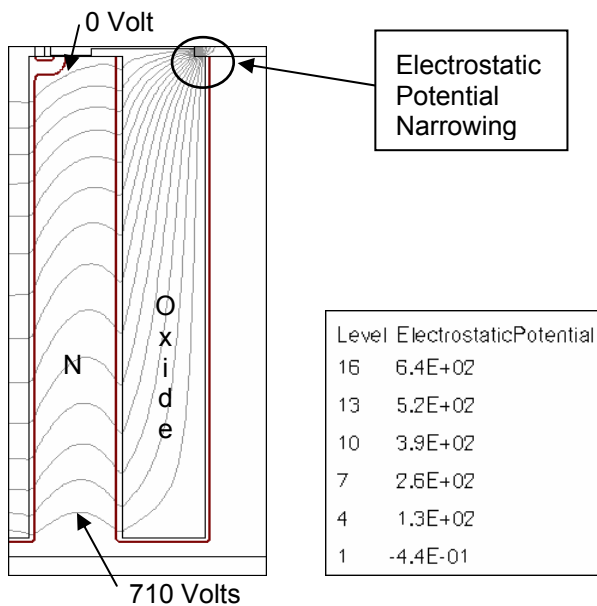


Figure 6: Electrostatic potential distribution in the termination.

### 3.2. ON-state behavior

Only the central cell of the DT-SJMOSFET is studied in the on-state because the edge cell does not take part in conduction.

The simulated breakdown voltage variations versus unbalanced diffused boron dose are presented in Figure 7. The simulations were made with a 16  $\mu\text{m}$  width base cell and a 4  $\mu\text{m}$  opening trench based on the laboratory possibilities in order to reach a better "specific on-resistance". In all cases, it can be observed that a light unbalanced boron dose would result in a dramatic decrease in the breakdown voltage. The higher the epitaxial doping concentration is, which is the most interesting case in the on-state (Figure 7) is, the lower the maximal breakdown voltage is. Because of this strong sensitivity to the boron dose, we will choose a weaker epitaxial doping concentration to fabricate DT-SJMOSFETs ( $3 \times 10^{15} \text{ cm}^{-3}$ ) exhibiting the best trade-off between the breakdown voltage, the specific on-resistance, and facility of manufacture.

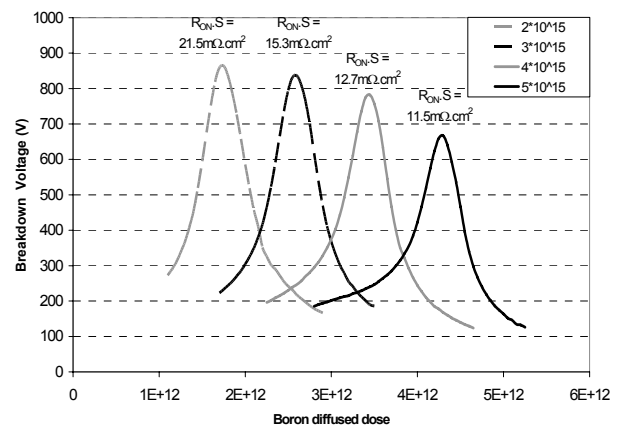


Figure 7: Breakdown voltage variations vs diffused P-type dose, for different epitaxial doping concentrations. Specific on-resistances are also given.

### 4. Parameters sensitivities

Some parameters sensitivity simulations will be discussed in order to evaluate the static performances evolution. At first we present the influence of parameters which affect the most the charge balance condition in central cell. These parameters will include the trench width ( $W_T$ ), the diffused boron dose ( $D_B$ ) and the trench verticality. Other parameters have been studied like the gate shape, its position or the P-body dose. They are not presented in this paper because they have a little effect on the specific on-resistance or on the breakdown voltage. The edge cell is also presented. The field plate length variation ( $L_{FP}$ ) and the last cell width ( $W_A$ ) are simulated in order to evaluate the parameters sensitivities.

#### 4.1. Trench profile sensitivity

##### Over-etching compensation

The simulations were made with a 16  $\mu\text{m}$  width base cell, a 4  $\mu\text{m}$  opening trench, an epitaxial layer doping concentration of  $3 \times 10^{15} \text{ cm}^{-3}$  and a constant boron diffusion length at 0.6  $\mu\text{m}$ , in order to reach a better current density. The simulated breakdown voltage variations (BV) versus trench width ( $W_T$ ) and diffused boron dose ( $D_B$ ) are presented Figure 8. It can be observed that the breakdown voltage is sensitive to both parameters; this is mainly a charge unbalance issue. For example, for a fixed boron dose, a variation in the trench width ( $W_T$ ) will change the number of N carriers. Then it can induce an unbalanced charge in either side. In the same way, for a fixed value of  $W_T$ , a variation of the diffused dose induces an unbalanced charge. In both cases, this charge unbalance will result in the variation of the breakdown voltage. However, the variations of the active area width can be corrected by adjusting the diffused boron dose so we get the best results on the line defining the charge balance. Boron dose and active area width have a poor influence on the "specific on-resistance".

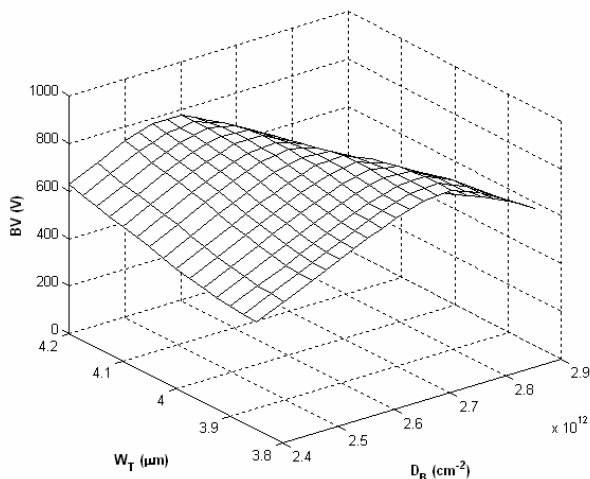


Figure 8: Breakdown voltage (BV) variations vs diffused P-type dose ( $D_B$ ) and deep trench width ( $W_T$ ).

##### Trench Verticality

The simulated breakdown voltage variations versus the trench slope defined by the difference ( $W_{BT} - W_{TT}$ ), where  $W_{BT}$  and  $W_{TT}$  are the width at the bottom and the top of the trench respectively (Figure 9), are presented in Figure 10. The chosen values for trench slope in these simulations are based on study results made in our team on realizing high aspect ratio deep trenches for integrated MIM capacitors applications [9]. This study used a time multiplexed Inductively Coupled Plasma etcher and a Bosch etch-process where an etching gas ( $\text{SF}_6$ ) and passivation gas ( $\text{C}_4\text{F}_8$ ) are used alternatively [10]. Results showed that deep trenches with an aspect-ratio of 12 can be

realized with a slope of about  $\pm 0.5 \mu\text{m}$  where the slope sign depends strongly on etching conditions (platen power, pressure, passivation / etching time ratio, ...) [11-13]. Our simulation results show that verticality of the trench is a critical parameter, particularly the negative slope case. The asymmetry is not yet confirmed but we think that in the case of positive trench slope, the N-type carriers deficiency in the bottom of the N<sup>-</sup> epilayer is counterbalanced by the N carriers in the N<sup>+</sup> substrate. This enables a deeper depletion in the epilayer for small bias variation explaining the increase of the breakdown voltage. Consequently, the trench verticality is necessary to insure equivalent performance with the SJ-VDMOSFET.

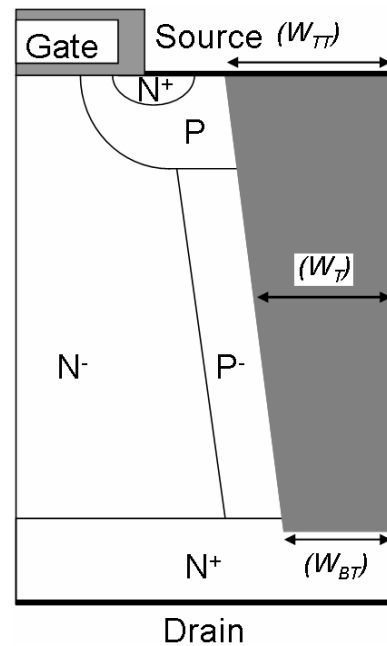


Figure 9: Schematic cross-section of a half-cell of a DT-SJMOSFET with the simulated parameters.

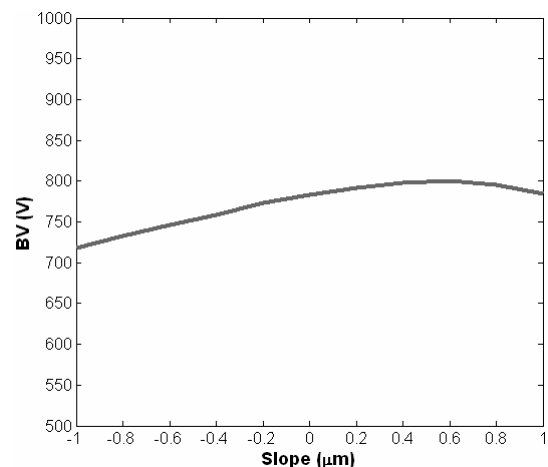


Figure 10: Simulated breakdown voltage (BV) variations versus trench slope.

## 4.2. Edge cell

### Field plate length

The simulations were made with a  $9\ \mu\text{m}$  width edge cell ( $W_A$ ), a  $8\ \mu\text{m}$  opening edge trench and  $1\ \mu\text{m}$  oxide field plate thickness. The simulated breakdown voltage variations versus the field plate width ( $W_{FP}$  defined on Figure 11) are presented Figure 12.

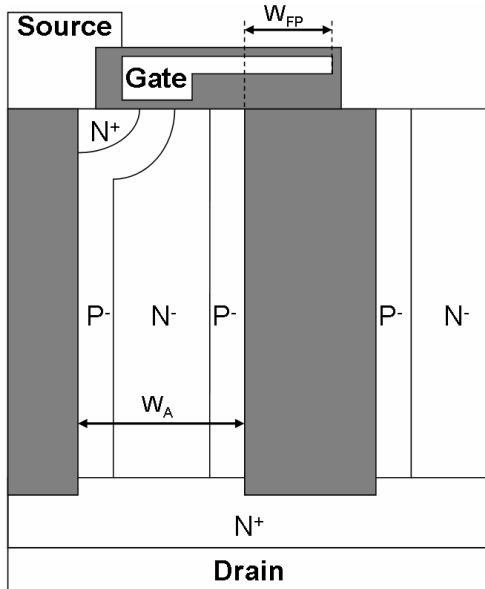


Figure 11: Schematic cross-section of the edge cell with the simulated parameters.

Our simulation results show that the breakdown voltage is not sensitive to the field plate width. Nevertheless the electric field between the end of the field plate and the end of the trench increase with the field plate width. The simulations do not present an oxide breakdown, but the electric field is close to  $10^7\ \text{V}\cdot\text{cm}^{-1}$  with the field plate wider than  $7\ \mu\text{m}$ . It is necessary to note that the edge cell sustains around 91% of the breakdown voltage of the central cell in the better conditions with a  $1\ \mu\text{m}$  oxide field plate.

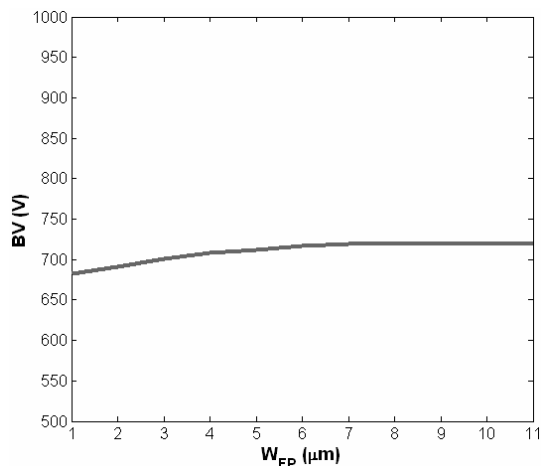


Figure 12: Simulated breakdown voltage (BV) variations versus field plate width ( $W_{FP}$ ).

In order to increase the breakdown voltage of the edge cell, it is necessary to increase the trench width. The problem comes from the filling of the trench. The wider the opening edge trench is, the more the filling time and the depth trench increase. Then, a  $8\ \mu\text{m}$  opening trench is a good trade-off between the manufacture and the breakdown voltage.

### Last edge width

The simulated breakdown voltage variations versus edge cell width ( $W_A$ , Figure 11) are presented in Figure 13.

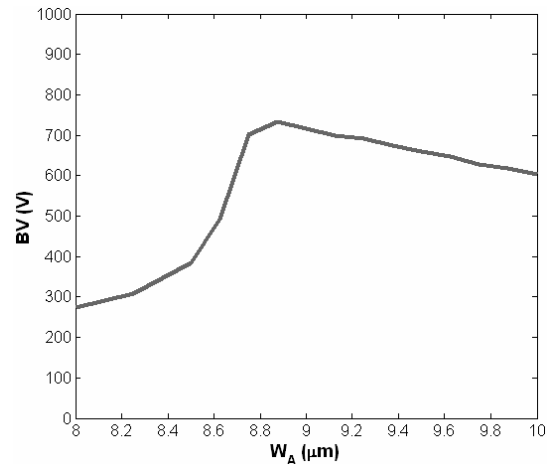


Figure 13: Simulated breakdown voltage (BV) variations versus edge cell width ( $W_A$ ).

Simulation results show that the breakdown voltage is very sensitive to the edge cell width, particularly for the values below  $9\ \mu\text{m}$ . The floating P-pillar is polarized when the depletion layer reaches the P-pillar /  $N^-$  epilayer junction. So, the wider the edge cell is, the more the P-pillar begins to create a depletion layer late. For width values lower than  $9\ \mu\text{m}$ , the two P-pillars are very close. The P-type excess carriers are not completely depleted by the N-type carriers in the substrate because the high doping level in the P-pillars ( $6 \times 10^{16}\ \text{cm}^{-3}$ ) is too important and the critical breakdown voltage value is rapidly reached.

In an optimal situation, the P-body and the left edge cell P-pillar continue to create a depletion layer until the floating P-pillar is reached. Then, the two P-pillars create a depletion layer until there is no P-type carrier. In the case of  $W_A$  values larger than  $9\ \mu\text{m}$ , one can expect an excess of N-type carriers in the epilayer. However, the effect of these excess carriers will be partially compensated by the heavily doped P-body.

To control this parameter ( $W_A$ ), the edge trench and the central trenches are recommended to be made in one step which will avoid the unintentional variations in  $W_A$  values due to the alignment errors. Even so, it is still important to consider the lateral trench over-etching. In order to keep an edge cell width upper than  $9\ \mu\text{m}$ , the over-etch effect has to be considered during the masks conception.

## 5. Conclusion

In this paper, a new vertical N-channel Superjunction MOSFET called DT-SJMOSFET dedicated to hybrid vehicle applications has been proposed with an original edge cell containing the peripheral potential. These DT-SJMOSFETs use a deep trench in the N<sup>-</sup> drift layer in order to form vertical N and P pillars, whereas the most widely reported technological fabrication of SJMOSFET involves the repeated use of epitaxies and implantations. The study has shown that the electric performances are very sensitive to the charge unbalance, but the sensitivity can be reduced by decreasing the epilayer doping concentration at the expense of the specific on-resistance. However to fabricate a DT-SJMOSFET exhibiting the highest breakdown voltage capacity, we must control accurately the trench shape (width, slope) to ensure the charge balance. The termination still needs to be controlled, notably the edge cell width in order to keep the charge balance.

The study needs to be completed with dynamic and thermal simulations. Moreover, the internal diode needs to be optimized in order to use it in switching mode. However, the realization of this structure remains difficult because the performances are very sensitive to the technological parameters' variations. The deep trench process, using boron diffusion across a thin oxide to realize P-pillars, is now in progress in order to validate the concept of the DT-SJMOSFET: we plan to fabricate 600 Volts Deep Trench diodes, to verify the edge cell, and DT-SJMOSFETs in the near future.

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MOSFETs (FLIMOSFETs) and Deep Trench SuperJunction MOSFETs (DT-SJMOSFETs).



**K. Isoird** received the M.S. degree from university of Montpellier and the PhD degrees in electrical engineering from the national institut of applied science of Lyon, France, in 1997 and 2001 respectively. From 2001 to 2003 she was post-doc at PEARL (Power Electronics Associated Research Laboratory) and LMP (Laboratory of Power Microelectronic). Since 2003 she is assistant professor at the university of TOULOUSE and She develops research activity on semiconductor power devices, within ISGE (System Integration for power management) team of LAAS (Laboratory for Analysis and Architecture of Systems).



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