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Extra-low parasitic gate-to-contacts capacitance architecture for sub-14 nm transistor nodes

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A B S T R A C T

We investigate in this work an original contact architecture to address 64 nm pitch transistor technology. This architecture, studied here in the fully-depleted silicon-on insulator (FDSOI) flavour, remains suitable for planar and 3D (trigate, FinFET) approaches. It includes a recessed gate-first process and self-aligned contacts that offer alternative solutions to technological problems such as limits in lithography resolution and stepper misalignment.

Because this type of contact architecture is likely to increase parasitic coupling between gate and source/drain (S/D) contacts, a set of optimization rules is proposed based on numerical simulations.

It is found that reducing gate thickness remains the best option to decrease the parasitic gate-to-S/D contact capacitance when transistors feature standard nitride spacers. The use of a low permittivity and thick gate capping layer is highly recommended to limit the sensitivity of parasitic capacitances to non-uniformity associated to chemical mechanical polishing (CMP) and stepper misalignment during S/D contacts lithography.

When low-k spacers are considered, the same optimization rules are still relevant to further decrease parasitic capacitances at the transistor level. In the particular case of airgap spacers, they result in a 50% reduction of the total parasitic capacitance. Nevertheless, when used alone, low-k spacers can reduce parasitic coupling by up to 80%; they appear as a first order parameter to tune parasitic capacitances.

At the circuit scale, it is demonstrated that an optimized architecture including low-k spacers is mandatory to meet the specific 10 nm node speed requirements at the circuit level. Insights are finally given to correctly choose the active area width W and supply voltage V_{DD} taking into consideration the speed/power consumption trade-off. We particularly showed that if a voltage value lower than the nominal supply voltage is used, spacers optimization become even more effective to reach higher circuit speed at constant dynamic power consumption.

Keywords:

Self-aligned contacts

FDSOI

Parasitic capacitance

Delay

1. Introduction

Over the last 40 years, device scaling has remained the fundamental engine of conventional microelectronics to achieve the gain in performance, productivity and cost. Following this trend, CMOS technology has witnessed a tremendous decrease in dimensions, leading to the demonstration of fully operational integrated circuits including a gate length approaching 20 nm [1].

Along with this reduction of dimensions, contacts module has reached a critical point in the fabrication of advanced technological transistors. For sub-14 nm nodes, the increased density of devices

makes the fabrication of source/drain contacts harder, given the reduced space between two adjacent transistors and the limitations of lithography resolution.

As for the 14 nm technological node, the use of a classical integration scheme for the realization of source-drain contacts becomes nearly impossible for the 10 nm node and beyond. In this paper, an original integration architecture is proposed, including an insulated recessed gate and self-aligned S/D contacts. We specifically considered a gate first approach; however this integration scheme can also be implemented with a gate last approach.

Because self-contacts are by definition in closer proximity to gates, they are likely to add parasitic effects to the operating device and circuit. As a consequence, the capacitive behavior of such structure is being studied. Possible optimizations of some

technological parameters are also investigated in order to limit the increase of capacitance at the device scale. Effectiveness of such optimizations at the circuit scale is finally evaluated in terms of delay and power consumption, considering performance requirements of the 10 nm technology node.

2. Self-aligned contacts integration: proposed process flow

In the case of the 10 nm technological node, each 14 nm gate length device features an associated gate-to-gate pitch of 64 nm. This leaves at maximum 50 nm between two consecutive gates sharing a common S/D to accommodate two sidewall spacers and one contact.

Given such density, patterning source–drain contacts by optical lithography in a classical way becomes risky because lithography misalignment of only a few nanometres produces an overlap between gate and S/D contacts, resulting in an electrical short. Formerly, optimized Self-Aligned Contacts (SAC) etch processes combined to a protecting Contact Etch Stop Layer (CESL) have been implemented for dense architectures such as DRAM cells ensuring electrical isolation between word line and bit line [2]. However, such a solution is unsuitable to a 64 nm pitch technology, especially because of the insufficient space to deposit the CESL between two consecutive gates.

To face the challenge of the 10 nm node onward, an original device structure is proposed as illustrated in Fig. 1 in the FDSOI case. Compared to a classical contact scheme where the S/D contact is filled using a single process step, the presented architecture exhibits two independent contact levels. The first one, referred to as *pre-contact*, is obtained by filling with metal all the space available between two consecutive gates spacers (Sp.). Pre-contacts are thus self-aligned to gates, providing a solution to the limitations of lithography resolution. Additionally, the fact that pre-contacts fully occupy space between two consecutive gates is a major trademark of this approach. Compared to what can be found in previous work on aggressive nodes [1,3], the surface of the S/D silicide layers is entirely contacted. This characteristic helps optimizing the contact resistance at the silicide/pre-contact interface, as the contact surface is maximized.

The second level of contacts is structured with a classical process and is therefore potentially prone to lithographic misalignment. To cope with the associated problem of electrical short, gates over active areas are recessed and capped with a dielectric layer (Diel.) as shown in Fig. 1, which constitutes a specific characteristic of the device architecture proposed here [4].

The fabrication of the proposed structure starts with the patterning of gate stack (high-k dielectric/metal/polysilicon) on a

SOI substrate. Spacers are successively deposited and etched, before implantations and faceted raised sources drains (RSD) epitaxy are realized. Second spacers are subsequently deposited and etched, followed by source–drain silicidation and pre-metal-dielectric (PMD) encapsulation. This last layer is planarized to allow for a partial recess of the gate polysilicon layer. This recess is realized everywhere except where further gate contacts are needed. Gate silicidation is performed. The recessed gate cavities are then filled with a dielectric capping layer.

Source–drain pre-contacts are realized by selective etching of PMD lying between consecutive gates, while masking parts that must not be etched like STI (Shallow Trench Isolation) trenches. This step is followed by deposition of metal and polishing. Contacts over source drain pre-contacts are finally etched through PMD and CESL layers.

3. Simulation results and discussion

3.1. Modeling parameters for capacitance extraction

Gate-to-S/D contacts coupling is known to add parasitic capacitive effects that have negative consequences in terms of speed and power consumption in an operating circuit. This is especially true for small gate length transistors, where this component, along with the overlap capacitance, becomes the major contributor to the total parasitic capacitance of the device [5]. In the proposed structure, self-aligned contacts are likely to amplify this parasitic coupling, as the gate-to-contact spacing is reduced [6]. The accurate quantification of this coupling component is therefore essential to carefully assess the viability of the proposed architecture.

Analytical equations have already been developed in the literature to evaluate parasitic coupling on a very large range of devices, including planar FDSOI transistors [7]. However, the structure studied here presents some original aspects which are not taken into account, such as the gate capping layer located between spacers.

As a consequence, 2D capacitance simulations were carried out to evaluate the impact of self-aligned contacts on the overall capacitive behavior of the structure, taking into account the effect of the gate capping layer. In the simulated structure, materials are considered either conductors or insulators. Particularly, the gate, raised source–drain and contacts are approximated as an ideal metallic material. It is assumed that the electrostatic landscape in the underlying semiconductor layers have a negligible impact on the electric field distribution between the gate and S/D. Based on this assertion, coupling effects in the contact layers can be thoroughly calculated by solving the Laplace equation because no

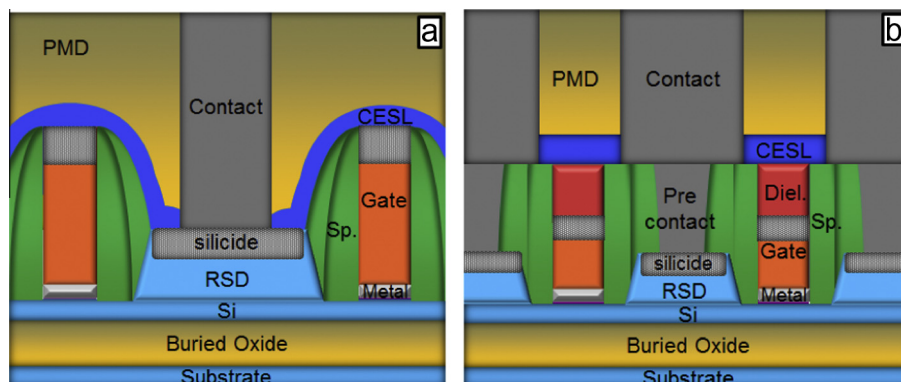


Fig. 1. Comparison of two MOSFET structures with standard contacts on raised source–drain (RSD) etched through pre-metal dielectric (PMD) and contact etch-stop layer (CESL) (a), vs. self-aligned contacts (b). The self-aligned approach remains unaffected by a lithographic misalignment of contacts as illustrated here.

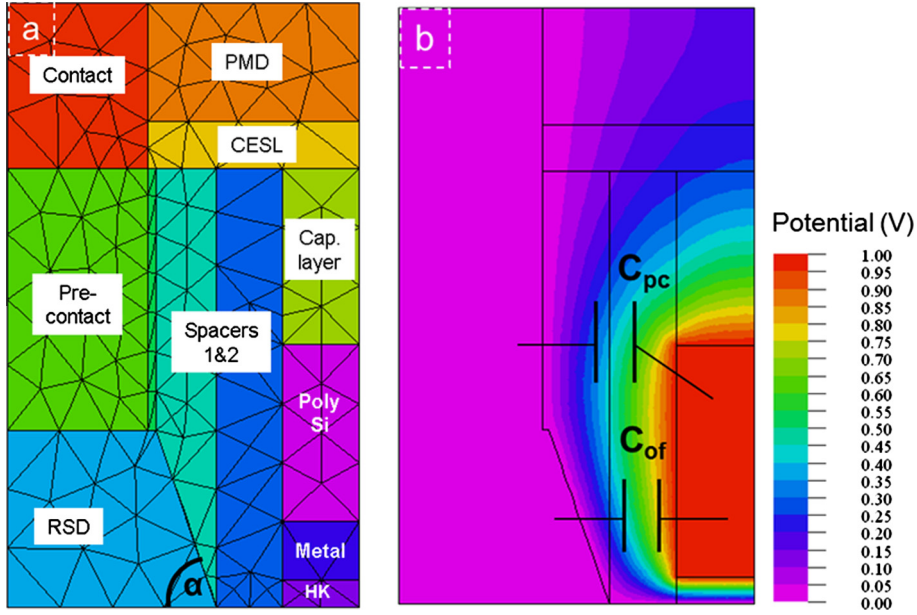


Fig. 2. Representation of the meshed structure obtained in the finite element analysis (a) and the corresponding electrostatic potential mapping generated by solving Laplace equation (b).

space charge need to be accounted for. As only the coupling between gate and source–drain contacts is being studied here, the channel region is not included in the analysis. A finite element method is used on the half meshed structure presented in Fig. 2a.

The total capacitance C between the gate and the source (or drain) is given by Eq. (1):

$$C = \frac{2 \cdot E}{(V_G - V_D)^2} \quad (1)$$

where V_G and V_D are respectively the gate and contact voltage. E is the energy in the whole structure that can be found with the help of Eq. (2). F is the local electric field, ϵ the dielectric constant of the material separating the gate and contact, and τ the volume of integration.

$$E = \iiint \frac{\epsilon \cdot F^2}{2} d\tau \quad (2)$$

The gate potential is set to 1 V while the S/D contact is set to the ground potential. In this configuration, a mapping of the electrostatic potential is obtained as shown in Fig. 2b.

The total parasitic capacitance of this structure can be divided into two main components: C_{of} , which corresponds to coupling between the gate and raised S/D (RSD), while C_{pc} characterizes the gate-to-contact coupling. Both of these capacitances are depending on geometrical and physical parameters (no V_G dependence) [7,8].

The C_{pc} component can divide itself into two components: $C_{pc_{||}}$ and $C_{pc_{fr}}$, which are respectively the parallel and fringe gate-to-contact components.

The parameters used for simulations are summarized in Table 1, some of which having fixed values. It is worth noting that RSD epitaxy angles are chosen based on previous studies showing reduced fringe capacitance due to facets [9]. Since no overlap between gate and Lightly-Doped-Drain (LDD) is considered here, the associated capacitance C_{ov} is taken as equal to 0.

The total parasitic capacitance associated to the gate-to-S/D contacts coupling ($C_{tot} = C_{of} + C_{pc}$) calculated from the proposed structure with the parameters given in Table 1 is 0.38 fF/ μm . This high value, inherent to the self-aligned architecture, already

Table 1

Detailed list of parameters used in simulations. In italic are examples of dimensions and materials for regions with varying parameters. Other values are fixed. Although the former are not optimized in terms of parasitic capacitances, they are technically feasible in terms of process.

Region	Dimensions	Material
Gate dielectric	Thick. = 2.3 nm	High-k, $\epsilon_r = 20$
Gate metal	Thick. = 5 nm	Metal
PolySi gate	Gate length = 14 nm (L_g), thick. = 40 nm	Metal
Capping layer	Thick.=10 nm	High-k, $\epsilon_r = 20$
Spacer 1	Thick. = 6 nm (tsp1)	Nitride, $\epsilon_r = 7$
Spacer 2	Thick. = 6 nm (tsp2)	Nitride, $\epsilon_r = 7$
RSD	Thick. = 15 nm 70° facet (NMOS case)	Metal
Pre-contact	Length = pitch- L_g -2 \times (tsp1 + tsp2)	Metal
Contact	Length = 26 nm	Metal
CESL	Thick.=4 nm	Nitride, $\epsilon_r = 7$
PMD	Thick.=36 nm	SiO ₂ , $\epsilon_r = 3,9$

exceeds ITRS specifications [10] for the 10 nm node technology, which only considers the outerfringe capacitance C_{of} in its prediction. As a consequence, an optimization of the proposed architecture needs to be carried out in order to reduce this figure and thus limit its impact on the dynamic performance at circuit level.

3.2. Parameters optimization

Among all the capacitive parasitic components of a transistor, this study focuses on the gate-to-contact parallel component ($C_{pc_{||}}$), which can be considered as a simple parallel plate capacitance. As for C_{of} , minimizing its value can therefore be achieved by reducing the gate height [7,11].

Considering that the gate resistance is mainly governed by the resistivity of the gate silicide layer, the fabrication process presented here allows for a recess of the polysilicon layer that reduces the gate height without any substantial increase of the resistance.

Fig. 3 shows the evolution of the total parasitic capacitance $C_{of} + C_{pc}$ as function of polysilicon thickness, for various capping materials. In anticipation of the final metal polishing step, different capping materials were investigated to avoid any damage to the

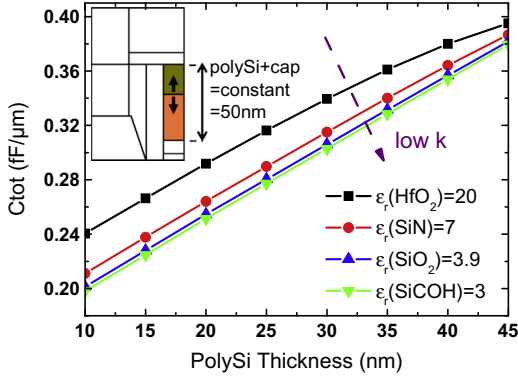


Fig. 3. Simulated variation of the parasitic gate-to-S/D contact capacitance as function of polysilicon layer thickness (cf. inset), for various capping materials.

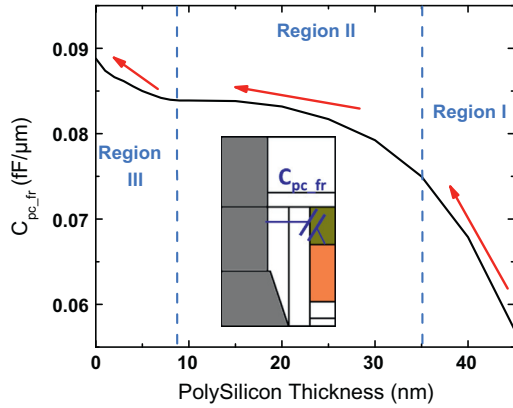


Fig. 4. Evolution of the gate-to-contacts fringing capacitance due to a recess of the gate's polysilicon layer (capping layer permittivity is $\epsilon_r = 20$).

structure. In spite of its high permittivity, HfO_2 is an example of capping material recognized for its good mechanical resistance to CMP. Other materials with lower permittivity were also studied.

Here, the sum of polysilicon thickness and capping layer thickness was fixed to 50 nm, in order to respect an aspect ratio comparable to those of recent technological nodes.

As expected, recessing the polysilicon layer is very effective to reduce the total capacitance of the structure. Thinning the 40 nm thick polysilicon layer down to 10 nm leads to a reduction of the coupling capacitance ranging from 40% to 50%, depending on the high or low permittivity of the capping layer, respectively.

The trend of the curves in Fig. 3 is in accordance with what can be found in literature [7,11]. Still, some variations from a pure linear trend are observed. The lower decrease of capacitance associated to a high-k capping layer ($\epsilon_r = 20$) is due to the increasing value of C_{pc_fr} as the recess goes on. This increase, illustrated in Fig. 4 as “region I”, slowly reaches a saturation value (region II) below a polysilicon thickness of 35 nm, due to the increasing distance between the gate top surface and the S/D contacts. Finally, for polysilicon thicknesses less than 10 nm, C_{pc_fr} increases again as the coupling of the gate top surface with faceted RSD is reinforced.

As presented in the device fabrication section, a chemical mechanical polishing (CMP) step is performed after the deposition of the pre-contacts metal. This step is mandatory to ensure that each source and drain does not form an electrical short-circuit with its neighbour. However, resorting to CMP introduces a potential uncertainty on the final thickness of the gate capping layer due to process non-uniformity. Consequences of this are studied in

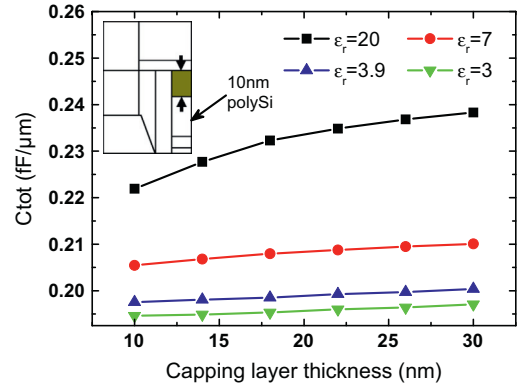


Fig. 5. Impact of the post-CMP capping layer thickness (cf. inset) on the total parasitic capacitance $C_{or} + C_{pc}$ for a 10 nm-thick polySi.

Fig. 5 considering a recessed polysilicon layer of 10 nm, and a 20 nm-thick gate capping layer with a variation of ± 10 nm.

As expected, for a given capping layer thickness, a higher permittivity results in a larger parasitic capacitance. In the case of high permittivity materials ($\epsilon_r = 20$ and $\epsilon_r = 7$), the capacitance increases with the capping layer thickness and finally reaches a saturation value. This phenomenon, similar to the one observed in Fig. 4 (region II) illustrates the fact that the fringe capacitance is mainly governed by the capacitive surface with the smaller area [7] (in this case, the gatelength L_g).

One can notice that the general impact of the capping layer thickness on C_{tot} remains relatively weak. Even when considering the worst case ($\epsilon_r = 20$), the maximum variation of C_{tot} is less than 0.02 fF/ μm .

Nevertheless, a high-k capping layer leads to a higher sensitivity to CMP non-uniformity so that low permittivity capping materials are preferred to ensure a weaker impact on C_{tot} .

Beyond the above analysis, the thinning of the capping layer must also be carefully assessed when correlated to lithography misalignment which is, by essence, an unpredictable parameter. In this case, contacts misalignment over pre-contacts can indeed have a non-negligible impact on the gate-to-S/D contact capacitance, especially when the capping layer features a high permittivity. Fig. 6 shows the evolution of this parasitic component with respect to the contact-to-gate distance x , considering HfO_2 as the capping material. As before, the polysilicon thickness is kept constant (10 nm).

If a thick capping layer (40 nm thick) remains after the pre-contact CMP process, almost no dependence is observed. Using such thick capping layer remains therefore the best way to minimize the impact of lithography misalignment on C_{tot} .

On the contrary, as the capping layer is much thinner, the gate-to-contact coupling strongly varies. In the case of a 5 nm capping layer, C_{tot} reaches a particularly high values when the contact is overhanging the gate ($x < 0$) compared to when it is not. This is due to the C_{pc_fr} coupling through the gate's top surface which increases and slowly turns from a fringe to a face-to-face parallel plate capacitance as the contact starts overlapping the gate.

For negative x values, the thinner the capping layer is, the stronger C_{tot} becomes. However this trend tends to reverse as the contact gets closer to the gate.

Apart from the optimizations previously proposed, another option to reduce C_{tot} lies in the choice of spacer materials. Spacers are the only separation between gates and S/D contacts in a self-aligned scheme. Using low-k spacers therefore appears as an interesting lever in the reduction of parasitic capacitances. This method has already been investigated on less aggressive nodes [12,13] and becomes very attractive for sub-14 nm technological nodes.

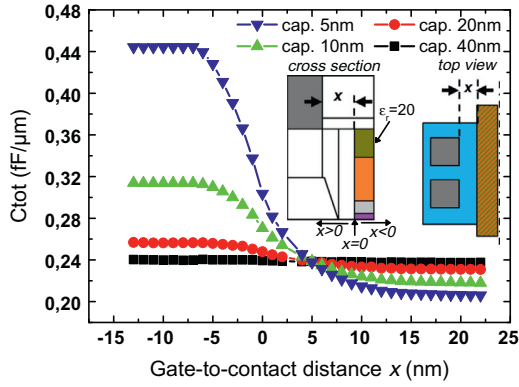


Fig. 6. Variation of the gate-to-contact capacitance as function of gate-to-contact distance considering various capping layer thicknesses ($x < 0$: the contact starts overlapping the gate; $x > 0$: the contact is moving away from the gate).

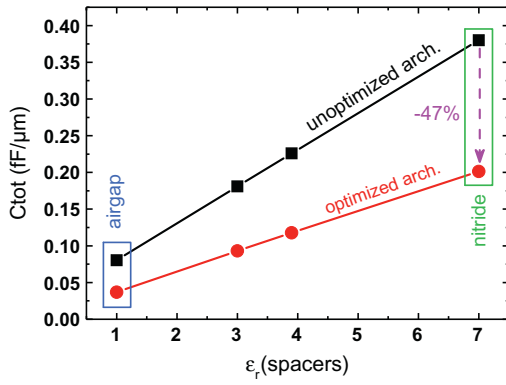


Fig. 7. Gate-to-SD-contacts capacitance dependence on spacers permittivity w/ and w/o architecture optimization.

Table 2

Detailed list of simulation parameters considered in the case of optimized and unoptimized architectures.

Parameters	Unoptimized arch.	Optimized arch.
PolySi thickness	40 nm	10 nm
Capping layer thickness	10 nm	30 nm
Cap. layer rel. permittivity	20	3.9

Fig. 7 is obtained by varying the permittivity of spacers 1 and 2, with and without applying any other optimization lever previously mentioned in this paper. Results show that when the relative permittivity of spacers is equal to 7 (standard nitride spacers), optimizing gate stack parameters (polysilicon thickness, capping layer thickness and material, see **Table 2**) effectively reduces the total parasitic capacitance by 47%. When considering airgap spacers ($\epsilon_r = 1$), further optimization of the structure still cuts C_{tot} by half. However, in terms of absolute values, the reduction of C_{tot} is attenuated as the permittivity of spacers is reduced. This is because most of parasitic coupling has already been highly attenuated by the use of low- k spacers, which appear therefore as the prominent parameter to tune C_{tot} .

Depending on the fabrication process, it can though be easier to perform an optimization of gate stack parameters instead of replacing initials spacers with new material ones.

3.3. Consequences at the circuit scale

SPICE simulations were carried out to evaluate circuit parameters such as speed and power consumption. We used a surface

potential-based model card adapted to the 10 nm FDSOI node, using data from 28 nm and 14 nm FDSOI technologies. S/D series resistance parameters were extracted by TCAD simulations and included in the model.

Delay per stage τ was evaluated by applying the method described in [14] on an 11-stages Ring Oscillator (RO) considering a fan out of 3 (FO3) in the configuration shown in **Fig. 8**. 14 nm gatelength transistors were simulated on 5 nm thick SOI film considering a nominal active area width of 140 nm and 15 nm thick buried oxide substrates. An additional capacitance C_{BE} is added at the end of each stage of the chain to emulate parasitic interconnection coupling occurring in the Back-End-Of-Line (BEOL). Oscillations of the circuit output voltage V_{out} are shown in **Fig. 9** in response to an input voltage $V_{in} = 0.8$ V.

The variation of delay with respect to the back-end capacitance C_{BE} is shown in **Fig. 10** considering various architecture configurations. This graph reveals that the absolute delay decrease when going from an unoptimized architecture to a more optimized one remains the same independently of the value of C_{BE} .

Considering now a fixed C_{BE} value of 1.5 fF/ μm based on ITRS specifications for the specific 10 nm node [10], a delay of 9.67 ps was extracted. This value corresponds to an unoptimized architecture in the case of nitride spacers. As for the excessive C_{tot} value found in Section 3.1, the extracted delay does not meet performance targets which require approximately a 25% delay decrease for each new generation. Recently, a delay of 13.6 ps was measured on FO3 ring oscillators for the 28 nm FDSOI technology [15], setting realistic targets to 10.2 ps and 7.65 ps for the 14 nm and 10 nm FDSOI technologies, respectively.

However, optimizing the structure as proposed in the previous section enables a reduction of τ down to 8.67 ps, still for $C_{BE} = 1.5$ fF/ μm . The additional use of low- k spacers such as airgaps leads to a further decrease down to 7.77 ps, finally meeting the -25% delay required at each node, as depicted in **Fig. 11**.

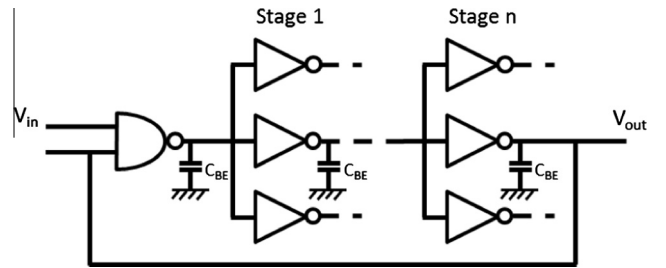


Fig. 8. Schematic of the simulated FO3 inverters chain.

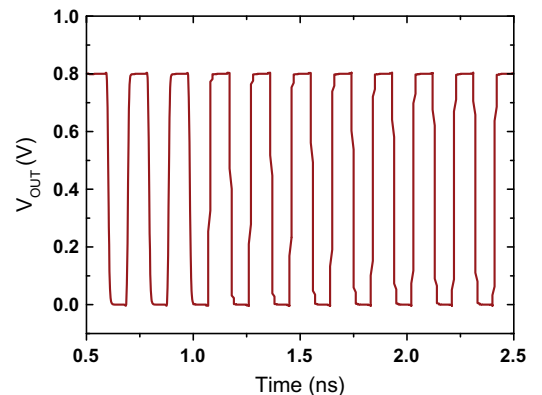


Fig. 9. Consecutive rises and falls of the ring oscillator output voltage as function of time.

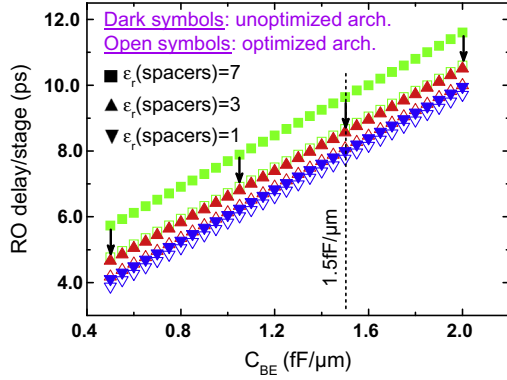


Fig. 10. RO delay per stage as function of back-end capacitance for various architecture configurations.

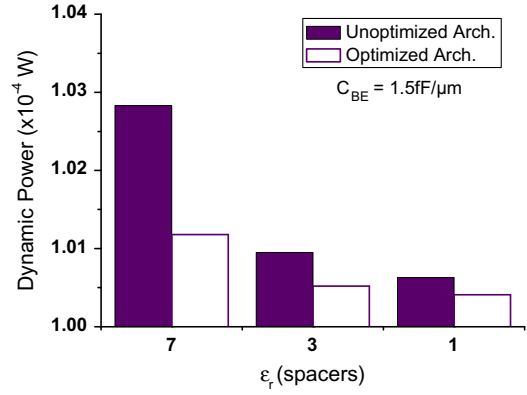


Fig. 12. Dynamic power consumption of the circuit considering different transistor architectures, with $C_{BE} = 1.5 \text{ fF}/\mu\text{m}$.

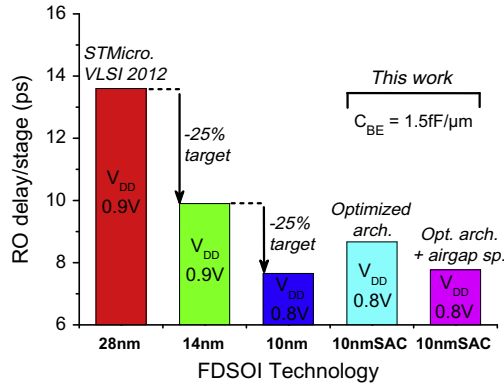


Fig. 11. RO delay predictions and benchmark for FDSOI technology nodes.

$$P_{DYN} = f \cdot \int_0^T i_D(t) \cdot V_{DD} dt \quad (3)$$

Dynamic power P_{DYN} of the above described RO was calculated by applying Eq. (3) where f is the circuit oscillation frequency. Considering a supply voltage $V_{DD} = V_{in} = 0.8 \text{ V}$, the drive current $i_D(t)$ was evaluated as function of the circuit oscillation time, as illustrated in Fig. 9. Fig. 12 summarizes the sensitivity of P_{DYN} for different structure configurations considering a fixed value of $C_{BE} = 1.5 \text{ fF}/\mu\text{m}$. The addition of airgap spacers in the case of an optimized structure results in a reduction of P_{DYN} less than 1%. Minimization of the parasitic capacitances at the transistor scale has therefore a low impact on the circuit dynamic power consumption. This is due to the simultaneous increase of the circuit frequency which counterbalances the capacitance reduction. Still, the values given in Fig. 13 remain in the same order of magnitude than what is found in the literature and are in accordance with the constant scaling trend of P_{DYN} from one node to another [16].

Finally, the implication of the active area width W and supply voltage V_{DD} on the speed/power consumption trade-off has been investigated in the case of an optimized architecture with nitride or airgap spacers. This gives insights on how to choose these parameters correctly.

For a constant dynamic power, the gain on the circuit speed remains roughly the same independently of the width of the active area. Fig. 13 shows that this improvement is always around -0.9 ps when airspacers are used instead of nitride in the case of an optimized structure, at $V_{DD} = 0.8 \text{ V}$.

However, the speed improvement enabled by airgap spacers varies as function of V_{DD} . The lower the value of V_{DD} is, the more effective is the speed gain. On Fig. 14, speed is reduced by 0.9 ps

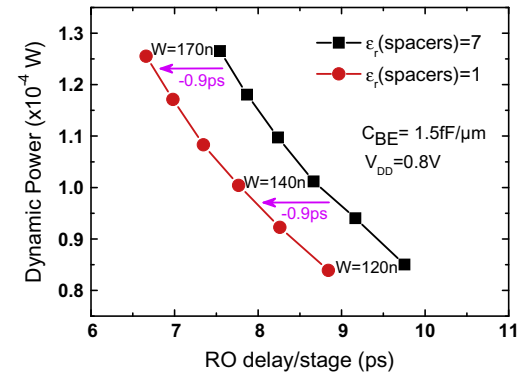


Fig. 13. Dynamic power consumption as function of RO delay on an optimized structure considering various spacer configurations and active zone widths at fixed $V_{DD} = 0.8 \text{ V}$.

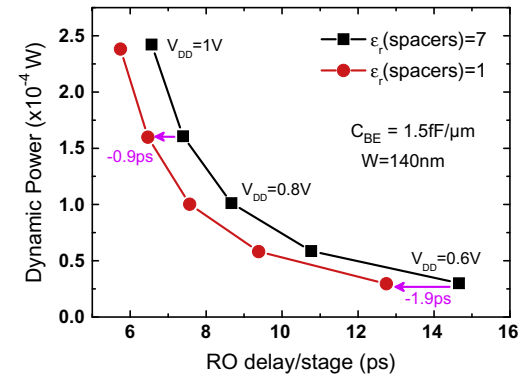


Fig. 14. Dynamic power consumption as function of RO delay on an optimized structure considering various spacer and supply voltage configurations at fixed $W = 140 \text{ nm}$.

at $V_{DD} = 0.9 \text{ V}$ while it is lowered by 1.9 ps at $V_{DD} = 0.6 \text{ V}$, considering a nominal value $W = 140 \text{ nm}$.

When dynamic power is kept constant, improving circuit speed by reducing parasitic capacitances at the transistor scale is therefore modulated by the supply voltage under consideration but remains insensitive to the width of the active zone.

4. Conclusion

An original architecture adapted to 64 nm pitch FDSOI transistors has been proposed, featuring self-aligned contacts and

insulated recessed gates. The process presented above offers advantages to counter difficulties associated to the lithography registration accuracy when structuring S/D contacts.

The optimization of such architecture was carried out by simulations in order to limit the increase of parasitic capacitances inherent to a self-aligned contacts approach.

On the one hand, when considering traditional spacers material like nitride, it was shown that recessing the gate polysilicon layer was a very effective solution, for any gate capping material. Along with this new feature, the use of a low-k gate capping layer is preferred to ensure the weakest impact on the gate-to-contact coupling and limit any sensitivity to the non-uniformity of CMP processes. Nevertheless, if the gate capping layer has a high permittivity, it should be as thick as possible to reduce sensitivity to lithographic misalignment.

On the other hand, when considering low-k spacers, these optimizations become less effective in terms of absolute values as most parasitic capacitances have already been highly reduced. Spacers permittivity therefore appears as a first order parameter in the reduction of parasitic capacitances at the transistor scale.

Consequences of such optimizations at the circuit level were also investigated. Results showed that an optimized architecture including airgap spacers was necessary to meet speed requirement predicted for the 10 nm node. Finally, at a constant dynamic power, resorting to lower values of V_{DD} improves the effectiveness of the proposed architecture optimizations to further increase circuit performance.

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