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Phase Noise Metrology and Modelling of Microwave Transistors Applications to the design of state of the art Dielectric Resonator Oscillators

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Invited Paper

ABSTRACT

Phase noise in microwave transistors is studied both theoretically and experimentally using residual phase noise measurements. The experimental approach allows the exploration of many interesting features of phase noise generation in these devices, such as the dependence of phase noise versus microwave power or transistor low frequency loading, meanwhile nonlinear simulation is still necessary to optimise the microwave load and the whole oscillator circuit. The different behaviours described are illustrated in various microwave circuits, and particularly dielectric resonator oscillators, with some of them featuring state of the art performance.

Keywords: Microwave oscillator, Phase noise, Noise modelling, Nonlinear modelling, DRO, sapphire oscillator

1. INTRODUCTION

Phase noise of microwave free running sources has always been an important problem in various applications. This noise generates an increased bit error rate in a telecommunication link, it degrades the sensitivity of a radar (particularly in the case of Doppler or FM-CW radar), it prevents the direct use of a microwave oscillator together with an atomic frequency reference. If the long term and medium term frequency stability of a microwave synthesiser are related to the performance of its quartz crystal reference, the short term stability depends on the performance of the microwave head of the system (mainly the VCO). Above approximately 1 kHz offset (typical value in a high Q source such as a phase locked DRO or a YIG based synthesiser), the source phase noise features a flat region which corresponds to the transition region between the free running VCO noise and the multiplied reference noise. In this region, and of course at higher offset frequencies (outside the PLL loop bandwidth), the phase noise is dominated by the contribution of the microwave oscillator noise, and sometimes also by the contribution of the other loop circuits such as the frequency dividers.

Reducing this noise contribution is a difficult challenge for microwave engineers and circuits designers. It cannot be done without a good knowledge of the noise mechanisms involved in the circuit. The main contributor to this noise is the microwave transistor. Both the transistor low frequency (LF) and high frequency (HF) noises can contribute to phase noise generation. The device low frequency noise (or excess noise) is converted close to the microwave carrier by the nonlinear elements. The transistor high frequency noise is added to the carrier and generates a noise floor which may be predominant at high offset frequencies, particularly if the oscillator output power is not high enough. In many cases however, the LF noise contribution is the main one and therefore a transistor with a low excess noise must be chosen in oscillators applications. But this is only the first step for phase noise reduction. Everything should be done to prevent the transposition of this noise near the oscillator carrier. To this purpose, different approaches may be chosen, either based on the experiment or on the nonlinear simulation.

In this paper, the phase noise properties of microwave transistors are investigated by both techniques. Firstly, a phase noise measurement bench, able to characterise the residual phase noise of transistor in open loop (or amplifier) configuration is presented. The phase noise of various devices measured in this way is discussed, together with the effect of the low frequency (LF) loading circuitry (bias network) in the case of bipolar devices.

The transistor RF loading is also of major importance. The phase noise is generated through the fluctuation (or more exactly, the modulation) of the device nonlinear elements i.e. the nonlinear capacitances and resistances. The LF

load optimisation is based on the study of how the transistor LF noise affects these elements and makes them fluctuate. The RF load optimisation is based on how to prevent a strong impact on phase noise from these fluctuating elements. This requires a reliable noise model of the device and a nonlinear CAD approach. Such a model, which may be call a "nonlinear noise model" because it is the association of a nonlinear model with noise sources intrinsically embedded in it, is particularly difficult to extract.

Circuit examples are then shown. Some of these circuits, realized with low 1/f noise SiGe HBT devices and optimised versus both RF and HF loading, feature state of the art phase noise performance. These circuits use either classical ceramic resonators (Dielectric Resonator Oscillators or DRO) or single crystal sapphire resonators (ultra high spectral purity DRO).

2. RESIDUAL PHASE NOISE MEASUREMENT OF MICROWAVE TRANSISTORS

In an oscillator loop, the frequency fluctuations come from the phase fluctuations of the amplifier [1], simply because the phase is constant on a loop turn and this makes fluctuate the frequency in order to compensate for the amplifier phase fluctuations. A perturbation analysis leads to the following formula, which relates the oscillator frequency fluctuations spectral density $S_{\Delta f}$ (in Hz²/Hz), the amplifier phase noise spectral density S_{ϕ} (in rad²/Hz), the oscillator frequency f_0 and the resonator loaded Q factor :

$$\mathbf{S}_{\Delta f} = \left[\frac{\mathbf{f}_0}{2\mathbf{Q}_{\mathrm{L}}}\right]^2 \mathbf{S}_{\Phi} \tag{1}$$

It is therefore equivalent to study the oscillator frequency noise $S_{\Delta f}$ or the amplifier phase noise S_{ϕ} . The interest of investigations in an amplifier configuration (or open loop configuration) rely on the fact that it is a simpler configuration than an oscillator, both for measurement and modelling : 1) there is no loop condition on phase, so the measurement can be performed in well defined conditions, easily reproducible using the simulation tools ; 2) the measurement can be performed down to the linear regime ; 3) it is easier and faster to simulate the performance of a driven circuit (open loop) than an autonomous circuit (closed loop) ; 4) It is essential to investigate the fundamental noise conversion processes within the device, independently of the surrounding circuit.

The conversion of the transistor phase fluctuations into oscillator frequency fluctuations is illustrated in Figure 1. The phase noise of a MESFET oscillator, realized with a parallel feedback loop on a transmission type dielectric resonator (loaded Q of 1500), is compared to the open loop phase noise of the transistor. The two curves intersect point is close to the resonator half bandwidth $f_o/2Q_L$, as described in [1]. The transistor phase noise features approximately a 10 dB/dec slope, which is characteristic of a 1/f fluctuation. The oscillator phase noise, inside the resonator bandwidth, features a 30 dB/dec slope which corresponds to the transistor 1/f phase fluctuations transformed into 1/f frequency fluctuations by the loop effect.

The open loop phase noise approach (or residual phase noise approach) has revealed many interesting behaviours and enlighten some complex noise mechanisms in III-V devices [2 to 5]. In [2], the RF load effect on the phase noise of some FET amplifiers is studied in this experimental configuration. In [3], residual phase noise data are used to locate the main noise source responsible for phase noise generation (on the gate, in this case). These results have lead to a FET noise model [4] which will be further described in this paper.

With silicon BJT and SiGe HBT devices, the same approach is more difficult to implement. These devices may feature a very low phase noise level, sometimes lower than the phase noise of the silicon schottky diode mixers used as phase detectors in this experiment. In order to characterise the phase noise of these devices, some special techniques must be implemented for phase detection. In our experiments, we use a cross correlation technique [6], which is based on a cross spectrum measurement on two identical mixers (see Figure 2 for the measurement bench). It allows a substantial improvement of the experiment noise floor by eliminating the uncorrelated noises of the two mixers, at the cost of acquisition time and averaging : the noise floor improves of about $10 \log \sqrt{N}$ (in dB), N being the averaging number. We currently use N = 200 for regular investigations (improvement of 11.5 dB) and occasionally N = 1000, for the characterisation of very low phase noise devices (improvement of 15 dB).

But the phase detector noise is not the only problem in this experiment. The microwave source noise can also be a real problem.



 $\label{eq:Figure 1} \textbf{Figure 1}: Measured phase noise of a MESFET amplifier and a MESFET oscillator realized with the same transistor (f_o = 4 \text{ GHz})$



Figure 2 : Residual phase noise measurement bench using a cross correlation technique (1-18 GHz)

Its phase noise can be theoretically eliminated using a good balance between the two phase detectors arms (no electrical delay). But the rejection of its amplitude noise (or AM noise) is more difficult. There are two ways in which this noise can be detected : by an unperfectly balanced mixer or directly by the device under test in nonlinear regime. We have proposed some solutions to these two problems [7], the second one being the more difficult since it is necessary to reduce the source AM noise itself, which is possible using a low phase noise limiter device [7].

Very low phase noise floors can then be reached (ex : -180 dBc/Hz at 10 kHz offset from a 3.5 GHz carrier), and very low noise devices can be characterised. Figure 3 represents the measurement of the SSB residual phase noise at 3.5 GHz of various transistors : one GaAs field effect device (more precisely, a PHEMT) and three different SiGe HBT devices. All these transistors are loaded onto 50 Ω and submitted to a microwave input power of about 0 dBm. All the silicon transistors feature a very good phase noise performance. Some differences between these devices have been found, but they are restricted to the 1/f part of the spectrum. The phase noise of the HEMT transistor is much higher. However, this device has not been particularly selected for its phase noise performance. The performance of a medium power MESFET device would have been much better, but still about 10 dB noisier than a silicon device at 10 kHz offset. However, the phase noise onto 50 Ω has to be considered together with the gain performance. It is indeed essential that the amplifier used in the oscillator should be able to compensate for the losses of a moderately coupled resonator. Regarding this last parameter, the devices classification is exactly the opposite of their classification versus phase noise performance. There is a trade-off to find between phase noise and gain performance [2,8].

From these open loop phase noise measurements data, the phase noise performance of an oscillator realized with one of these transistors can be calculated with the following formula :

$$L(f)_{\text{(in dBc/Hz)}} = 10 \log \left[S_{\varphi}\right]_{\text{(in dBrad/Hz)}} + 20 \log \left[\frac{f_0}{2\sqrt{2} Q_{\text{L}} f}\right]$$
(2)

L(f) being the oscillator SSB phase noise, f the offset frequency, f_0 the oscillation frequency and Q_L the resonator loaded Q factor. As an example, this leads to approximately -142 dBc/Hz at 10 kHz offset from a 3.5 GHz carrier, for a loaded Q of 5000 using the data of Figure 2 for the two best SiGe devices. However, such a performance could have not been reached without a careful selection of the devices bias network. Details on this network are given in the next section.

3. INFLUENCE OF THE BIAS NETWORK ON BIPOLAR TRANSISTOR PHASE NOISE

In the experiment described in section I, the DUT biasing network is of prime importance. This is not because of the outside noise coming from the power supply or any other interaction with the electrical network. All this is very well controlled through the use of battery based power supplies and Faraday's shielding. The real goal of the biasing network is to minimise the impact of the transistor LF noise on the device nonlinearities control voltages.

This approach is not very efficient in FET oscillators. As we will see further in this paper, the main nonlinear element in a FET is the gate-source nonlinearity (and particularly its capacitance). But the control of the gate-source LF load is difficult, because of the very high impedance on this transistor access at LF. On the contrary, the bipolar transistor features at LF an input impedance of a few tens or hundred ohms, and it is very easy to experiment the influence of the LF loading on phase noise for these devices.

There are two main control voltage in a bipolar transistor : Vbe and Vce. Any LF fluctuation in one of these voltages will result in an RF modulation, either of phase or amplitude or, generally, both. More particularly, the input base-emitter junction is very efficient to convert a LF voltage fluctuation into a phase fluctuation [9]. A current excess noise source is associated to this diode, which is often the only excess noise source considered in a simple bipolar transistor LF noise model (ex : SPICE models). It is easy to cancel the effect of such a noise source using a low impedance load at baseband frequencies, where the noise must be reduced. This can be done, as an example, with a high value capacitance [9] in parallel on the base-emitter bias network as shown in Figure 5.

The result is an important phase noise improvement, which is of course dependent on the device's noise characteristics (between 5 dB and 20 dB, typically). An example is shown in Figure 5 for an Infineon BFP620 device. Of course, this technique is also valid for other noise sources, and some improvement can sometimes be obtained on the phase noise by optimising the collector bias network.

If an high performance is required closer to the carrier, or if the size of the filtering capacitor is prohibitive for the application, a low impedance bias network can also be used [16,17] (Figure 4). However, this approach changes the transistor nonlinear steady state, and the whole circuit must be simulated again. Moreover, it is not always easy to control directly the bipolar transistor voltage V_{be} instead of its current i_b .

With the high value capacitance approach, the only problem may be in the circuit stability (which is modified by any change on the bias network). This can be a difficult problem to solve since the theoretical study of oscillation start up and stability is not easy with today commercially available CAD software, particularly if the time constants involved in the circuit are very large compared to the oscillation frequency.

4. INFLUENCE OF THE RF LOADING ON AMPLIFIERS PHASE NOISE

The phase noise is inversely proportional to the resonator loaded Q factor. This assumption is found on any theory on phase noise, including the simplest ones [1], and this means that it should be true. Actually, it is true, but only if the other circuit parameters are hold constant while increasing or decreasing the Q factor. This is not what is done in practice : usually, an engineer will choose a resonator coupling factor on the basis of the gain he is able to obtain with the active device. So many circuits make use of a transistor matched for the highest small signal gain at a given frequency, associated with a resonator featuring approximately 2 dB less losses than the available small signal gain.

This approach leads to very poor phase noise results, both for FET [2] or bipolar transistors oscillators [8]. Firstly, it is easy to demonstrate that, above 6 dB decoupling for the resonator, the improvement on the loaded Q (and consequently on phase noise) is very weak. So 8 dB gain is largely sufficient for the active device, and very good results can be obtained with an amplifier featuring only 6 dB gain. But this only explains why the phase noise does not improve too much at very high decoupling levels. The other reason of the phase noise degradation is in the conversion factor between the LF noise and the phase noise.

If we consider that the amplifier phase fluctuations comes from the conversion of a unique LF noise source of spectral density S_{v} , we can rewrite the equation (1) as follows :

$$\mathbf{S}_{\Delta f} = \left[\frac{\mathbf{f}_0}{2\mathbf{Q}_L}\right]^2 \mathbf{k}_{\Phi}^2 \mathbf{S}_{v} \tag{3}$$

with k_{ϕ} being the conversion factor of the voltage fluctuations into phase fluctuations.

From the eq. (3), we clearly see that any improvement of Q_L will reduce the oscillator frequency fluctuations only if k_{ϕ} is constant. But improving the small signal gain by an appropriate matching network creates a resonant behaviour which enhances the phase fluctuations. Therefore, the higher gain does not coincide at all, unfortunately, with the smaller k_{ϕ} . The simulation of these two parameters, small signal gain and k_{ϕ} , are plotted in Figure 6 versus the RF input impedance of a MESFET and a SiGe bipolar transistor. The coefficient k_{ϕ} corresponds to the conversion coefficient of the LF gate-source (base-emitter) voltage fluctuations into phase fluctuations through the FET (SiGe HBT). It is plotted multiplied by a constant value of the low frequency noise S_v in order to visualise a phase noise level instead of a conversion factor.

It is clear on this plot that the phase noise variations versus the transistor input load are very large. For some values of this input load, the phase noise dramatically drops down non physical values. This is only due to the simple LF noise model used in this simulation, which involves only one noise source (fluctuations of the LF base-emitter voltage). However, if this noise source is predominant, the real phase noise data should follow this curve until it reaches a given level where another source becomes predominant. Unfortunately, these data have not yet been verified experimentally on the whole Smith chart, but only on a very small number of configurations. However, these results already demonstrate the importance of the nonlinear simulation for oscillators phase noise optimisation. Therefore, the problem is : how reliable can be a CAD approach for phase noise computing ? Which are the main CAD techniques available and which transistor model must be used to efficiently compute the transistor or oscillator phase noise ?



Figure 3 : Residual phase noise at 3.5 GHz of four different transistors, three SiGe HBT devices and one PHEMT device. The transistors are maintained on 50 Ω load at RF and the microwave input power is 0 dBm. A capacitive noise filtering network (20 μ F) is used to bias the SiGe HBT devices, such as the one depicted in Figure 4.



Figure 4 : Bias network with a noise filtering capacitor. The control of the DC base current is maintained thanks to a high value resistance R_{bias} (about 10 k Ω) and the phase noise can be optimised above 100 Hz offset by varying R_{noise} (in many cases, the optimum is found for R_{noise} equal to zero).



Figure 5: Influence of the bias network on the residual phase noise of an SiGe HBT device at 3.5 GHz



Figure 6 : Evidence of a trade-off between phase noise and gain performance versus the RF input load Simulated data for two different devices : a MESFET (upper plot) [2] and an SiGe HBT (lower plot)

5. CAD AND PHASE NOISE

The simulated phase noise results already presented in paragraph III have been calculated using an harmonic balance software and an equivalent circuit model for the transistors (a foundry model for the MESFET device and a laboratory extracted nonlinear model of the HBT device [12]). The simulation technique used for phase noise computing is a sensitivity technique, which consists to induce a small quasi-static perturbation on the oscillator (the amplifier) steady state, and to examine the consequence on the oscillator frequency (the amplifier phase). This technique has the advantage of being simple and faster than the other techniques, and particularly in case of an open loop phase noise computing where the system frequency is known. It is well suited for phase noise computing on the whole Smith chart, which would require an important computing time with other techniques.

This quasi-static technique is also known as a *modulation* technique [10]. The "modulation" name comes from the fact that it is a real perturbation of the circuit nonlinear steady state. Another technique is the *conversion* approach [10], based on the superposition of noise sidebands on an unperturbed nonlinear steady state and on a calculation using the conversion matrices (N dimensional derivatives of the nonlinear steady state). Finally, some CAD software also propose time domain techniques and a technique which mixes time domain and frequency domain (*envelope* technique) [11].

All of these simulation techniques have their advantages and drawbacks. The *modulation* technique is insensitive to any low frequency dispersion. It is thus unable to predict a behaviour such the one described in section II, involving high value capacitances. However, the LF noise equations can be treated separately from the conversion and a two step procedure can solve this problem. The use of a *conversion* technique may result in difficulties in predicting the phase noise very close to the oscillator carrier, because of a natural divergence of the system equations (only in the oscillator case). A solution to solve this problem is to increase the computing precision (and particularly the oversampling parameter in the harmonic balance software). Otherwise, this technique is able to calculate the different parts of the oscillator spectrum, including the phase modulation domain ($f > f_0/2Q_L$). Concerning the *envelope* technique, it seems very efficient but it is not generally designed to plot a phase noise spectrum in commercial software (rather dedicated to deterministic modulation).

Therefore, many different tools are available to calculate the phase noise of an amplifier or an oscillator. If these tools are used with a good knowledge of their limitations, the phase noise should be calculated precisely. The main problem in phase noise calculation is not in the computing approach but rather in the noise modelling of the active device.

In linear noise modelling, it is not essential to physically locate a noise source in the transistor model. An equivalent noise sources approach is generally used, with two extrinsic noise sources and their correlation factor. On the contrary, in a nonlinear circuit, the location of a noise source versus a nonlinear element is essential. If this noise source modulates a nonlinear element, it will be transposed to higher frequencies and generate phase noise. If it is at the transistor output, it cannot modulate the main nonlinear elements in the device, and has a very weak effect on phase noise. Moreover, the microwave power changes the values of the transistor low frequency equivalent circuit. As an example, if the microwave carrier is increased, a gain compression is observed at low frequency. This also creates strong changes in the observed phase noise spectrum.

The amplifier phase noise is therefore the result of many different fluctuations in the device, and can be expressed by an equation of this type :

$$S_{\varphi} = \sum_{i} k_{i}^{2} (V_{1}, V_{2}) S_{i}$$
 (4)

where S_{ϕ} is the amplifier phase noise spectral density, S_i the spectral density of the ith noise source and k_i the corresponding conversion coefficient of this noise source into phase fluctuations, which may depends on the transistor intrinsic control voltages (V1,V2) and thus be nonlinear (rem: this equation supposes that the intrinsic noise sources are not correlated).

The goal is therefore to compute precisely the various nonlinear conversion coefficients. Indeed, an accurate computing of these coefficients should be able to describe all the complex behaviours discussed above such as the dependence of the phase noise versus the microwave power.

However this is not an easy task. As an example, the noise source which is predominant in the phase noise spectrum may be negligible in the transistor LF noise spectrum. An accurate modelling must involve both LF noise measurements and residual phase noise measurements at different microwave power levels.

We have presented such a complex model for a FET oscillator [4]. In this model, it has been necessary to take into account the nonlinearity of the transistor channel resistance in order to simulate the behaviour observed on the residual phase noise spectrum versus the microwave input power. This behaviour is shown in Figure 7. It is clear that a generation-recombination (g-r) noise source becomes more and more predominant while increasing the microwave power, and this was impossible to predict only taking into account the LF noise measurement (the LF noise spectrum on the quiescent transistor features a completely different shape from the phase noise spectrum at high microwave power). In our model, depicted in Figure 8, the g-r noise source is added as a current noise source in parallel to this nonlinear channel resistance Ri.

The same difficulties may be encountered while modelling bipolar devices. However, in case of silicon bipolar devices (or SiGe devices), the observed behaviours are simpler. The noise is generally the combination of a pure 1/f noise and a white noise floor, and only the conversion of the 1/f component is difficult to compute if the main 1/f noise source cannot be precisely located in the device. Therefore, accurate phase noise simulations are easier to obtain [12].

6. INFLUENCE OF HF NOISE ON TRANSISTOR PHASE NOISE

Up to 100 kHz offset, and probably much higher than this frequency, no white noise region is observed on the residual phase noise data measured on III-V field effect devices. Equivalently, the spectra measured on oscillators realized with these transistors feature high level slopes of 30 dB/dec (in case of a predominant 1/f noise) or a mixing of 1/f and generation-recombination noise. In these circuits, the phase noise is entirely a conversion process and is translated from low frequency by the device nonlinearities, as previously described.

In silicon bipolar devices (or SiGe devices), a white noise floor is reached on the residual phase noise plot at a frequency f_c which is in the range of [1 kHz – 100 kHz], depending on the transistor (see by example, Figure 3). Such a noise floor may result from the conversion of the LF white noise floor, or may be due to the directly superimposed HF noise. The main difference between these two noise contributions is in the multiplicative nature of the first mechanism (conversion) and on the additive nature of the second one (HF phase noise). In a residual phase noise experiment, it is easy to control the carrier level and to check this behaviour. If the phase noise floor is inversely proportional to the carrier power, it is probably an additive noise.

Such an experiment has recently been carried on, with different silicon bipolar devices. The predominant influence of the HF phase noise has been demonstrated in most cases, for offset frequencies higher than 10 kHz [13]. Therefore, a transistor noise model for phase noise calculation should be reliable not only versus the LF noise sources location but also versus the HF noise sources location !

7. OSCILLATORS EXAMPLES: SIGE HBT DRO

The oscillators examples discussed here are only based on SiGe HBT devices. The reason is that these devices are today the best suited to design very low phase noise oscillators in the low microwave range (approximately from 1 GHz to 10 GHz or 20 GHz) in which most of our investigations have been performed. Moreover, the design of oscillators in hybrid technology allows the choice of the active device, the use of bias filtering networks (as described in section 3) and finally a good control of the amplifier and resonator parameters (as an example, it is possible to evaluate the Q factor of the circuit), contrarily to oscillators designed with an MMIC technology, and only hybrid DRO circuits are considered in this paper. The resonator coupling has already been discussed in the preceding sections, together with the necessary amplifier gain. However, there are many topologies that can be used to meet these requirements. The better known ones are the *series feedback* and the *parallel feedback*.

The advantage of the *series feedback* is that the resonator is coupled to a single microstrip line. The amplifier is in this case a negative resistance, which is realised either in an MMIC technology or using a non-zero line length between the transistor emitter electrode and the ground in an hybrid technology.



Figure 7: Measured residual phase noise of a PHEMT device versus different input microwave power levels at 3.5 GHz from the linear regime up to about 4 dB gain compression (-8 dBm < Pin < + 4 dBm); from ref. [4].



Figure 8: Proposed model for the PHEMT device. Two LF noise sources are included in this model, and located close to the transistor gate electrode. Moreover, the channel resistance Ri is nonlinear; from ref. [4].



Figure 9 : Phase noise of a 10.2 GHz SiGe HBT DRO with a resonator loaded quality factor of $Q_L = 2500$. The phase noise is measured by two different techniques, and compared to the simulated data [14].



Figure 10 : Phase noise of the beat signal between two 4.85 GHz SiGe HBT – sapphire resonator oscillators. As the noise of the two sources is added incoherently, the phase noise of one oscillator is 3 dB lower than this curve. From ref. [18]

The *parallel feedback* is very interesting when a physical separation of the amplifier circuit and the resonator is required (very high Q cavity resonators). Also, the optimising parameters are different in both circuits types and this topology probably offers more possibilities for the circuit optimisation (but this is not clear in oscillator literature). We have obtained very good results with both circuit topologies, as further shown, and we think that there is no fundamental difference between the two. A systematic optimisation with a nonlinear software should lead in both cases to a good phase noise.

The spectrum shown in Figure 9 corresponds to a 10.2 GHz series feedback oscillator realised in hybrid technology on alumina substrate, using a Murata resonator and an SiGe HBT transistor [12,14]. This oscillator uses a 20 μ F noise filtering capacitor on the base. The resonator loaded Q factor is 2500. The oscillator phase noise is measured using two different techniques [14] : delay line discriminator and injection locking on an Anritsu synthesiser. It is also simulated [12] using a sensitivity technique (see section III) and the agreement between theory and experiment is excellent. It has not been optimised, however, versus the RF load and although this result is a state of the art result (the only similar performance has been obtained with the same active devices by a Daimler Chrysler Research team [15]), we suspect that it could be improved.

8. SIGE HBT FOR ULTRA HIGH SPECTRAL PURITY MICROWAVE SOURCES

The best dielectric resonator today uses an high order mode (whispering gallery mode, WGM) of a single crystal sapphire cylinder. The unloaded Q factor of such a resonator is about $2 \ 10^5$ at ambient temperature (for a resonant frequency between 5 GHz and 10 GHz), and a few millions or tens of millions at low temperature. The association of a low phase noise transistor with a sapphire WGM resonator leads to a very high spectral purity oscillator which may be used in phase noise and frequency metrology applications.

We have designed various oscillators of this type in the frame of the PHARAO project, in which a very high spectral purity microwave source is required in order to interrogate an exceptionally stable cesium clock. The first sapphire - SiGe HBT oscillator realized [16] has been designed using a transistor selected through residual phase noise measurements and an optimized bias network. However, no real optimization of the transistor RF load had been performed. Then, a complete nonlinear model of the transistor has been extracted and another source has been designed using a CAD approach [17,18]. The performance obtained has been very impressive : -138 dBc/Hz at 1 kHz offset from a 4.85 GHz signal at ambient temperature, and this performance agreed very well with the simulated one.

Such a microwave source is very difficult to characterize. A classical technique in this case is to realize two identical oscillators and to compare the two oscillators one to another. Generally, the two sources will oscillate at close but different frequencies and a direct comparison is in this case impossible. A solution is then to study the beat frequency between the two sources and to compare it to an high spectral purity synthesizer. In our case, the two sources were at 4.866 GHz and 4.849 GHz, and the beat frequency at 17 MHz. The RF synthesizer is the main limiting factor in this experiment, as shown in Figure 10. However, a pretty good noise floor can be reached and the sapphire – SiGe HBT oscillator is correctly characterized between 10 Hz and 3 kHz offset frequencies.

This performance corresponds to the best single loop microwave oscillator ever published at ambient temperature. The only better source is the interferometric oscillator from the University of Western Australia [19], but this oscillator make use of a complex noise cancellation circuit, which requires a fairly high volume and which is difficult to tune.

CONCLUSION

The microwave oscillator is a complex system in which the mechanisms responsible for phase noise generation are not always easy to understand. It is shown in this paper that the open loop phase noise characterization and modelling approach can be very helpful to this purpose. Various circuit parameters which determine the phase noise performance are discussed, the most difficult to optimize being the transistor RF load for which a complete non-linear model with the noise sources embedded in it (and physically located) is required.

This approach is used on different oscillators, and particularly on oscillators based on SiGe transistors which are today the best choice for low phase noise operation at microwaves (below the millimetre wave range). The performances obtained with these devices on resonator stabilised oscillators are very impressive, and can compete with the best microwave sources realised with any other technology (quartz synthesised sources included).

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