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Design and Manufacturing of a Double-Side Cooled, SiC based, High Temperature Inverter Leg

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ABSTRACT

In this paper, we present a small (25x25x3 mm^3) power module that integrates two silicon-carbide (SiC) JFETs to form an inverter leg. This module has a "sandwich" structure, i.e. the power devices are placed between two ceramic substrates, allowing for heat extraction from both sides of the dies. All interconnects are made by silver sintering, which offers a very high temperature capability (the melting point of pure silver being 961 °C). The risk of silver migration is assessed, and we show that Parylene-HT, a dielectric material that can sustain more than 300 °C, can completely coat the module, providing adequate protection.

Keywords

3-D packaging, sandwich module, JFET, silver sintering, silver migration

1 Introduction

Silicon Carbide (SiC)-based power devices can in theory operate at very high temperatures (in some cases more than 1000°C, [1]). In reality, many elements (passivation, metal contacts, oxide reliability...) set the maximum temperature of a SiC die to a much lower value, usually 200–400 °C, depending on device. Among the existing SiC power devices, the vertical Junction Field Effect Transistor (JFET) is suited to "high temperature" (300 °C or more) operation [2].

However, although this device was found to withstand continuous operation at 300 °C, that does not mean that it can operate with limited cooling: as was shown in [3], SiC JFETs must be provided with sufficient cooling (2-4 K/W or less) to prevent thermal runaway. There is, therefore, a need for a high temperature package with low thermal resistance.

Double-side cooling, a technique in which heat is removed from both sides of a die, is attractive. It is often implemented in the form of a "sandwich" structure (the die is clamped between two ceramic substrates) [4]. This has the additional advantage of resulting in lower inductance than with classical (wirebonded) power modules [5].

Among the many high temperature bonding solutions [6] that could be used for the assembly of a sandwich structure, silver sintering is particularly attractive: "low temperature" process (less than 300°C), lead-free, high thermal conductivity (more than 100 W/m.K). It has, however, one major issue: the risk of silver migration [7]. When operating at more than 100 °C, in presence of oxygen and with an electric field, silver atoms tend to migrate and to form conductive filaments across electric potentials, eventually resulting in short circuits.

In addition to this silver migration risk, many other issues had to be addressed to produce a high-temperature capable, silver sintered sandwich power module.

- The SiC JFETs have relatively fine patterns, so an accurate etching process was developed to produce the ceramic tiles, and care was taken regarding the alignment of the parts during the assembly.
- The top metallization of the dies (aluminium) is not compatible with silver sintering, requiring a dedicated preparation process.
- The thin layer of silver cannot provide much compensation for any difference in height when several devices are to be assembled in the same sandwich, so the thickness must be well controlled.

The solutions developed to tackle these issues are presented in this article. In the first section, we present the

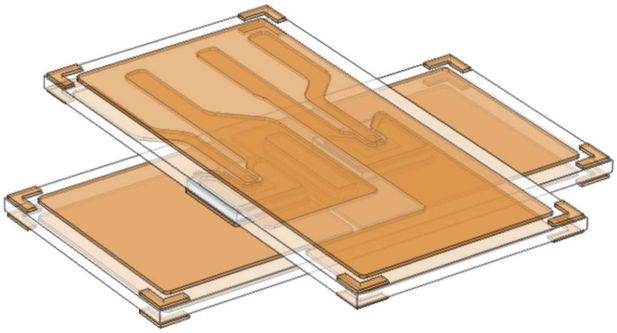

Figure 1: 3-D view of the "sandwich" structure, with two SiC JFET in half-bridge configuration. The ceramic tiles measure 12.7×25.4 mm^2 each.

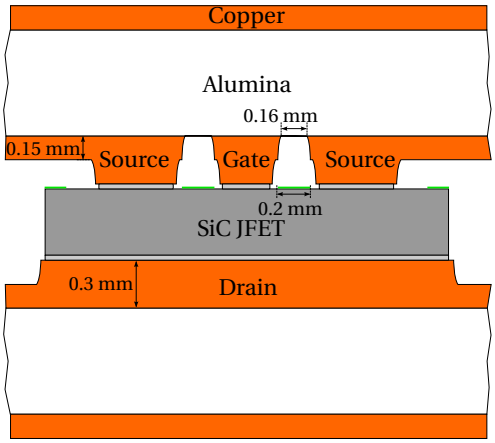

Figure 2: Up-to-scale cross section of the sandwich module around the SiC die (here a 2.4×2.4 mm^2 die) showing the relative thicknesses and spacing between the copper tracks. The alumina thickness is 0.635 mm, and that of the sintered-silver layer ≈ 0,025 mm.

sandwich structure. In the second section, the silver migration risk is assessed, and a solution is proposed to mitigate said risk. Finally, we present the manufacturing steps we used to produce working sandwich modules.

2 The "sandwich" structure

A 3D concept view of the sanwich module described in this paper is visible in figure 1. This module contains two SiC JFETs (SiCED, 1200 V), to form a half-bridge structure. The body diode of the JFETs is used so no external diodes are needed. Modules were made with two die sizes (2,4×2,4 mm^2 and 4×4 mm^2 dies), requiring a dedicated set of DBC (ceramic) tiles for each die size, as they have different patterns.

A dual-step etching process comparable to that used in [8] is needed to produce the DBC tiles. This is depicted in figure 2: the inner copper layers have some protrusions

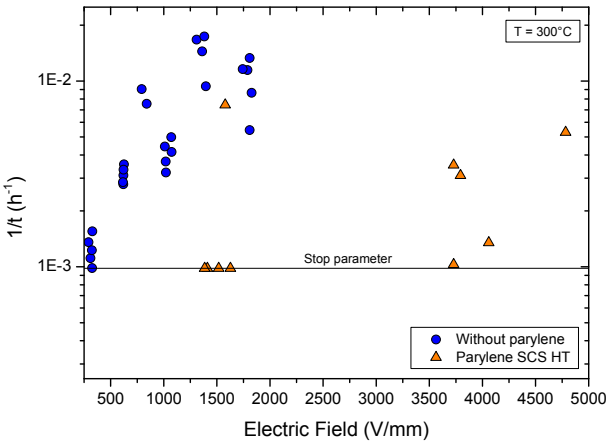

Figure 4: Time before a short circuit appears between the electrodes of a test sample as a result of silver migration, for an ambient temperature of 300 °C, depending on the electric field applied, and for two sets of samples: unprotected (blue dots), and coated with a 20 μm layer of parylene HT (yellow triangles).

where a contact is required with the die, and are thinner elsewhere. This keeps the copper conductors away from the edge protections of the die, which is required to maintain its blocking voltage capability.

Alumina-based DBC substrates were selected for this module based on cost considerations. Silicon Nitride, however, might prove to be a better option from a reliablity point of view. No specific finish was applied on the copper layers, as silver sintering was found to work (albeit not optimally) on bare copper [9]. Here again, a better option might be a gold or silver-based finish (the exact composition will depend on the sintering paste).

3 Silver Migration

The silver migration phenomenon is described in [7]. Basically, it is related to the silver oxide becoming unstable at high temperature. To assess the extend of the issue, we manufactured special test samples, consisting of two silver electrodes stencil-printed on an alumina substrate. A photograph of some test samples is given in figures 3a and 3d, for an inter-electrodes gap of 1 mm (various gap values were investigated, from 0.5 to 2 mm, see [10]).

The test samples were placed in a forced-convection oven, with a voltage bias (up to 1100 V, using a Keithley Source and Measure Unit – SMU – 2410). Up to 10 samples were tested simultaneously, using a high-voltage switch system (Keithley 7001 with 7154 switch card). Periodically (every 15 mn), the leakage current of each test sample was measured. When this current exceeded a given value (100 μA), the corresponding test sample was disconnected and the test resumed with the remain-

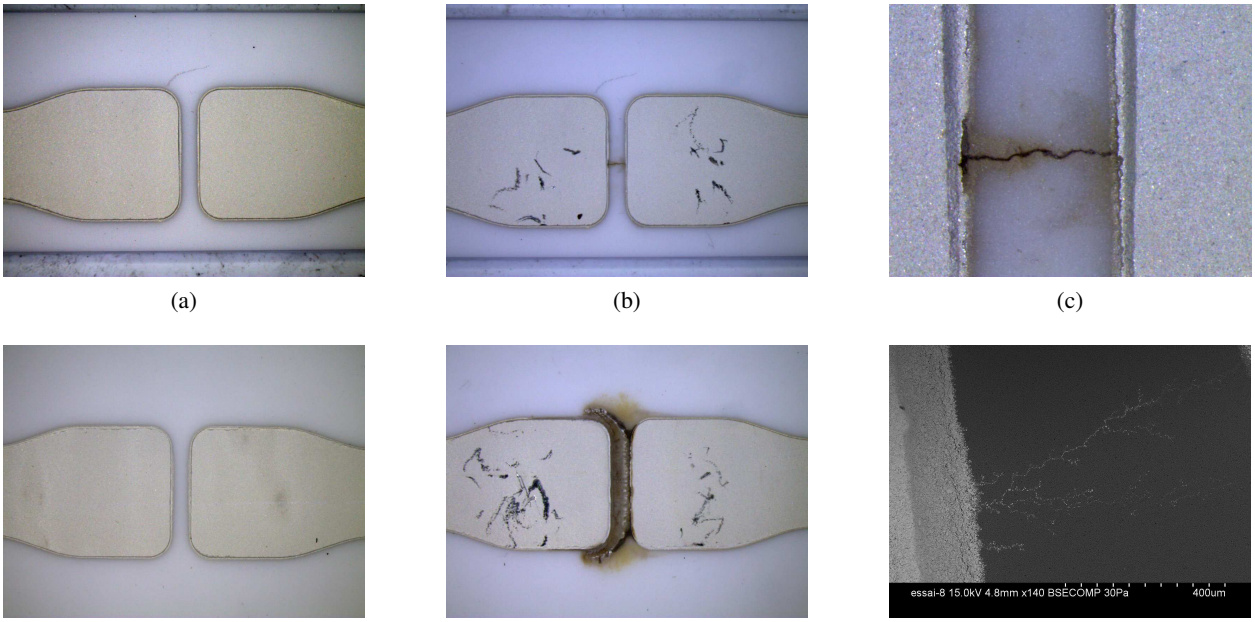

Figure 3: Pictures of some of the test samples, before the test (a) and (d), and after (b) and (e) respectively. An enlargement of (b) can be seen in (c), while an electron microscope view from another sample is visible in (f). It can be seen that the pattern and coverage of the silver deposit vary widely. All samples presented here have a 1 mm gap between electrodes

ing samples. The test was stopped once all test samples had failed, or after the test had run for 1000 h.

Tests were run for different gap sizes, different ambient temperature (from 250 to 300°C, different voltages (230 to 1100 V). In most cases, milver migration was observed in less than 1000 h. The migration patterns are quite different from one sample to the other, as can be seen in figures 3b (close-up in 3c) and 3e, all coming from the same test batch. A close-up view of a different sample, using a scanning electron microscope, shows the "dendritic" aspect of the silver filament.

The time before failure as a function of the electric field (voltage difference between the electrodes divided by the gap), at 300 °C ambient, is plotted with blue round dots in figure 4. As can be seen, the time before failure is fairly short, from less than 100 h (1E-2 h^{-1}) up to 1000 h (1E-3 h^{-1}), for electric field levels that can be experienced within a real power module (less than 1000 V/mm).

As described above, silver migration occurs in the presence of oxygen. To prevent migration to occur, an idea is therefore to coat the silver layers with an oxygen barrier. Parylene HT (SCS Coatings) was found in [11] to be a good oxygen barrier and to be able to withstand long-term operation at 300 °C. Furthermore, parylene has a vapour-phase deposition process that results in uniform and conformal coating, even on complicated shapes, as we will show later in this paper.

Test samples with a 20 μm layer of parylene HT were submitted to the same test conditions as the un-coated samples (300 °C ambient). The corresponding times-to-failure are plotted with yellow triangles in figure 4. A dramatic improvement can be observed with most samples matching the 1000 h parameter without failure. One test sample was found to fail at 134 h for a 1578 V/mm field, which is probably related to a manufacturing default.

As a consequence, Parylene HT can be considered as a suitable material to mitigate the risks associated with silver migration. It is important to note that the tests presented here constitute a worst-case configuration, with silver used as the electrode material. The electric field actually experienced by a sintered silver die attach should be lower.

4 Module Manufacturing

The various parts of the sandwich module are visible in figure 5, for both designs (one set for 2.4×2.4 mm^2 dies, another for 4×4 mm^2 dies): two DBC tiles, two JFET dies, and one small copper spacer. The DBC tile with the source and gate patterns (left) will be referred to as "source" substrate, and the other one as the "drain" substrate.

The manufacturing process can be summarized as follows:

- Etching of the DBC substrates: as the accuracy re-

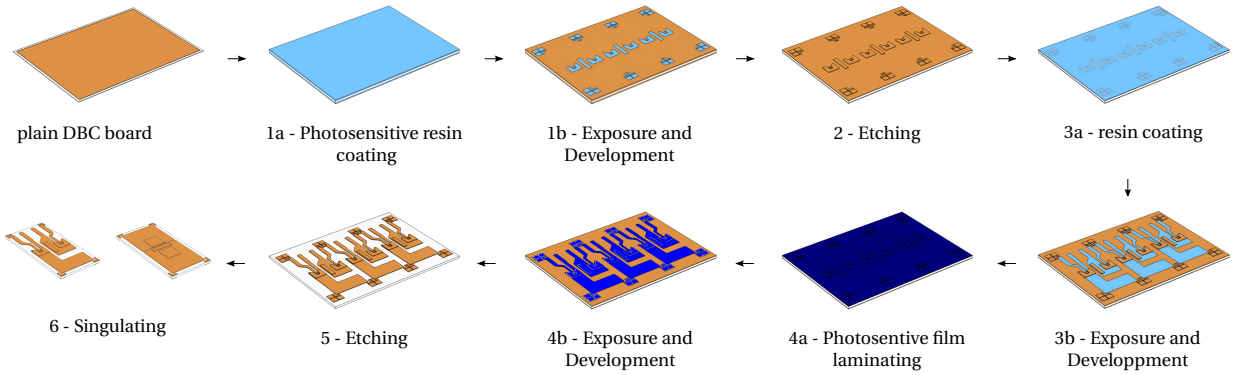

Figure 6: 2-level etching process to produce the DBC tiles.

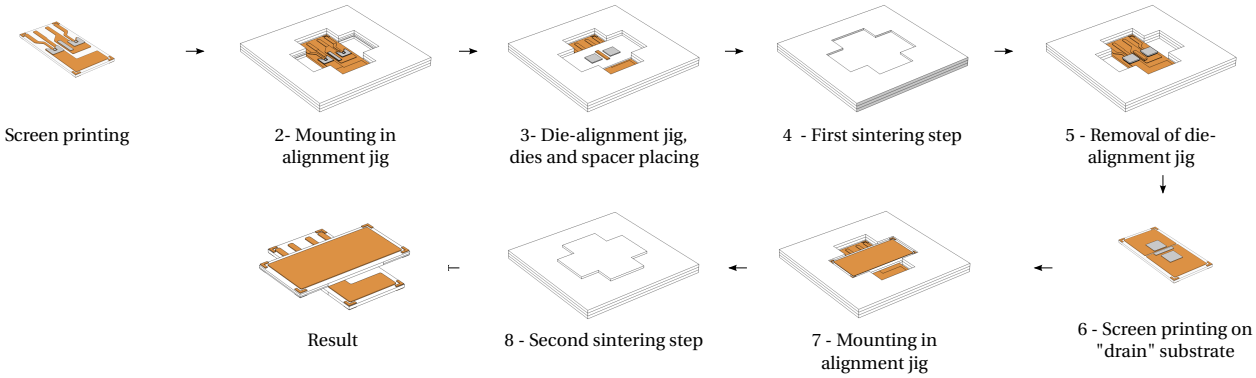

Figure 7: Assembly workflow, showing the ceramic jigs used to ensure a proper alignment of the parts. During the sintering steps, a piece of ceramic is placed over the parts for pressure distribution.

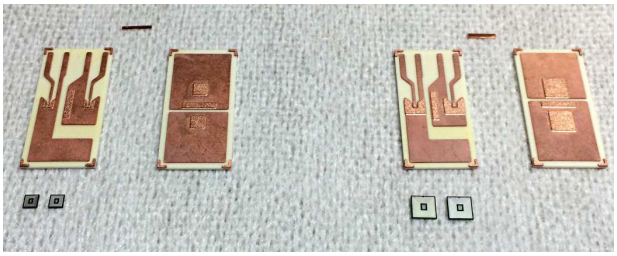

Figure 5: Two sets of parts (one for the 2.4×2.4 mm^2 JFET dies, one for the 4×4 mm^2 JFET dies) before assembly. A set comprizes two ceramic tiles, two JFETs and one spacer.

quired (see figure 2) exceeds the design rules of the DBC manufacturers we know, a custom etching process was developped;

- Die topside metallization: the JFETs have an aluminium topside metal, suited to wirebonding but not to silver sintering. A plating step is therefore required to cover the aluminum with another metal (silver);
- Assembly, using silver sintering.
- Parylene HT coating of the module

4.1 Etching of the DBC substrates

As described in section 2, a two-level etching process was required to create some copper protrusions to connect the dies. This process is described in figure 6: First, a photosensitive resin (MC dip coating, microchemicals) is applied on a plain DBC board by dip coating (6 mm/s withdrawal speed, 5 mn drying at 100 °C in an oven). It is then exposed to UV light (Quintel Q-2001 CT mask aligner, 200 W mercury lamp, 90 s) through a mask and developed using ma-D 331 (micro resist technology). The exposed copper is etched half-way through using ferric chloride (6 minutes using a spray etcher).

After cleaning, the substrate goes through a second resin coating/exposure/development process. However, because of the features now present on the copper, the resin layer was found not to be uniform enough: the crests of the protrusions only have a very thin layer of resin, not sufficient to protect them from the ferric chloride. Therefore, an additional layer of photosensitive material (Dupont PM275 photosensitive dry film) is laminated on

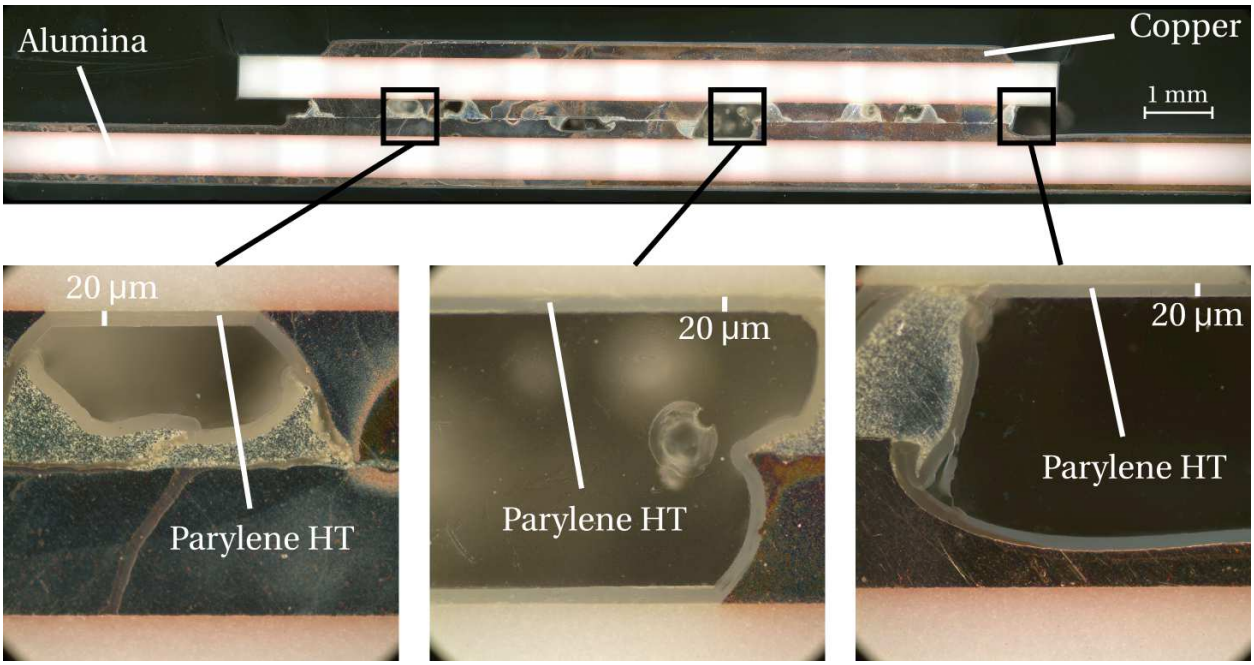

Figure 9: Cross section of a test assembly (no dies, poor control of copper etching and silver sintering) showing that the parylene HT coating is uniform over the entire sample, even in the most intricate cavities..

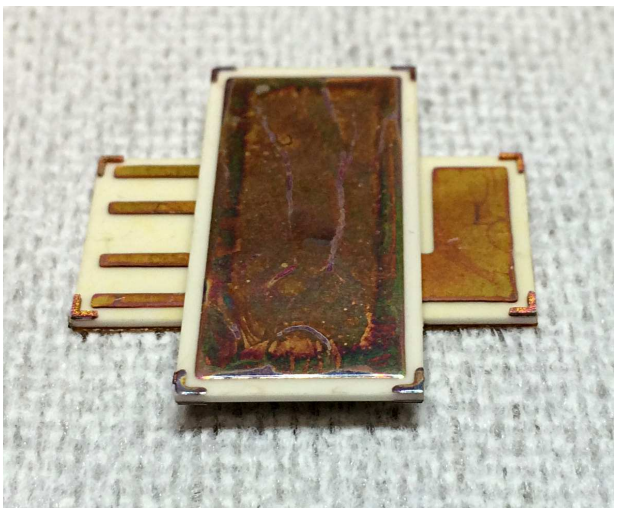

Figure 8: The module after assembly

top of the substrate (step 4a in figure 6), exposed and developed (using a 1% wt Na_2CO_3 solution).

Finally, a second etching step is performed (9 mn), the photosensitive materials are removed in acetone, and the substrates are cleaned and singulated (using a disco DAD3220 wafer saw).

Overall, the copper features are found to be within 50 μm of the desired dimensions, which is satisfying.

4.2 Plating of SiC dies

The JFET dies are mounted in a stainless-steel mask with openings matching their topside layout. The alignment is provided by pockets managed in the mask (DB Products). The mask and dies are then placed in an electron-gun evaporator (EVA300), for the deposition of Ti and Ag (200 nm).

4.3 Assembly

The assembly process is described in figure 7. The two sintering steps are performed using Heraeus LTS-117O2P2 silver paste. First, a 50 μm-thick layer of silver paste is stencil-printed on the substrate. Then a short 5-minute drying at 85°C is performed to prevent the silver paste to flow while keeping some tackiness. The parts to join are put in contact, using some alignment jigs (laser cut alumina), and placed on the heating platen of the sintering press. A 30 mn, 85 °C drying step is then performed, followed by a 70 °C/mn ramp and a 30 mn, 240 °C sintering step under a pressure of 2 MPa.

A picture of the resulting module is visible in figure 8. No cleaning was attempted after assembly, which explains the clearly visible oxidation marks on the copper. A low power electrical characterization showed that the module was functional (no short or open circuit) and that no change in performance of the devices could be observed.

4.4 Parylene coating

Because of time constraints, parylene HT coating was attempted on a non-functional, preliminary assembly with no dies. A cross section of this test vehicle is visible in figure 9. It shows that parylene forms a very uniform layer all over the module, even in the most intricate parts. Along with the high temperature results from section 3, this proves that parylene is a very attractive solution for the encapsulation of high temperature power modules.

5 Conclusion

A "sandwich" structure comprizing only high-temperature suited elements and materials has been presented. It uses silver sintering as a bonding material, and parylene HT to prevent silver migration. The complete manufacturing process, which offers a resolution compatible with the fine layout of the SiC dies has been described in details. Short terms developments consist in high voltage (540 V) tests on parylene-HT-coated functional samples over the whole temperature range.

Acknowledgement

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