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Integrated packaging allows for improvement in switching characteristics of silicon carbide devices

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The Presentation file will be available after the conference.

Abstract

Silicon Carbide devices can achieve very high switching speed, but that requires specific packaging solutions. In this paper, we discuss the effects of parasitic devices on the switching behaviour. Three different prototypes are then presented, offering three different packaging and integration approaches (low inductance packaging, integration of the gate drivers, integration of common-mode filtering). The consequences on the switching speed are discussed.

1. Introduction

Silicon carbide (SiC) power devices offer many advantages over their ubiquitous silicon-based counterparts. They can operate at much higher temperature [1], at higher voltages [2] and higher switching frequency [3].

However, special packaging techniques are required to use SiC devices at their full potential (this is also true for GaN devices). Increasing the switching speed to reduce switching losses might cause voltage spikes that could either damage the devices, or generate electro-magnetic interferences (EMI). In many cases the switching speed of the transistors is limited by the impedance of the gate loop.

In many ways, these considerations about packaging parasitics are not different from those associated to the emergence of silicon MOSFETs and IGBTs, a few years ago. The physical principles are identical with wide-bandgap devices, but their magnitude differ. High voltage silicon carbide (1200 V and more) switches are comparable in performance (switching speed, recovery, on-resistance) to low-voltage (30-50 V) silicon devices. A few years ago, we demonstrated in [4] that the switching behaviour of low voltage, MOSFET-based converters was more dictated by the parasitic devices (stray inductances) than by the MOSFETs themselves. We now expect the same to be true for high voltage, SiC based architectures.

Integration is a powerful solution to design more compact converters, in particular with lower parasitic inductances. In this paper, we present some converters that have been designed in our research labs to take full advantage of SiC devices by integrating more functions in the power module.

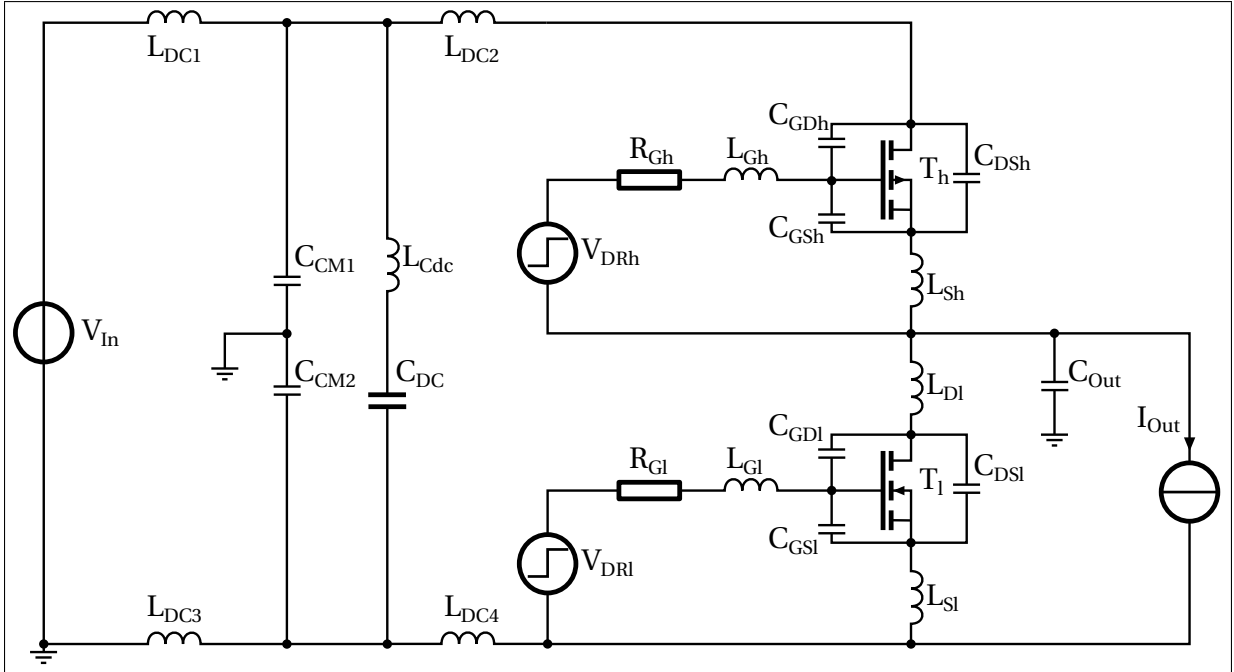


Fig. 1: Circuit diagram of a half-bridge including the main parasitic devices (resistors and inductor coupling not shown for the sake of clarity).

2. Analysis of the switching cell

2.1. Parasitic elements and switching behaviour

The circuit diagram of a half-bridge, the basic cell that will be considered here, is visible in fig. 1. In addition to the two transistors (we assume they have an internal body diode), each interconnect can be associated with parasitic resistors, inductors and capacitors. However, for the sake of clarity, only the most relevant parasitic devices are represented in fig. 1. The resistors are not shown, nor are the coupling between the inductors. Only the inductors and capacitors that are submitted to (respectively) strong current and voltage transients are depicted.

These parasitic devices caused by the layout of the converter are not the only unwanted elements. In particular, the capacitances of the power devices must be considered, as they are usually much larger than those due to the layout (in the nano-farad range, as compared to tens or hundreds of pico-farads). However, these devices capacitances are strongly non-linear (they are voltage-dependent), requiring specific characterization setup and models [5]. Some power semiconductor devices have an internal PiN body diode (as it is the case with the JFETs described below). The reverse recovery of this diode also has a strong influence on the switching performance of the circuit.

2.2. Influence of the parasitic elements

The gate inductance L_G is often relatively large (tens to hundreds of nH), because the gate drivers are kept separated from the power devices (often on a PCB located above the power module). A large L_G can slow down the commutation, or it can cause oscillations with the input capacitance of the power device. This requires a larger R_G to control the ringing, resulting in an even lower switching speed.

However, the impedance of the gate circuit must be kept low to avoid spurious turn-ons: in the case of Fig 1, when T_h turns on, the drain voltage of T_l (V_{Dl}) rises rapidly. A current proportional to $\frac{dV_{Dl}}{dt}$ flows through C_{GDl} . If the gate circuit of T_l has a low enough inductance, it will absorb most of this current, and the gate voltage of T_l will remain mostly unaffected. In the opposite, if the impedance of the gate circuit is too high, the current will flow through C_{GSl} , causing a rise in the gate voltage of T_l . If V_{GSl} exceeds the threshold voltage of the transistor, T_l turns-on, resulting in a short-circuit of V_{In} .

The drain inductance (L_{D1} , L_{DC2}) stores energy ($\frac{1}{2}LI^2$) when the corresponding transistor is on. In a hard-switching structure, this energy must be dissipated at turn-off, causing switching losses and voltage spikes. L_D also causes ringing with the capacitances of the power devices. L_D must therefore remain as small as possible. Much like for the gate drivers, the DC capacitors are kept separated from the semiconductor devices causing L_{DC2} (see fig. 1) and L_{DC4} to reach tens of nH.

The source inductance L_S is common to the power path (drain current) and to the control path (gate current). Not only does it have the same effect as described above for L_G and L_D , but it also introduces a negative feedback that opposes (slows down) both the turn-on and turn-off. Therefore, even minute values of L_S have a dramatic effect on the switching speed of the power device. Sophisticated solutions to cancel this negative feedback, for example by forcing a magnetic coupling between L_G and L_S were investigated [6], but they require an increase in L_G , which is not desirable. In any case, L_S is usually smaller than L_G or L_D , in the order of a few nH (for a half-bridge power module).

It is also worth noting that there is an optimal $\frac{L_D}{L_S}$ ratio [7]: a large value means that the devices switches rapidly (small L_S), triggering large drain voltage ringing caused by the large L_D (under-damping). A small ratio means that the transistor switches more slowly (large L_S) than required to prevent drain voltage ringing to occur (over-damping).

The parasitic output capacitance C_{Out} , formed between the output conductor and the surrounding ground, experiences fast voltage changes when the transistors switch. A current (the “common-mode current”) will flow through this capacitor and return to the voltage source “externally”, via any conductive path available (for example an metallic enclosure). This is depicted in fig. 1 by the “ground” symbol. For a standard power module, using a ceramic substrate, C_{Out} is in the order of a few tens or hundreds of pF, but can be much larger depending on the load (for example if a shielded cable is used between the converter and an electrical motor). Larger C_{out} values can also result in slower switching.

To contain the common-mode current within the converter and to prevent it from disturbing other systems, common-mode filtering capacitors (C_{CM1} and C_{CM2}) can be used. They offer a shorter path for the common-mode current, especially if L_{DC1} and L_{DC3} are large compared to L_{DC2} and L_{DC4} .

3. Design improvements

In the previous section, we estimated the orders of magnitude of the parasitic devices associated with a “standard” packaging (i.e. a power module hosting the semiconductors, with

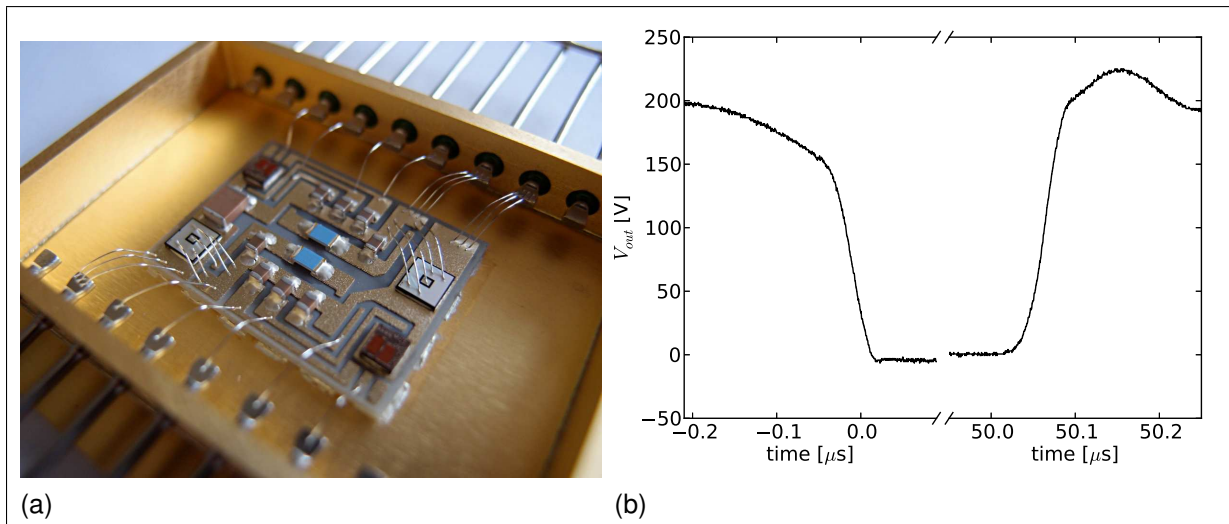


Fig. 2: The populated power substrate (before wirebonding of the gate driver circuits) in its hermetic case (without lead) (a) and the output voltage of the inverter leg ($50 \Omega/1 \text{ mH}$ load, 200 V DC bus) (b).

the gate drivers and the DC-bus capacitors on separate boards). Various concepts can be developed to overcome the limitations of such packaging. Here, we describe three different approaches:

- to reduce the size of the control and power loops, by integrating the gate drivers and (part of) the DC bus capacitance directly on the same substrate as the power devices;
- to reduce the parasitic inductance values by using a busbar structure over the entire converter
- to integrate some common-mode filtering directly in the power module, as close as possible to the source of common-mode current.

It is worth noting that these concepts were developed for high temperature applications (120 to $300 \text{ }^\circ\text{C}$ ambient) more than for fast switching performance. In many aspects, however, high temperature converters must be optimized for fast switching. For example, the proper thermal management of a system operating at elevated ambient temperature is often difficult, so a high efficiency is desirable to reduce the amount of heat to be managed. Regarding Electro-Magnetic Compatibility (EMC), high temperature passive devices are not common and very expensive, so an efficient and smaller EMC filter is preferred.

Of course, a system that would be designed from the start for high switching speed, without the constraints of high temperature operation could take advantage of many “low temperature” technologies, such as those based on printed circuit board (PCB) [8]. Nevertheless, the concepts presented here demonstrate the improvements that can be expected by integrating more functions in the power module

3.1. Integration of gate driver

The module depicted in figure 2a integrates, on the same substrate, the gate driver (custom design using Silicon On Insulator –SOI– technology), the power devices (1200 V , $50 \text{ m}\Omega$ SiC JFETs from SiCED), and some passive components (including a –small, 10 nF – 600 V DC bus capacitor). This demonstrator was designed for very high temperature operation (it was suc-

cessfully tested at 310 °C ambient), leaving only little technological choices to the designer (few available components and mounting technologies). More technical details are given in [9]. SOI is commonly used for high voltage integrated circuits such as the gate drivers, as the isolating layer limits the leakage currents that would be too high with pure silicon. Another advantage associated with SOI is a higher operating temperature [10] (usually more than 150 °C), meaning that the gate driver die can be located near the hot power devices.

However, despite the use of wirebonds to connect the dies (and to connect the dies to the long terminals of the package, as a hermetic case was required for this inverter leg), it can be seen in figure 2b that the switching transient is very fast (<15 ns rising), and with little ringing.

Some commercially available power modules have an integrated gate driver [11]. It is unclear whether this development was driven solely by the need of better switching performance, or to make the module easier to use, but it proves that the integration of the gate driver circuit is possible on an industrial scale.

3.2. Low inductance packaging

Another approach to improve switching performance is to reduce the value of the parasitic inductances. As inductance is related to the length of the conductors and the surface area of the commutation loop, This requires to modify the layout of the power module. The busbar structure (flat conductors separated by a thin dielectric layer) is a way to reduce the surface area of the commutation loop [12] and is attractive to connect the power module.

A further improvement is obtained by replacing the wirebonds interconnects. A technology called SiPLIT (Siemens Planar Interconnect Technology) uses the same principle as the busbar, with a thin dielectric layer separating the conductors in the module. This allows for a 50% reduction in parasitic inductances [13]. Another approach is the “sandwich” structure [14], where the power devices are placed between two metal-ceramic substrates. In addition to an improved inductive behaviour (although probably not as reduced as with the SiPLIT), the sandwich structure allows to cool the power devices by both sides (double side cooling) [15].

The power converter described here uses both busbar interconnects and sandwich structure. It was designed to operate in the vicinity of an internal combustion engine, in a hybrid car, with a cooling fluid temperature of up to 120 °C[16]). For this converter, a direct cooling technique

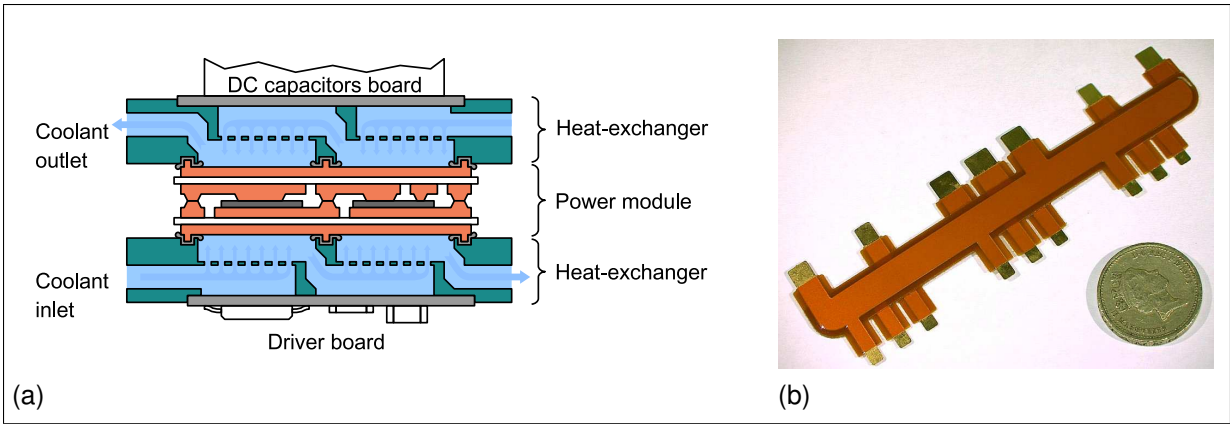


Fig. 3: Cross-section of the “double-side” cooling structure (a) and photograph of the laminated busbar used to connect the capacitor board to the power modules (b).

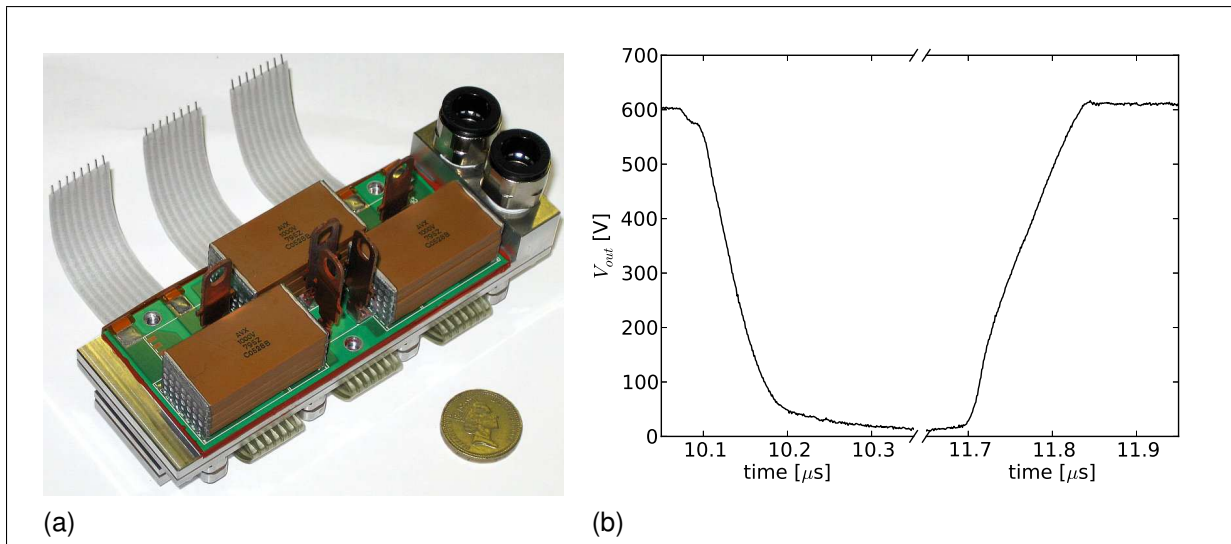


Fig. 4: The complete inverter, with the top cover removed, showing the ceramic capacitors (a). The three ribbons visible on top are the signal and power supply connections to the gate driver boards (not visible). Switching waveform captured at the output of one of the inverter legs, for a 600 V DC bus and 7 A phase current (on an inductive load) (b).

was selected, where the cooling fluid is in direct contact with the back of the power module substrates (fig. 3a). This allows both for low parasitic inductance and very low thermal resistance from junction to fluid (<0.4 K/W, [17]).

A laminated busbar (fig. 3b) is used to provide a low-inductance connection between the DC capacitor board and the “sandwich” modules. The capacitor board itself uses insulated metal substrate (IMS), which by design generates very small parasitic inductances. Overall, from the terminals of the inverter to the sandwich modules, a parasitic inductance of 10 nH was measured [17].

The complete inverter, visible figure 4a is equipped with 6 1200 V silicon IGBTs and 6 Schottky Barrier Diodes (SBDs). An example of waveform captured at the output terminal of one of the sandwich modules is visible in figure 4b. Thanks to the absence of recovery phenomenon (use of SBDs) and to the low-inductance design, the waveforms show no ringing at the nominal voltage and current.

3.3. Integration of common-mode filtering

Increasing the switching speed is usually an advantage from the thermal and efficiency points of view, but has detrimental effects on the EMC. In particular, as explained in section 2.2, higher dv/dt at the output of the bridge causes an increase in the common-mode (CM) current flowing through the parasitic capacitor C_{out} (see figure 1). Although filtering higher frequency harmonics is in theory easier because it requires smaller passive devices, it is not so simple in the case of CM current: the location of the filter is also important, to provide a short path to keep the CM current within the converter or within the module.

A solution is to directly integrate the CM filter capacitors (C_{CM1} and C_{CM2} in figure 1) directly in the power module, as visible in figure 5a [18]. This makes it possible to “capture” the high frequency harmonics directly at the source. In this way, a simpler input filter is required (for example a first order filter instead of a second order). An example of the EMI spectrum emit-

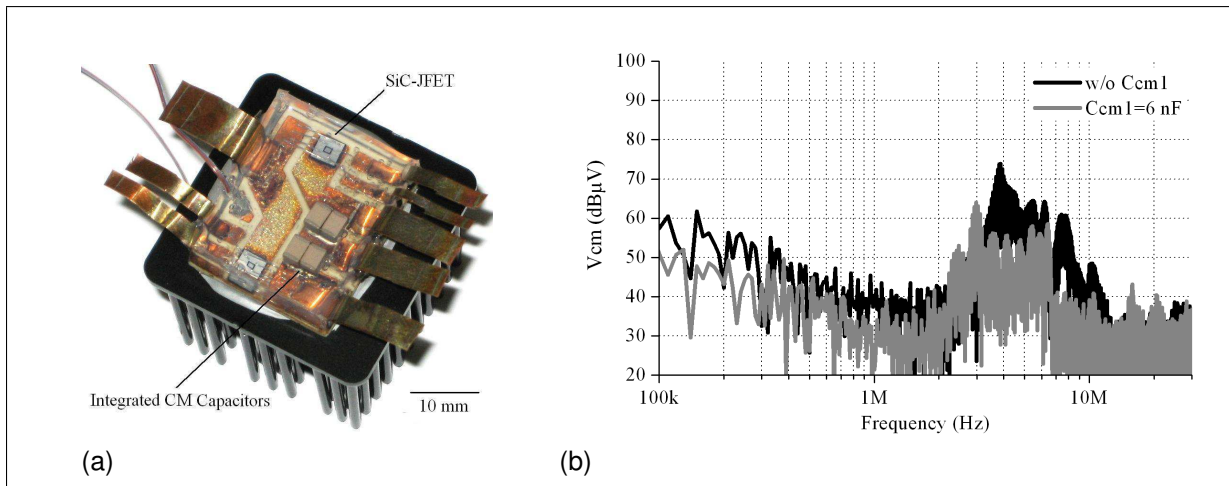


Fig. 5: The power module with integrated common mode filtering (capacitors). This module is an inverter leg, using two SiC JFETs (SiCED) (a). Effect of the Common-Mode (ccm) capacitors on the EMI spectrum, compared to a module with the same layout, but without any capacitor mounted (b).

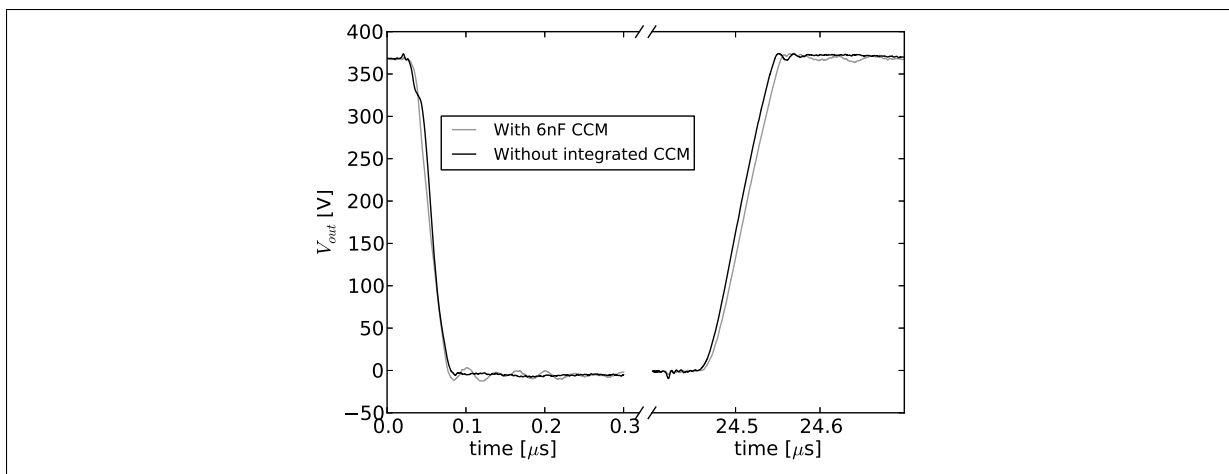


Fig. 6: Switching waveform captured at the output of the module, for a 365 V DC bus and 1.7 A phase current (on an inductive load).

ted with and without the integrated filtering is visible in figure 5b. The waveforms in figure 6 show that there is no noticeable effect of the integrated capacitors on the switching speed, and therefore on the efficiency of the converter.

4. Discussion and Conclusion

The three approaches developed here offer improvements over standard packaging, allowing switching times as small as 15 ns. If the “sandwich” structure requires a large alteration of the manufacturing process (in particular, power devices with a suitable topside metallization are needed), this is not the case for the other modules. Gate driver or common-mode capacitors are integrated using the standard “planar” technology.

The main downside of this approach is the additional module space required for the integrated functions. For a silicon-based module, this might be an issue as the size of the module is often dictated by the number of power dies to accommodate (the dies are placed as close as

possible to each other). In a SiC-based module, however, the dies are smaller. They are placed further from each other for thermal considerations, so integrating additional functions might be possible with limited consequences on the the size of the module.

In any case, a specifically-designed packaging is required to make the most of the excellent existing SiC Devices.

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