



# Thin film transistors fabricated by in-situ doped unhydrogenated polysilicon films obtained by solid phase crystallization

Laurent Pichon, K. Mourgues F. Raoult T. Mohammed-Brahim K. Kis-Sion  
D. Briand O. Bonnaud

## ► To cite this version:

Laurent Pichon, K. Mourgues F. Raoult T. Mohammed-Brahim K. Kis-Sion D. Briand O. Bonnaud. Thin film transistors fabricated by in-situ doped unhydrogenated polysilicon films obtained by solid phase crystallization. Semiconductor Science and Technology, 2001, 16, pp.918-924. hal-00994988

**HAL Id: hal-00994988**

**<https://hal.science/hal-00994988>**

Submitted on 22 May 2014

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# **Thin Film Transistors fabricated by *in-situ* doped *unhydrogenated* polysilicon films obtained by Solid Phase Crystallization**

L. PICHON<sup>\*</sup>, K. MOURGUES, F. RAOULT, T. MOHAMMED-BRAHIM,  
K. KIS-SION, D. BRIAND, O. BONNAUD

Groupe de Microélectronique et Visualisation, UPRESA 6076, Université de RENNES I,  
Campus de Beaulieu, 35042 RENNES cedex, FRANCE, phone : (33) 02 99 28 60 69  
fax : 02 (33) 99 28 16 74 e-mail : lpichon@greyc.ismra.fr

Permanent address : GREYC, ISMRA-Université de Caen, UPRESA 6072, 6 boulevard du Maréchal  
Juin, 14000 Caen, France.

*Abstract-* High mobility low temperature ( $\leq 600^\circ\text{C}$ ) *unhydrogenated in-situ* doped polysilicon thin film transistors are made. Polysilicon layers are grown by a LPCVD technique and crystallized in vacuum by a thermal annealing. Source and drain regions are *in-situ* doped. Gate insulator is made of an APCVD silicon dioxide. Hydrogen passivation is not performed on the transistors. One type of transistors is made of two polysilicon layers, the other one is constituted of a single polysilicon layer.

The electrical properties are better for transistors made of single polysilicon layer: a low threshold voltage (1.2 V), a subthreshold slope  $S = 0.7$  V/dec, a high field effect mobility ( $\approx 100 \text{ cm}^2/\text{Vs}$ ) and a On/Off state current ratio higher than  $10^7$  for a drain voltage  $V_{\text{ds}} = 1$  V.

At low drain voltage, for both transistors, the Off state current results from a pure thermal emission of trapped carriers. However, at high drain voltage, the electrical behavior is different: in the case of single polysilicon TFTs, the current obeys the field-assisted (Poole-Frenkel) thermal emission model of trapped carriers while for TFTs made of two polysilicon layers, the higher Off state current results from a tunnel effect.

## I. INTRODUCTION

Since the early 80's low temperature Thin Film Transistors (TFTs) technologies are of a very great interest for elaboration of Active Matrix Liquid Crystal Displays (AMLCDs) and two-dimensionnal imaging systems [1]. Many investigations are carried out with the aim of developing, at the lowest cost, fabrication processes of polysilicon TFTs with improved electrical properties leading to a high field effect mobility and On/Off state switching [2-4].

Studies were made to optimize deposition and crystallization conditions of polysilicon layers leading to larger polysilicon grains in high-performance TFT's. From these studies it appears that crystallinity of polysilicon can be improved by adjusting the deposition pressure [2,5] and the crystallization technique suitable with the maximum withstood temperature of a low-cost glass substrate [6,7]. Moreover, for long time many studies showed that a polysilicon film deposited in the amorphous state and then crystallized by a low temperature ( $\leq 600^{\circ}\text{C}$ ) thermal annealing contains grains of larger size than in the case of polysilicon as deposited film. In previous works [5], we showed that the size and the quality of the grains depend on deposition parameters of the deposited amorphous silicon layer such as pressure and temperature. The resulting quality of the amorphous material is much better as the deposition pressure is close to the pulverulence limit pressure (ie the polysilicon looks like powder after deposition).

The low temperature ( $\leq 600^{\circ}\text{C}$ ) crystallization thermal annealing, the so-called Solid Phase Crystallization (SPC), is the lowest-cost crystallization technique: silicon is deposited in the amorphous state and then crystallized by a thermal annealing [5]. On the other hand, the Excimer Laser Annealing (ELA) is the most important and promising crystallization technique of TFT polysilicon layers. But this process is more expensive and more difficult to implement, in particular in terms of surface roughness [8]. However, excimer laser annealed polysilicon layers offer usually a higher degree of crystallinity[9]. Therefore, a hydrogen passivation is

needed to improve the electrical properties of the SPC-Poly-Si layers [1] and thus a prematured aging (due to the presence of a large content of hydrogen atoms) of the TFTs cannot be avoided [10].

Furthermore, the doping process of the polysilicon layer can be a key-issue to substantially improve the quality of the Poly-Si such as the amorphization of polysilicon layers thanks to implantation doping process [11]. But, it is worth noting that, if this later doping process is the most common to dope the polysilicon layers, the *in-situ* doping one can be a good alternative, suitable with a low temperature thermal annealing. A control of the doping concentration at a low level is possible, and a long-time thermal annealing can be avoided as in the case of implanted ones [12].

Moreover, in the case of LCD-TFTs, gate insulation by a high-temperature thermal oxidation process is not possible. However, alternative technologies can be used, such as Chemical Vapor Deposition (CVD) [13,14], Rapid Thermal Oxidation [15], Low Thermal Oxidation [16], and sputtered silicon dioxide deposition [17]. Usually, by using these types of insulation processes, the gate insulator/active layer interface is not of a good quality and therefore some investigations were made in order to improve the surface treatment of the active layer [14,18]. In particular, it was observed that the oxygen plasma acts as a cleaning process of the active layer surface and reduces the interface state density by passivation of the dangling bonds [18]. Furthermore, the combination of an oxygen plasma plus an RCA-type cleaning can ensure a good gate insulator/active layer interface quality [4,19]. Therefore, we showed that this last cleaning process allows an improvement of the electrical properties of the TFTs such as: a decrease of the threshold voltage and of the subthreshold slope, and an increase of the field effect mobility [19].

In this paper, we present the fabrication processes of polysilicon TFTs, exhibiting high electrical properties. Accordingly to our previous works [4,5,14,19], we took into account of

the advantages of: i) *the in-situ* doping process, ii) the effect of the pressure deposition of the polysilicon layers and thus of the SPC technique, and iii) the cleaning plasma effect before deposition of gate insulator. The first point leads to deposit one single film with undoped back region and highly doped up region that can be removed to define channel zone in the bulk of the deposited film leading to a significant improvement of the process. Moreover, one the objective of this study is to analyse and understand the several conduction mechanisms in both structures to explain the differences in the electrical characteristics previously observed.

## II. EXPERIMENT

Low temperature ( $\leq 600^\circ\text{C}$ ) *unhydrogenated in-situ* doped polysilicon thin film transistors are made through a four-mask aluminium gate process. Two types of process are studied.

### *Process I. (fig. 1. a)*

At first, a 150 nm thick undoped amorphous silicon layer is deposited by LPCVD technique on an  $\langle 100 \rangle$  n-type oxidized monosilicon wafer. Then, amorphous polysilicon layer is plasma etched into islands, by Reactive Ion Etching (RIE), to form the active layer. After that, a second 150 nm thick phosphorus heavily *in-situ* doped LPCVD amorphous silicon layer is deposited with a phosphine/silane mole ratio equal to  $4 \times 10^{-4}$ . The phosphorus concentration is equal to  $4 \times 10^{20} \text{ cm}^{-3}$  [20]. The two amorphous silicon layers are deposited at  $550^\circ\text{C}$  and then crystallized by SPC technique: a thermal annealing in vacuum at  $600^\circ\text{C}$  during 12 hours ensures the crystallization. The heavily *in-situ* doped SPC-polysilicon layer is plasma etched to form the source and the drain regions. Furthermore, an RF oxygen plasma is performed at room temperature for ten minutes on the structure before an RCA-type cleaning to ensure a good active layer/gate insulator interface quality as described in introduction. Therefore, a 60 nm thick APCVD  $\text{SiO}_2$  layer is deposited at  $450^\circ\text{C}$  during 2.5 min with a silane/oxygen gas

mixture, to insulate the gate electrode. A thermal annealing in nitrogen at 600°C during one hour is carried out to ensure densification of the APCVD SiO<sub>2</sub> gate insulator. Finally, Aluminium is thermally evaporated and wet etched to form source, gate and drain electrodes. Usual post-metallization annealing is performed at 390°C in an atmosphere of forming-gas to improve aluminium contacts.

#### *Process II (fig. 1. b)*

In the second process, a 300 nm thick LPCVD amorphous silicon layer, with two differently doped stacked regions, is deposited and crystallized in the same conditions to those of the process I. The 150 nm thick lower half layer is undoped and the upper half layer is heavily *in-situ* doped with a phosphorus doping concentration equal to  $4 \times 10^{20} \text{ cm}^{-3}$  [20]. Therefore, the heavily *in-situ* doped region is first plasma etched to define the channel, the source and the drain regions. After the protection of the channel with a photoresist mask, source and drain regions, the undoped region is plasma etched to insulate the structures. After that, cleaning and surface treatment of the active layer, gate insulation and metallization steps are identical to those in the process I. It is worth to notice that for the TFT fabricated through this process, the active layer, the source and drain regions are located on the same polysilicon layer.

At this level, we mention that the two types of transistors did not undergo a specific hydrogen passivation, but only a usual forming-gas annealing in order to improve the aluminium contacts.

Electrical characterization of the TFTs is performed in darkness, using a HP 4145 B semiconductor parameter analyser.

### III. RESULTS AND DISCUSSION

Electrical characterization of the two types of TFTs shows classical output characteristics (figure 2): a linear mode at low drain voltages and a saturation mode at high drain voltages, with a good modulation of the drain current with the gate voltage. We can deduce that each type of TFTs has good ohmic contacts. Furthermore, we can notice that the bilayer-poly-Si TFTs (process I) exhibit a lower drain current level. This can be attributed, in main part, as it will be further discussed, to the poorer channel region quality, and the active/drain layers interface, which may act as a large grain boundary, responsible of the decrease of the field effect mobility and of the increase of the threshold voltage in bilayer-poly-Si TFTs.

Transfer characteristics for both TFTs are plotted in figure 3. In the case of monolayer-poly-Si TFTs, the transfer characteristics shift to lower gate voltages, which shows a lower threshold voltage in this type of TFTs. Furthermore, the On/Off state switching (subthreshold slope) and the On state current level are better. At low drain voltage ( $V_{ds} = 1V$ , fig. 3. a), the Off state current is weakly dependent on the gate voltage. In comparison to the bilayer polysilicon TFTs, the monolayer-poly-Si TFTs show lower leakage current in the range of large negative gate voltage and slightly higher minimum of the leakage. At high drain voltage ( $V_{ds} = 13V$ , fig. 3. b) the Off state current is strongly dependent on the gate voltage and is higher in the case of bilayer-poly-Si TFTs.

Table I summarizes electrical parameters of the TFTs deduced from the electrical characterization. Electrical parameters such as field effect mobility ( $\mu_{FE}$ ) and threshold voltage ( $V_T$ ) were determined according to the simplified electrical model [21].  $\mu_{FE}$  is calculated from the slope of the  $I_{ds}(V_{gs})$  curve (transconductance) plotted in the linear mode.  $V_T$  is determined in the saturation mode by the intercept of the  $I_{ds}^{1/2}$  versus  $V_{gs}$  curve with the axis gate voltage. The subthreshold slope (S) is the measured reciprocal slope of the transfer characteristics in the switching region [14]. On/Off current ratio is calculated at  $V_{ds} = 1V$ : On state current is the drain current measured at  $V_{gs} = 20V$  and Off state current is the



minimum of the drain current in the transfer characteristics. Therefore, as it has been discussed previously, we observe a decrease of the threshold voltage (from 4 to 1.2 V), of the subthreshold slope (from 1 to 0.7 V/dec), and an increase of the field effect mobility (from 63 to 100 cm<sup>2</sup>/Vs) from the bilayer to the monolayer-poly-Si TFTs. It is worth to notice that these results are very good for the two types of *unhydrogenated* polysilicon TFTs, in comparison with those usually obtained in hydrogenated ones [1]. Moreover, the high gate length (L=25μm) of the TFTs and the crystallization temperature (600°C) cannot be suspected of a reduction of the gate length due to a diffusion of the dopant into the channel during crystallization, and thus of an overestimation of the calculated field effect mobility. These good results can be attributed to the combined effects of: i) the good quality of the 150 nm thick polysilicon layers [7], ii) the good surface treatment of the active layer [14,19], and iii) to the high quality of the APCVD SiO<sub>2</sub> [14].

Furthermore, these results express an improvement of the electrical properties of TFTs fabricated according to the process II. This is due to a better gate insulator/active layer interface. Figure 4 shows the Transmission Electronic Microscopy (TEM) micrographs of polysilicon layers elaborated in the same conditions to those of TFTs. We can observe that an interface is clearly visible at halfheight in the case of bilayer structures whereas none is observed in monolayer ones. Under the deposition and annealing conditions, nucleation is known to start preferentially at the amorphous silicon (a-Si)/SiO<sub>2</sub> interface, and therefore the grains are growing up to the surface, leading to a columnar structure. Between the two deposition steps of polysilicon layers of bilayer-poly-Si TFTs, impurities are adsorbed on the first layer surface and remain, in spite of an HF rinsing. At the beginning of the annealing, the inferior layer crystallizes from the SiO<sub>2</sub>/a-Si interface. The presence of impurities at the junction between the two amorphous layers might lead to a second front of nucleation, however not enough activated to induce a significant growth of grains before the grain

growing from the inferior interface reaches it. The front of crystallization, which is not regular because of the variation of the grain growth rate due to the different crystallographic orientations of the grains [22], meet then a disrupted zone stopping its monotoneous advance. The up-layer starts to crystallize from this superior interface. This last one is very rough (fig. 4. a) since it is formed with the coalescence between the inferior grains and the line of seeds resulting from the adsorbed impurities. On the contrary, the deposition process of the polysilicon layer of monolayer-poly-si TFTs does not involve introduction of impurities. Consequently, none interface has to be observed, and that is shown in Fig. 4. b. Note that this last figure indicates too that crystallization does not start from the air/heavily-doped silicon interface, confirming that the crystallization of the doped layer of the bilayer-poly-Si TFT starts from the a-Si/poly-Si interface. Because the active layer of the channel is located in this area after dry etching of the *in-situ* doped region, the choice of the two proposed processes might play a preponderant role on the characteristics of the transistors. Moreover previous studies showed that the polysilicon layers have good structural and electrical properties in particular such as a grain size of the same order of the film thickness [23] and a density of states DOS lower than  $10^{18} \text{ cm}^{-3} \text{ eV}^{-1}$  [24]. Furthermore, the large increase of the field effect mobility suggests that the interface quality improvement is not the only responsible. We have to consider the existence of the polysilicon layer interface in the bilayer-poly-Si TFTs, near the drain region, which may also contribute to the dispersion of the field effect mobility in these TFTs. Moreover, a SIMS analysis showed the presence of phosphorus atoms in the initially undoped region of constant concentration and within the range of  $10^{17} \text{ cm}^{-3}$ . This concentration is lower than the volume average defect density which is close to  $5 \times 10^{17} \text{ cm}^{-3}$ . Thus, i) the intragranular mobility is not affected by this rather low doping level, ii) the compensation of active defects by the doping concentration should decrease the barrier height at grain boundaries and allows to increase the global field effect mobility and, iii) the doping

concentration can create a small shift of the threshold voltage. Furthermore, the improvement of the field effect mobility can be also attributed to the oxygen plasma : it creates an oxidation of the channel region, and thus the resulting native oxide is removed by the RCA-type cleaning which reduces the surface roughness in the channel region. Moreover, this oxygen plasma reduces the interface state density by passivation of the dangling bonds [18] which is responsible of the improvement of the electrical parameters such as the threshold voltage and the subthreshold slope.

Lets us to remark that the field effect mobility value for such monolayer-poly-Si TFTs ( $100\text{cm}^2/\text{Vs}$ ) is a record for TFTs built in solid phase crystallized polysilicon layers, where in this case it is usually stated that the values lies in the range  $20\text{-}30\text{ cm}^2/\text{Vs}$  [25]. Moreover, this high value is representative of more than 80% for each batch of more one hundred transistors, fabricated on 2 inches dimensioned substrates from several processes.

In figure 3. a, transfer characteristics show different behaviour of the leakage current before and after  $V_{\text{gs}} = -5\text{V}$ . For  $V_{\text{gs}} > -5\text{V}$  (region I) the  $I_{\text{ds}}(V_{\text{ds}})$  curves present a linear behaviour for the two types of TFTs for  $V_{\text{ds}} \leq 1\text{V}$ . This later traduces an ohmic conduction of the whole active layer thickness. Therefore, in the monolayer-poly-Si TFT, the higher minimum drain current of the transfer characteristics, can be explained by a lower active layer resistance in this type of TFTs. In the case of bilayer-poly-Si TFTs the channel region is located in a pertubated region due to the existence of the two polysilicon layers. This region exhibits a high electrical resistivity. Thus, we can consider that the ohmic conduction in the bilayer-poly-Si TFTs is mainly ensured through a lower effective active layer thickness than in the case of monolayer-poly-Si TFTs. Thus, the resistance of the active layer is higher for the bilayer-poly-si TFTs leading to a lower value of the drain current in the region I. Moreover, for  $V_{\text{gs}} < -5\text{V}$  (region II) the leakage current is independant of the gate voltage and is higher for bilayer-poly-Si TFTs. This can be explained by a higher thermal emission of trapped

carriers in the space charge region of the drain junction due to a higher defect density in this type of TFTs. This means that in the region I, the leakage current is due to the ohmic conduction of the polysilicon film, whereas in the region II generation of trapped carriers is the main mechanism responsible for the leakage current.

In Fig. 5 we plot the off-state current versus the reciprocal temperature (for the temperature varying from 290 to 470 K) at  $V_{ds} = 1V$  and  $V_{gs}$  varying from -3 to -20 V. For the two types of TFTs the linearity of the curves with the same activation energy ( $E_A = 0.59$  eV) show that the off-state current is due to a pure thermal emission the drain junction, where the electrical conduction model can be given by the relationship:

$$I \approx I_0(V) \exp \left( - \frac{E_A}{kT} \right) \quad (1)$$

where  $V (= V_g - V_d - V_{fb})$  is the voltage accross the drain region, and  $V_{fb}$ , the flat band voltage, is the gate voltage determined at the minimum of the drain current of the tranfer characteristics. These results are similar to those obtained in the case of hydrogenated TFTs [26]. Furthermore, we have to notice that the activation energy in both regions has the same amplitude since  $E_A$  in region I reflects the activation energy of the resistivity of the undoped polysilicon film which is proportionnal to  $\exp(-E_G/2kT)$  where  $E_G$  is the energy gap of the silicon, and in region II it reflects the thermal emission from midgap traps located at the grain boundaries.

However, at high drain voltages ( $V_{ds} = 13$  V, fig 3. b) the electrical behavior of the off-state current is quite different. In order to understand this difference, we analysed the field enhanced emission of carriers at the drain junction. Usually, the local electric field  $F$  is given by the following expression  $F = (V_{gs} - V_{ds} - V_{fb})\epsilon_{SiO_2}/(\epsilon_{Si} t_{ox})$  and the Poole-Frenkel type

mechanism gives a current described by [27]:

$$I = I_0 e^{-\frac{E_i - q\sqrt{\frac{qF}{\pi\epsilon_0\epsilon_s}}}{2kT}} \quad (2)$$

where  $I_0$  is the generation current at zero electric field and  $E_i$  the energy barrier. In Fig. 6 we plot the  $I_{ds}$  versus  $\sqrt{V_{ds}}$  curve in a semi-logarithmic scale. In the monolayer-poly-Si TFTs, at gate voltages  $V_{gs} < -6V$  (fig 6b) the linearity of the curves shows that the Off state conduction obeys the former relationship by approaching the local electric field only by its lateral component indicating that in our case the drain voltage is mainly responsible for the lowering of the energy barrier  $E_i$  at the grain boundary as it has been previously observed [26]. Let us note that the plot of the  $I_{ds}$  versus  $F$  does not lead to a linear curve, that confirms the previous explanation. However, for the bilayer-poly-Si TFTs this model seems to be valid only at gate voltages  $V_{gs} > -6V$  (Fig 6a). At more negative gate voltages, the Off-state current seems to be strongly dependent both the drain and gate voltages but does not obey the former relationship. This suggests that the electrical conduction could result from a field-enhanced type thermal emission. Indeed, it is worth to notice that accordingly to the plots of the figure 6.b, the electrical behaviour of the off-state current of the monolayer-poly-Si TFTs is similar to that of hydrogenated bilayer-poly-Si TFTs previously studied [26]. In this case we observed a decrease of the activation energy of the corresponding current at high drain and gate voltages, and a decreasing thermal dependence of the current when the temperature decreases. Thus, the lowering of the Off state current in the monolayer-poly-Si TFTs can be explained by the combined effects of i) the lack of active/drain layer interface, ii) and a better gate insulator/active layer interface quality as it has been observed in figure 4. In the TFTs from the

process II, these effects lead to a significant reduction of the defect density in the space charge zone of the drain junction, as in the case of hydrogenated bilayer-poly-Si TFTs. Therefore, the field-assisted (Poole-Frenkel) thermal emission of trapped carriers from these defects is less important in the monolayer-poly-Si TFTs. On the contrary, in the case of bilayer-poly-Si TFTs, the higher defect density and the higher local electrical field at the drain junction may strongly contribute to a higher Off state current resulting from tunnel emission of trapped carriers.

#### IV CONCLUSION

In this paper two types of four-mask aluminium gate fabrication processes of *unhydrogenated in-situ* doped polysilicon thin film transistors are presented. The electrical characterisation shows that the electrical properties are better in TFTs made by a single polysilicon layer. Furthermore, this last process is very competitive to those obtained from ELA polysilicon TFTs because of its relative low-cost fabrication process (including only four mask steps, SPC and *in-situ* doping techniques, and avoiding hydrogen passivation step), and the good reproducibility in terms of surface roughness. Therefore, thanks to a relatively high field effect mobility, our monolayer-poly-Si TFT process could be a good alternative for a low-cost production process of TFTs for driving circuits applications.

These good performances are mainly attributed to the better crystallinity of the active layer and of the gate insulator/active layer interface, and to the lack of active/*in-situ* doped drain layers interface in the monolayer-Si-poly TFTs fabrication process. This later allows a reduction of the defect density at the drain junction, responsible for the emission of trapped carriers at the Off state. Therefore, in monolayer-poly-Si TFTs, we observe a lower off-state current for high voltages. However, the current level remains still high. But, we have to consider that some improvements could be brought by a control of the doping process in the

transition region from the active layer to the drain region allowing the elaboration of a lightly doped drain region in this type of TFTs. Thus, a more significant lowering of the drain current level at the Off state could be considered. In this case, TFTs could be promising candidates for switching pixel application in large-area AMLCDs.

**Acknowledgement :**

The authors want to thank L. Hadji with the GMV for TEM photographs.

## REFERENCES

- [1] O. Bonnaud, ESSDERC' 98 proceedings, Edition frontières“, p 42 1998.
- [2] C. A. Dimitriadis, P. A. Coxon, N. A. Economou, “ Leakage current of undoped LPCVD polycrystalline silicon thin film transistors ”, *IEEE Trans. Electron Devices*, vol ED-42, N°5, p 950, 1995.
- [3] D. N. Kouvatsos, A. T. Voutsas, M. K. Hatalis, “ High-performance thin-film transistors in large grain size polysilicon deposited by thermal decomposition of disilane ”, *IEEE Trans. Electron Devices*, vol ED-43, N°9, p 1399, 1996.
- [4] L. Pichon, F. Raoult, O. Bonnaud, J. Pinel, M. Sarret “ Low temperature ( $\leq 600^{\circ}\text{C}$ ) polysilicon thin film transistors having in-situ doped polysilicon source and drain contacts, *IEEE Electron Device Lett.*, vol EDL-16, N°9, p 376, 1995
- [5] T. Mohamed-Brahim, M. Sarret, D. Briand, K. Kis-Sion, O. Bonnaud, A. Hadjaj, “ Polycrystalline silicon characteristics dependence on starting amorphous silicon ”, *Journ. de Phys IV*, vol 5, C5 p 913, 1995.
- [6] A. Mimura, N. Konishi, K. Ono, J. I. Ohwada, Y. Hosokawa, Y. A. Ono, T. Suzuki, K. Myiata, H. Kawakami, “ High performance low-temperature Poly-Si n-channel TFT's for LCD ”, *IEEE Trans. Electron Devices*, vol ED-36, N°2, 1989.
- [7] H. Kuriyama, H. Hamada, “ Excimer laser annealing technology for poly-Si thin film transistors fabrication ”, *ESSDERC' 96 Proceedings*, Editions frontières, p 1041,1996.
- [8] D. Pribat, P. Legagneux, F. Plais, C. Reita, F. Petinot, O. Huet, “ Low temperature polysilicon material and devices ”, *Mat. Res. Soc. Symp. Proc.*, Vol. 424, p 127, 1996.
- [9] T. Noguchi, A. J. Tang, J. A. Tsai, R. Reif, “ Comparison of effects between large-area-beam ELA and SPC on TFT characteristics ”, *IEEE Trans. Electron Devices*, vol ED-43, N°9, p 1454, 1996.



- [10] L. Pichon, F. Raoult, T. Mohammed-Brahim, O. Bonnaud, H. Sehil, “ Effects of the in-situ drain doping on hot-carrier degradation in polysilicon thin film transistors, *Solid-State Electron.*, vol 39, N°7, p 1065, 1996.
- [11] K. T. Y. Kung, R. Reif, “ Comparison of thin-film-transistors fabricated at low temperatures ( $\leq 600^{\circ}\text{C}$ ) on as-deposited and amorphized-crystallized polycrystalline Si ”, *J. Appl. Phys.*, vol 61(4), 1987.
- [12] H. Biay-Cheng, M. K. Hatalis, D. W. Greve, “ Low-temperature polycrystalline silicon thin-film-transistors for displays ”, *IEEE Trans. Electron Devices*, vol ED-35, N° 11, 1988.
- [13] Amir. A Lakani, ”Device-quality  $\text{SiO}_2$  film on InP and Si obtained by operating the pyrolytic CVD reactor in the retardation regime, *Solid-State Electron.*, vol 27, p 921, 1984.
- [14] L. Pichon, F. Raoult, K. Mourgues, O. Bonnaud, “ High performances of low temperature ( $\leq 600^{\circ}\text{C}$ ) unhydrogenated polysilicon thin film transistors ”, *Mat. Res. Soc. Symp. Proc.*, Vol. 403, p 417, 1996.
- [15] K. Ohyu, Y. Wade, S. Lijima, S. N. Natsuaki, “ Highly reliable thin silicon dioxide layers grown on heavily phosphorus doped poly-Si by rapid thermal oxidation ”, *J. Electrochem. Soc.*, vol 137, p 2261, 1990.
- [16] G. Sarabayrouse, P. Taurines, E. Scheid, D. Bielle-Daspét, A. Martinez, “ Feasibility and electrical properties of  $600^{\circ}\text{C}$  thermal silica layers for thin film transistors applications ”, *Thin Solid Films*, vol 197, p 21, 1991.
- [17] S. Suyama, A. Okamoto, T. Serikawa, “ the effects of oxygen-argon mixing on properties of sputtered silicon dioxide films, *J. Electrochem. Soc.*, vol 134, p 2260, 1987.

- [18] N. H. Nickel, P. Mei, J. B. Boyce, “On the nature of the defect passivation in polycrystalline silicon by hydrogen and plasma treatments”, *IEEE Trans. Electron Devices*, vol ED-42, N°8, p 1559, 1995.
- [19] L. Pichon, F. Raoult, K. Mourgues, K. Kis-Sion, T. Mohammed-Brahim, O. Bonnaud, “Low temperature ( $\leq 600^{\circ}\text{C}$ ) unhydrogenated in-situ doped polysilicon thin film transistors: towards a technology to flat panel displays”, *Thin Solid Films*, vol 296, p 133, 1997.
- [20] M. Sarret, A. Liba, O. Bonnaud, “Low pressure chemical vapor deposition of low in-situ phosphorus doped silicon thin films », *Appl. Phys. Lett*, 59 (12), p 1438, 1991.
- [21] S. M. Sze, *Physics of Semiconductor Devices*, Wiley, New York, 2nd edition, p 442, 1981.
- [22] L. Haji, P. Joubert, J. Stoemenos, N. A. Economou, “Mode of growth and microstructure of polycrystalline silicon obtained by solid-phase crystallization of an amorphous silicon film”, *J. Appl. Phys.*, vol 75, n°8, p 3944, 1994.
- [23] T. Mohammed-Brahim, M. Sarret, D. Briand, K. Kis-Sion, L. Haji, O. Bonnaud, D. Louer, A. Hadjaj, “Effect of starting amorphous structure on the solid-phase crystallization of silicon”, *Phil. Mag B.*, vol 76, n°2, p 193, 1997.
- [24] T. Mohammed-Brahim, K. Kis-Sion, D. Briand, M. Sarret, O. Bonnaud, JP. Kleider, C. Longeaud, B. Lambert, “From amorphous to polycrystalline thin films : dependence on annealing time of structural and electronic properties”, *J. of Non-cryst Solids*, p 962, 1998.
- [25] S. D. Brotherton, “Polycrystalline silicon thin film transistors”, *Semicond. Sci. Technol.*, vol 10, p 721, 1995.

- [26] L. Pichon, F. Raoult, O. Bonnaud, H. Sehil, D. Briand, "Conduction behaviour of low temperature ( $\leq 600^{\circ}\text{C}$ ) polysilicon TFTs with an in-situ drain doping level ", *Solid-State Electron.*, vol 38, N°8, p 1515, 1995.
- [27] H. C. De Graff, M. Huybers, J. G. Groot, " Grain boundary states and characteristics of lateral polysilicon diodes", *Solid-State Electron.*, vol 25, p 67, 1982.

Figure caption

Figure 1: Cross section of the two types of the low temperature *unhydrogenated in-situ* doped polysilicon.

- (a) Bilayer-poly-Si TFTs,
- (b) Monolayer-poly-Si TFTs.

Figure 2: Output characteristics of the *unhydrogenated in-situ* doped polysilicon TFTs ( $V_{gs} = 0 - 20$  V, step 4 V), for :

- (a) the bilayer-poly-Si TFT,
- (b) the monolayer-poly-Si TFT.

Figure 3: Transfer characteristics of the two types of the *unhydrogenated in-situ* doped polysilicon TFTs ( $W/L = 60 \mu\text{m} / 25 \mu\text{m}$ ) at:

- (a)  $V_{ds} = 1$  V
- (b)  $V_{ds} = 13$  V.

Figure 4: TEM micrographs of polysilicon layers

- (a) bilayer structure,
- (b) monolayer structure.

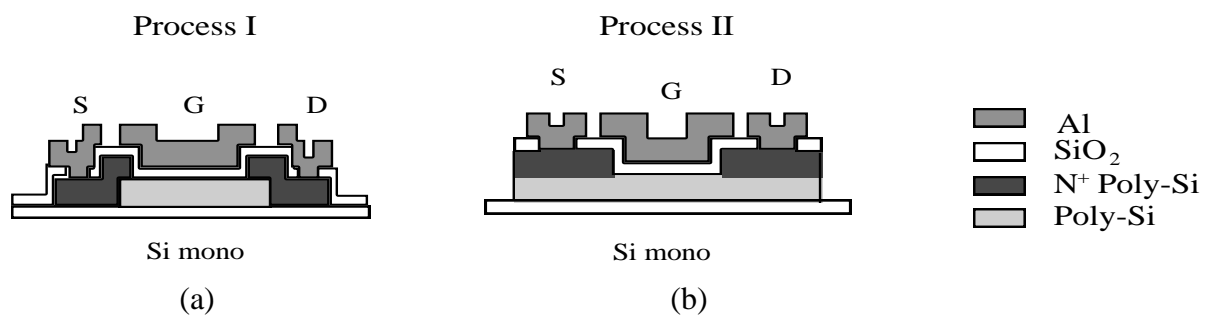
Figure 5: Variations of the Off state current versus the reciprocal temperature at  $V_{ds} = 1$  V, for:

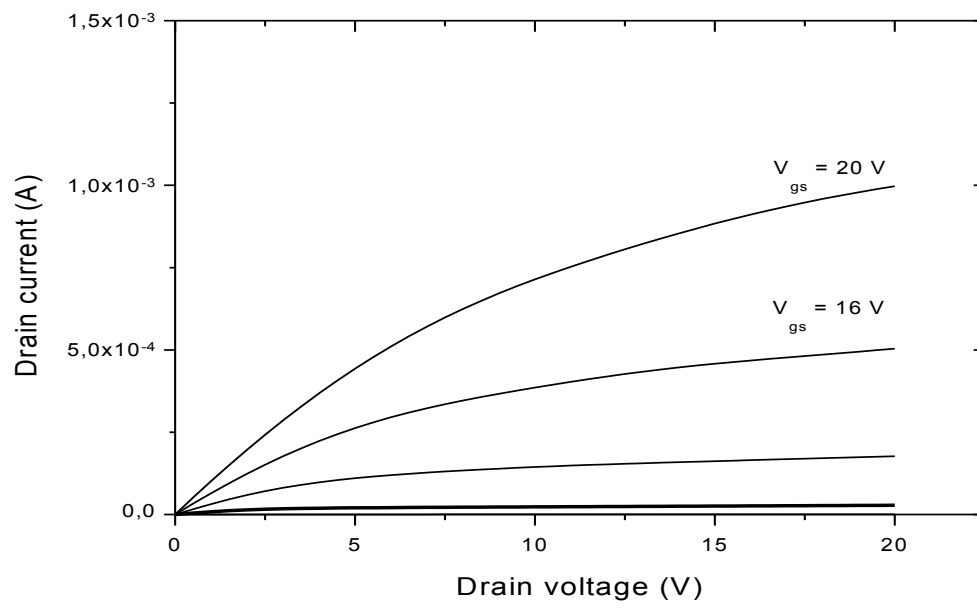
- (a) the bilayer-poly-Si TFTs,
- (b) the monolayer-poly-Si TFTs.

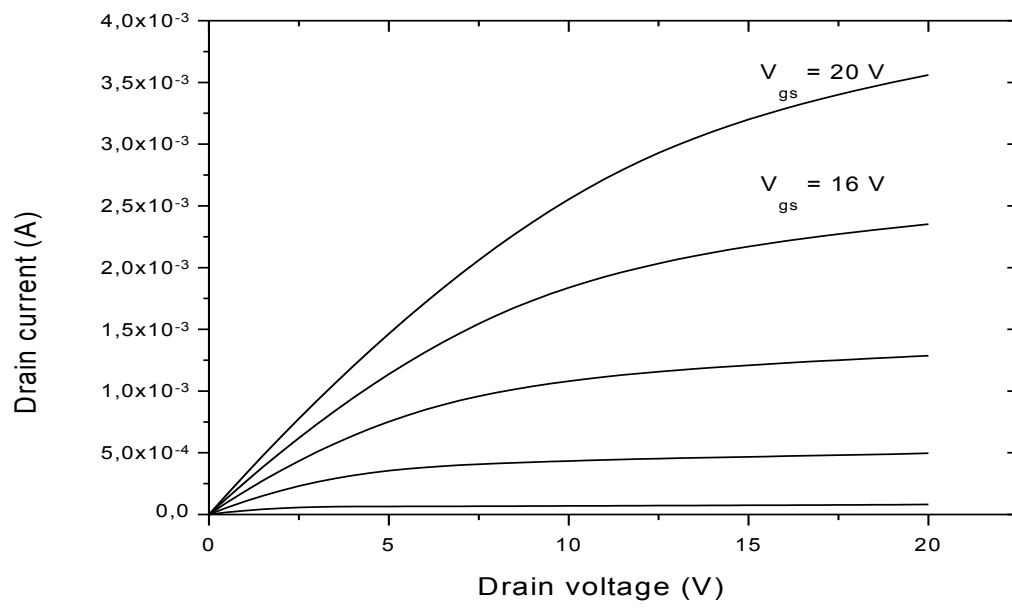
Figure 6: Variations of the Off state current versus the drain voltage rootsquare, for:

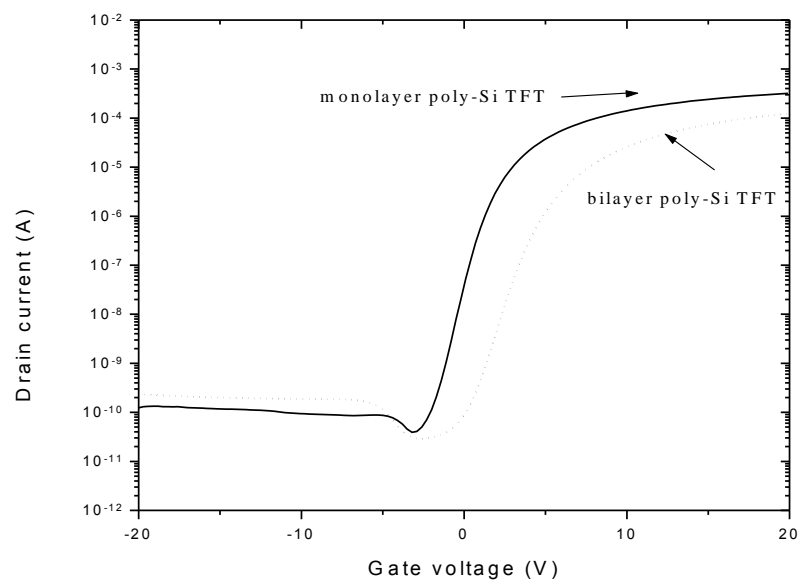
- (a) the bilayer-poly-Si TFTs,
- (b) the monolayer-poly-Si TFTs.

Table 1: Summary of the electrical properties of the two types of the *unhydrogenated in-situ* doped polysilicon TFTs.

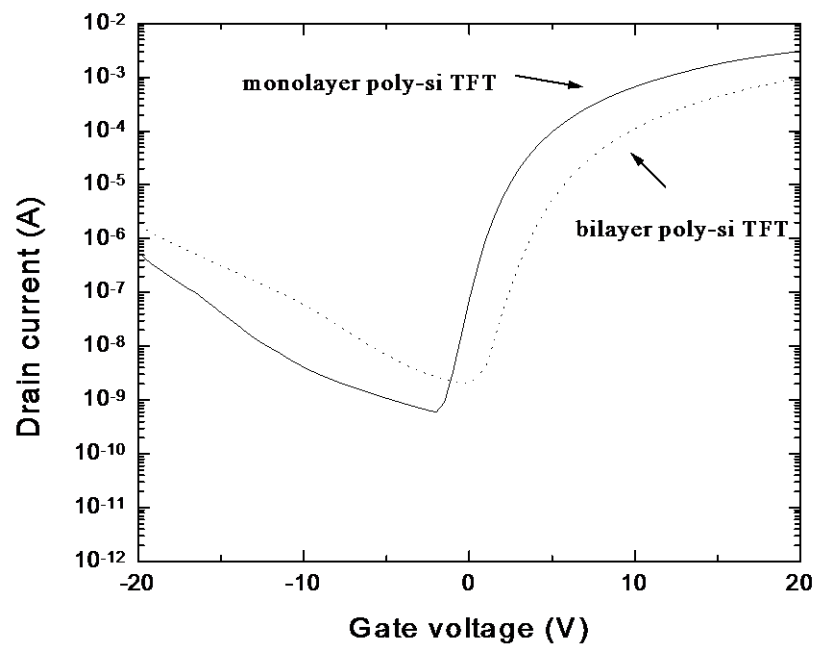


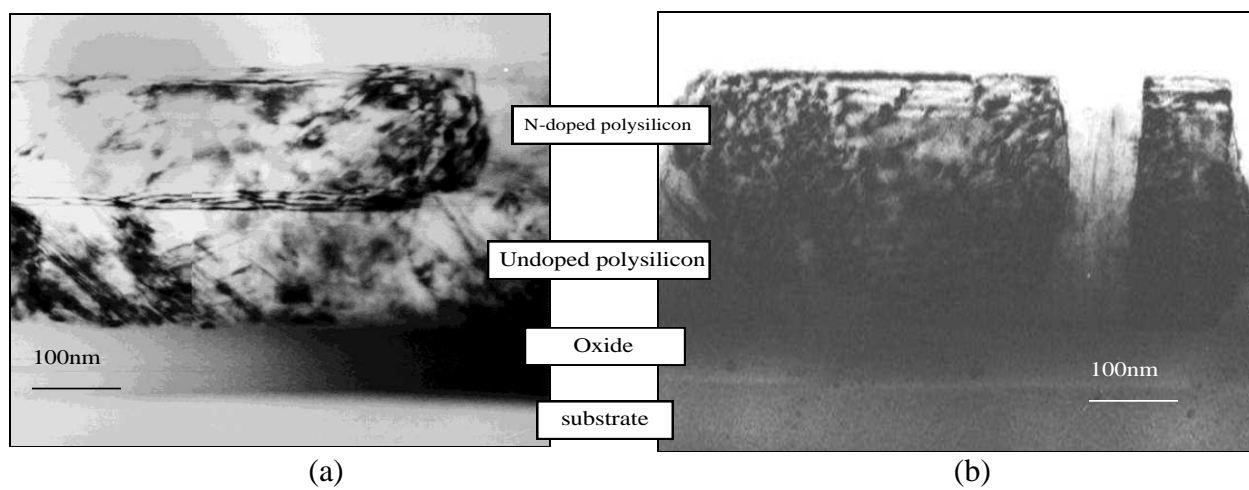


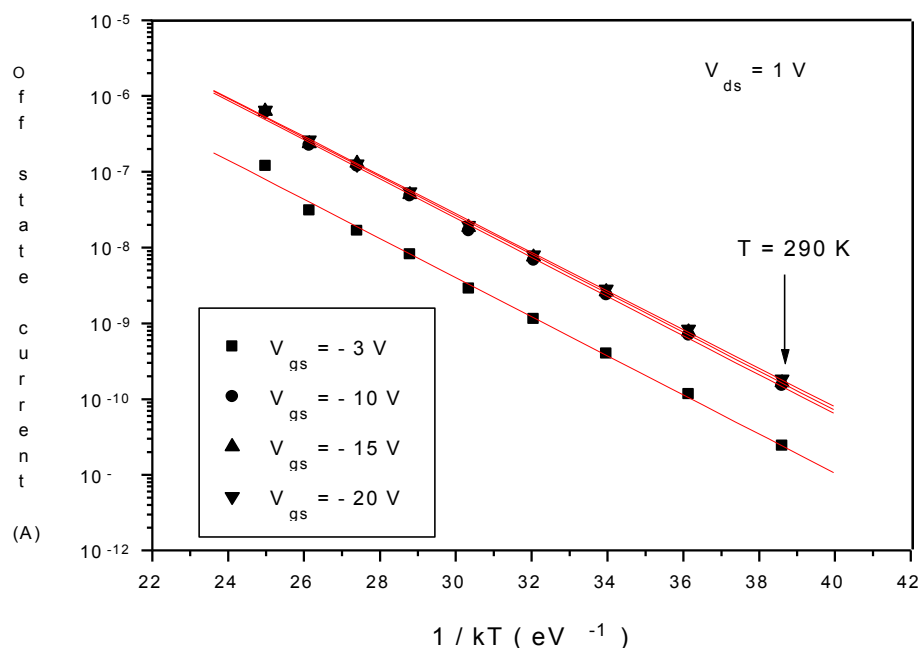


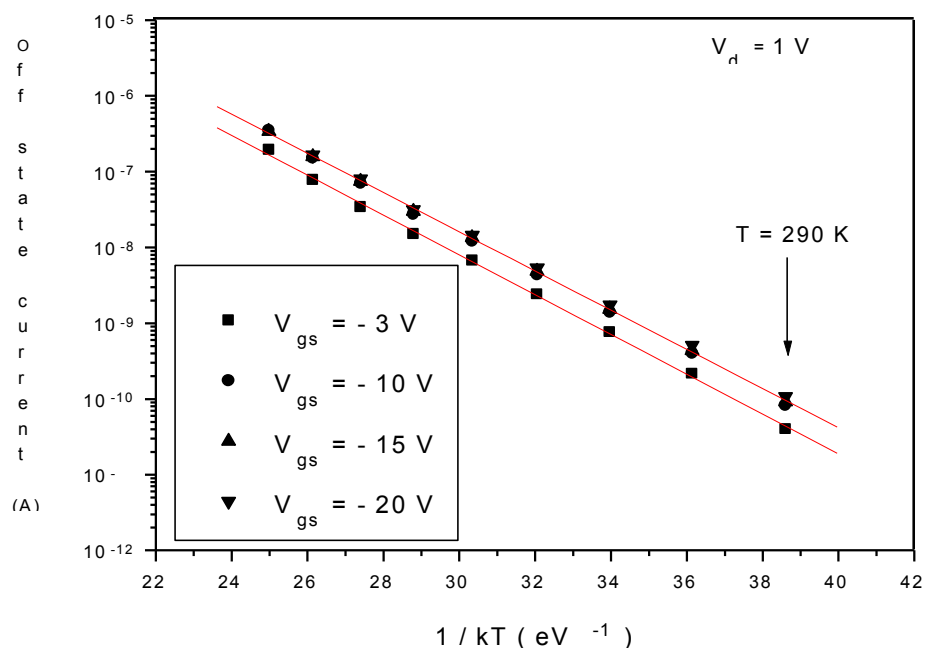


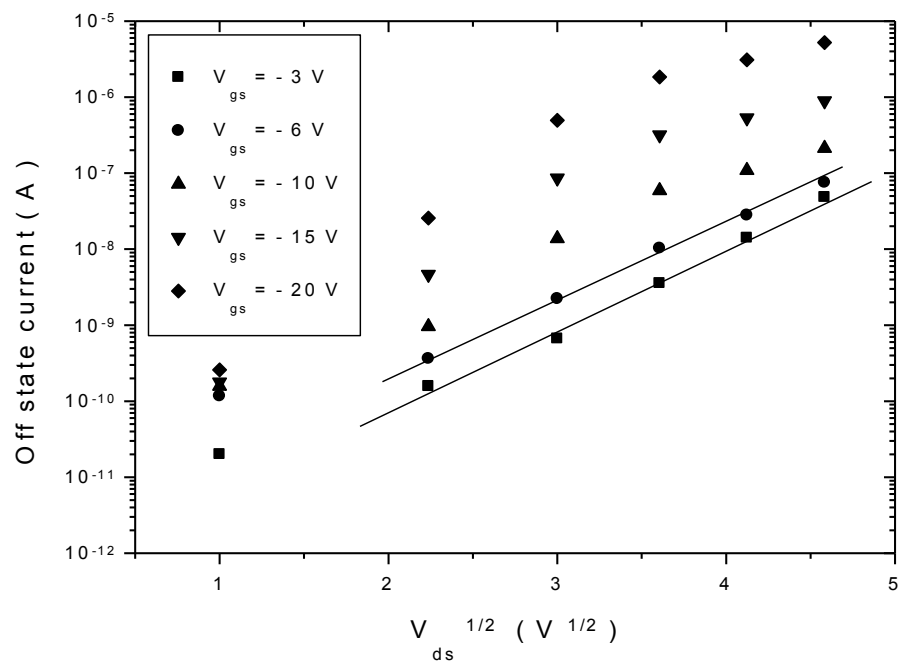


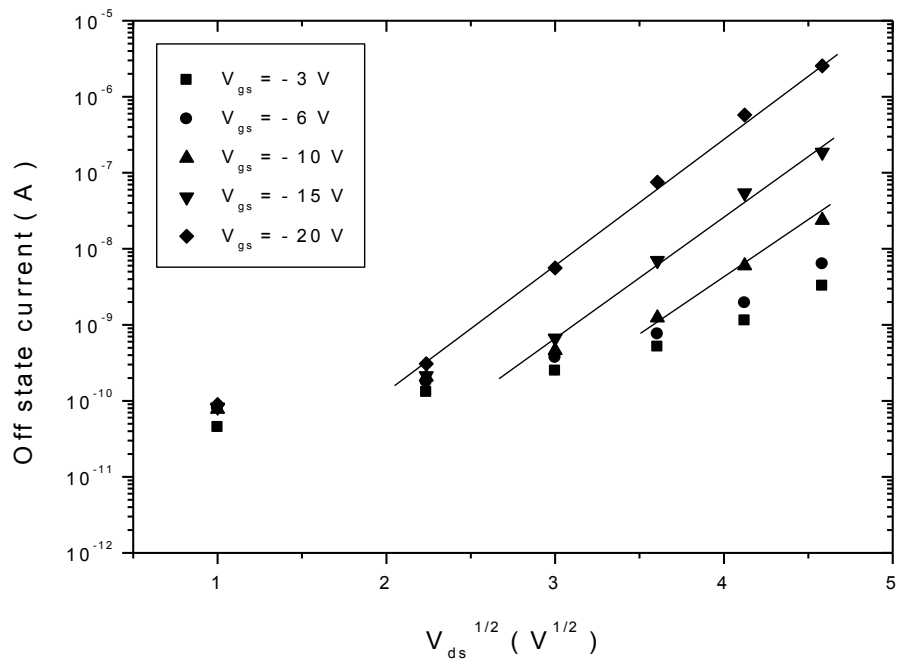












	Threshold voltage ( V )	Subthreshold slope ( V / dec )	Optimum field effect mobility ( $\text{cm}^2 / \text{Vs}$ )	On / Off state current ratio
bilayer poly-si TFT	4	1	63	$6 \times 10^6$
monolayer poly-si TFT	1.2	0.7	100	$10^7$