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Phononic engineering of silicon using “dots on the fly” e-beam lithography and plasma etching

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A B S T R A C T

Nowadays, the interest in reducing the lattice thermal conductivity (k_L), without affecting the electrical one (k_e), represents one of the main objectives for researchers in thermoelectricity. In semiconductors, lattice vibrations contribute about 95% to thermal conductivity. Because phonons and electrons transport operates over markedly different length scales, the power factor ($S^2\sigma$), and consequently the ZT factor of merit, can be significantly improved through the reduction of k_L without sacrificing the electrical conductivity (σ) and the Seebeck coefficient (S).

In this work, we focus on the realization of an efficient e-beam lithography patterning methodology for phononic crystals to investigate thermal conductivity reduction in novel integrated thin film converters. The adopted “dots on the fly” lithography strategy, combined with an appropriate anisotropic plasma etching technique, permits the fabrication of phononic crystal patterns with minimal dimensions, easy layout and writing speeds 3 orders of magnitude larger of those obtained by conventional techniques.

Keywords:

Phononics
E-beam Lithography
Plasma etching
Thermoelectricity

1. Introduction

Over the last years a considerable amount of phononic engineered patterning methodologies have been developed as a consequence of the growing interest towards nanofabrication and development of solid state thermoelectric converters.

The progresses in nanotechnology are presenting exciting possibilities to reduce thermal losses and pattern the active medium in such a way that the phonons spectral distribution and propagation can be tailored.

Phononic crystals (PCs) are the elastic counterpart of the so-called photonic crystals. Following the same line of reasoning, phonons are collective vibrations propagating in a periodic lattice. Engineering PCs is possible to artificially control and induce dispersion properties as frequency band gap, negative refraction or wave guiding [1–3]. These features are the result of Bragg reflection on the artificial lattice.

In such periodic materials, the operating frequency scales as the inverse of the lattice constant (or pitch) a , manifesting the so-called “Zone-folding effect”. Furthermore, phononic band gaps width is controlled by the geometric ratio of constituting materials or filling fraction, the contrast between the physical characteristics of the inclusions and the matrix, as well as their geometry and shape.

Recently, it was advocated that PCs with nanometer scale pitches could efficiently modulate the natural phonon density of states up to the thermal range and thus lead to a reduction of thermal conductivity k [4–7]. The k_L (lattice thermal conductivity) general expression, derived from the Boltzmann transport equation within the single relaxation time approximation, indicates the principal contributions to the heat transport: density of states $g(E)$ (integrated over the whole energy spectrum), phonon group velocity v_g , specific heat c_{ph} and phonon relaxation time τ [8].

$$k_L = \int_0^\infty dE \cdot g(E) \cdot c_{ph} \cdot v_g^2 \cdot \tau$$

There exist several theoretical approaches to treat and solve the previous equation considering different approximations. The most interesting one is the Callaway model [9], which adopts the Debye's approximation, neglecting the phonon dispersion and not differentiating longitudinal and transversal polarization. The model was successively corrected by Holland [10], who considered a different behavior for the two polarization contributions, included phonon dispersions and corrected the relaxation time expressions.

Patterning PCs represents the most interesting approach to reduce k_L and to increase $ZT = S^2\sigma T/\kappa$ for globally enhancing the thermoelectric conversion efficiency η .

Silicon is considered as an attractive material for its advantageously high Seebeck coefficient (thermoelectric power is about

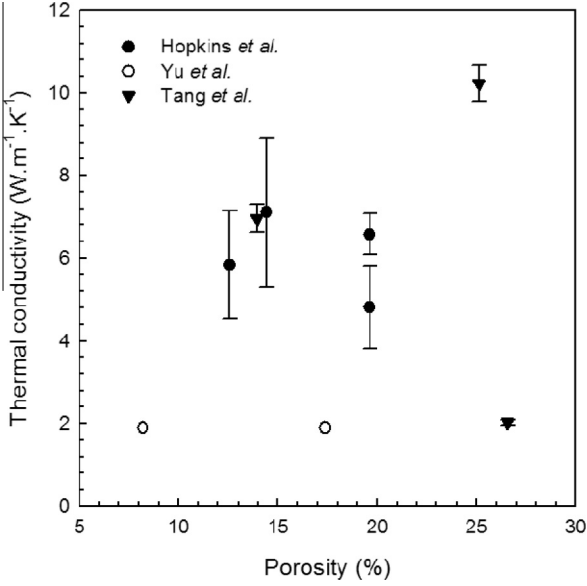


Fig. 1. Thermal conductivity measurements of periodically patterned silicon membranes as a function of the total surface porosity. Results of Yu et al. [12], Tang et al. [13] and Hopkins et al. [14].

400 $\mu\text{V}/\text{K}$ for highly doped p-Si [11]) and tunable electrical conductivity, dependent on doping. The necessity of using a low cost, CMOS compatible and environmentally harmless material to act as active medium for phonons, makes silicon a good candidate for the scope.

Recent experiments conducted by Yu et al. [12], Tang et al. [13] and Hopkins et al. [14] have demonstrated a drastic reduction of k down to 1/100th of the Si bulk value ($149 \text{ W m}^{-1} \text{ K}^{-1}$) in various free-standing periodic nanomesh structures (Fig. 1). A further reduction by one order of magnitude of the thermal conductivity k could be possible by exploiting all the typical effects of phononic engineering (anisotropy, group velocity reduction, phononic band gap), driving to a sensible increase of the silicon thermoelectric efficiency.

The patterning of a phononic crystals structure is the main challenge of the fabrication process. The dimension of the repetition period a (the so-called lattice constant) is established by two parameters: phonon wavelength ($\lambda \sim 2 \text{ nm}$) and its mean free path ($\Lambda \sim 100 \text{ nm}$). To guarantee an efficient reduction of the k coefficient, through the scattering of the acoustic phonons by the periodic array of inclusions, the crystal constant a should be comprised between these two values. Indeed, phonons that account for most of the thermal conductivity have a wavelength in 1–100 nm range. Thus, the lattice constant a is fixed by phonon parameters to values in the range of tenths of nanometers.

In the next sections, the nanofabrication methodology is first described and followed by experimental results before the final conclusive section.

2. Nanofabrication methodology

The main variables to tune during the fabrication process are the lithographic electron-beam (e-beam) impinging dose, the resist minimum resolution and etching parameters (concentration and pressure of reactive gas in the chamber as well as power and time).

The selected resist for PCs patterning is ZEP 520, which assures high resolution and sensitivity, high stability in time and good plasma etch resistance [15].

Even if limited by proximity effects and low throughput, e-beam lithography permits to reach the desired resolutions for dense and

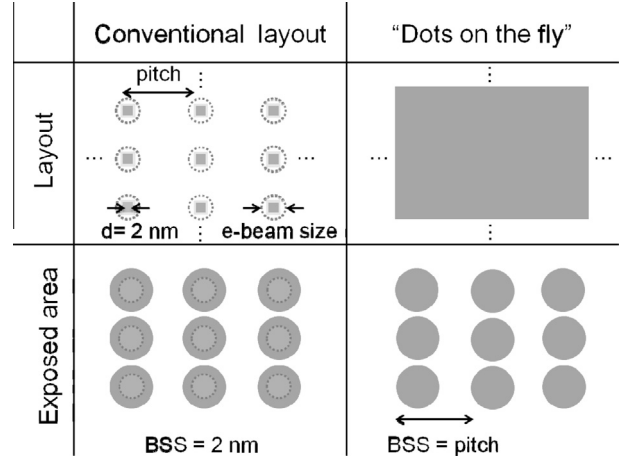


Fig. 2. Comparison between the conventional e-beam writing technique and the “dots on the fly” (BSS = beam step size). For the conventional methodology the pitch is dictated by the distance between the squares designed in the layout (2 nm). Once the electron beam impinges with a high dose, the resist enclosures are featured as in the bottom image. For the “dots on the fly” the square designed is of dimensions of hundreds of microns, but the BSS is increased up to the pitch dimensionality.

small-pitch patterns. To overcome these problems two strategies have been adopted to open identical arrays of cylindrical holes on the silicon surface (Fig. 2). We report here the results related to both and their comparison.

The first methodology relies on overdosing square patterns sized as a minimal ($2 \times 2 \text{ nm}$) beam step size (BSS) of the e-beam equipment Vistec EBPG 5000+. The charge dose ranges from $50000 \mu\text{C}/\text{cm}^2$ to $150000 \mu\text{C}/\text{cm}^2$ using a current of 300 pA. The electron beam size is estimated to 10 nm according to the aperture of $400 \mu\text{m}$. The respective dimensions of the BSS, pitch and beam size are sketched on Fig. 2. The resulting exposed area features circular patterns of diameter directly related to the electron impinging dose.

The second approach, sometimes referred to as “dots-on-the-fly” (DOTF), relies on increasing the BSS up to the desired pitch, using higher currents (10 nA) and lowering the electron dose ($10\text{--}80 \mu\text{C}/\text{cm}^2$) in order to obtain regularly spaced pixels. The electron beam size is almost the same (12 nm) for this current. Following this approach entail a sensible increase of the writing speed as discussed in the following section.

The features transfer, through the 80 nm-thick film of ZEP 520 (positive resist by ZEON Corp.), is realized by Cl_2 physical plasma anisotropic etching (30 sccm, 30 W, 5 mTorr, Plasmalab System 100, Oxford Instruments). The resist is cleaned with a 20 min double bath of PG Remover (MicroChem Corp.), preceded by 10 min of UV light exposition.

3. Results and discussion

Fig. 3 summarizes, for each strategy, the diameter of the obtained cylindrical holes and the respective optimal electron doses as a function of the pitch a , comparing the experimental results with the simulated ones.

An analytical model has been developed to justify the results, confirm the experimental trends and estimate the enclosures optimal diameters. Beam shape, electrons diffusion and pattern periodicity were taken into account to correctly simulate the proximity effects. The electron beam is assimilated to a Gaussian distribution. The model provides useful guidelines to predict holes diameter depending on the parameters previously cited. In such a way it is possible to perform an *a posteriori* analysis starting from the desired characteristics.

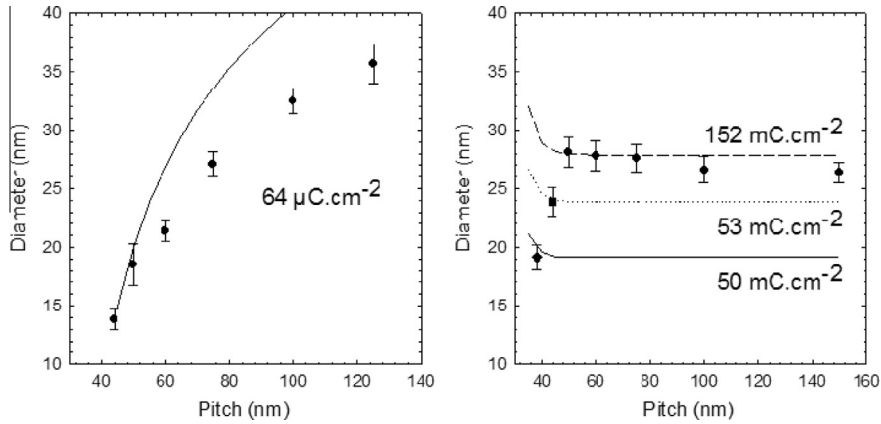


Fig. 3. Diameter of the cylindrical holes as a function of the pitch a for the “dots on the fly” (left) and the conventional methodology (right). The experimental points are compared with the simulated trend.

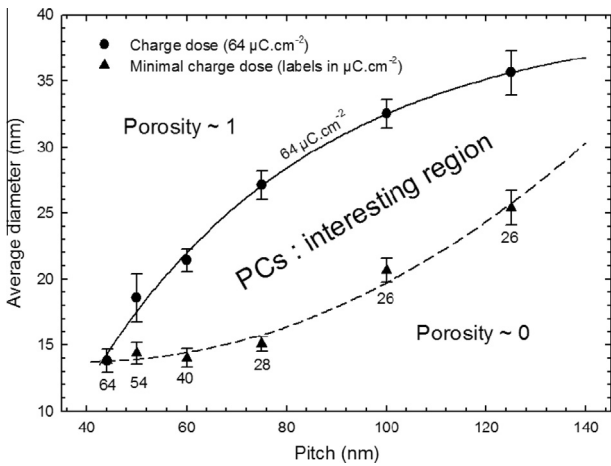


Fig. 4. The “dots on the fly” trends for diameter versus pitch are plotted. The lower curve represents the diameter opened for each pitch by the lowest possible efficient dose. The upper one is plotted for the higher dose ($64 \mu\text{C}/\text{cm}^2$) tested, sufficient to open all the pitches.

In order to have a better insight in the electrons spread in the resist and to individuate an optimal waist parameter, a Monte Carlo simulation with Skeleton™ (Synopsis®) has been performed. The obtained value of 15 nm is consistent with the results for the minimal resolution achievable with the used ZEP resist. Its effect is cumulated differently depending on the methodology investigated, considering the specific machine beam step size (BSS) and the electron-beam impinging dose. The dose accumulation effect is neglected after a distance of 5 neighbors (5 lattice constants a).

A good agreement is reached between the experimental results and the simulated ones, demonstrating the correct modeling of the key parameters determining the holes diameter.

Fig. 3 presents the fittings obtained from experimental data points, corresponding to different doses. It can be observed that, for the conventional method, lower doses over the enlightened area are required to open smaller pitches (38 and 44 nm) to avoid the influence of massive proximity effects, which expose intensively the resist, causing breaks in the patterns or extremely high porosity.

The main advantage presented by DOTF relies on the sensible increase of the surface writing speed to values 3 orders of magnitude larger when compared to the average speeds for the elder method (from $10^{-5} \text{ cm}^2/\text{min}$ up to $10^{-2} \text{ cm}^2/\text{min}$). Such a decrease in writing time is mainly given to the suppression of the electron beam blanking time for the DOTF methodology, entailing a considerable hardware time reduction. The higher current used also contributes to a further reduction of the writing time. Indeed, the dose per pattern only depends on the resist intrinsic contrast curve and is thus equal for both approaches. Using a higher current results in a decrease of the writing time. However, in this case, the gain from current is at best of a factor 33 (10 nA vs. 300 pA) while the total difference between the two methods is of three orders of magnitude.

The potentialities of the DOTF technique have been investigated to explore resolution limits and optimal doses for different pitches.

In Fig. 4, the diameters of holes are plotted as a function of pitches for two different doses: an arbitrary medium-high dose ($64 \mu\text{C}/\text{cm}^2$) and the minimal required dose over the impinging area to open the trenches (which varies depending on the pitch desired). The collected data enlighten the presence of a region in between the experimental curves where the patterns are precisely opened.

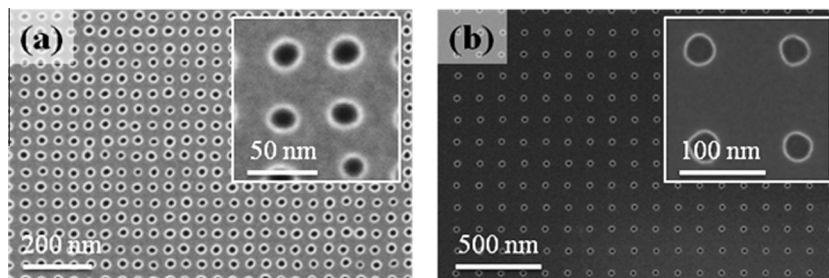


Fig. 5. SEM pictures of the phononic patterns obtained with the “dots-on-the-fly” strategy: (a) pitch 44 nm, diameter $13.8 \pm 0.9 \text{ nm}$ and (b) pitch 125 nm, diameter $25.4 \pm 1.3 \text{ nm}$.

The top curve represents a lower limit for the zone where the proximity effects hinder the fabrication of regular patterns, resulting in values for the porosity tending to the unity. Alternatively, the region below the bottom curve imply values of porosity close to zero, associated to electron doses not sufficient to succeed in opening the features. The resist minimal resolution is reached for feature sizes of about 14 nm, as predicted by Sceleton™ simulations.

Nanomesh uniform patterns were fabricated on (100) Silicon wafer for pitches ranging from 44 nm up to hundreds of nanometers, demonstrating the efficiency of the adopted method (Fig. 5).

4. Conclusions

A robust fabrication process has been developed to pattern silicon phononic crystal structures with the “dots on the fly” technique. An easy layout, a writing time consistently reduced by 3 orders of magnitude with respect to the conventional lithography strategies, an anisotropic Cl₂ etching recipe are decisive advantages of this methodology, contributing to the realization of periodic patterns with pitches down to 40 nm, comparable to the actual state of the art. Therefore, pattern sizes down to 13.8 ± 0.9 nm with a 44 nm pitch and 19.1 ± 1 nm with a 38 nm pitch can be achieved with “dots-on-the fly” and conventional layout respectively, but considering a consistent difference in writing speed.

The use of silicon guarantees compatibility with CMOS technologies and enables the integration of PCs nanopatterned structures in thin film thermoelectric energy converter. Furthermore, the presented process avoids metallic hard masks deposition and thus preserves surface from contamination.

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