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Low temperature noise spectroscopy of p-channel SOI FinFETs

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1. Abstract

The aim of this study is to use the excess low frequency noise versus the temperature in order to characterize the traps in the depleted silicon film of p-channel FinFETs on standard and strained substrates. An important number of identified traps related to boron and carbon can be observed, in particular for the strained substrate devices.

2. Introduction

It is already known that the multi-gate FinFETs are considered as strong contenders for the nano MOS device structures, mainly because the 3D geometry, through a better electrostatic control of the gate over the conduction channel, leads to an improved control of the short-channel effects and provides an enhanced mobility due to the undoped channel [1]. The performance enhancement can be further obtained without adding major process complexity by the use of the strain engineering: biaxial strain (sSOI) or of the uniaxial strain, implemented by contact etch stop layers (CESL) [2]. Furthermore, the integration of SiGe in the source and the drain regions, realized by selective epitaxial growth (SEG), leads to a reduction of the access resistances [3].

One of the methods used for material characterization is provided by the study of the generation–recombination (GR) noise, corresponding to a Lorentzian type of spectra and allowing to do the so-called noise spectroscopy when performed as a function of temperature at fixed biasing [4]. The low frequency noise at different temperatures as a function of the applied gate voltages was already studied for the p-channel FinFET devices in order to investigate the $1/f$ noise [5,6].

This work is focused on the study of the Lorentzian noise contributions on the total low frequency noise versus temperature as a diagnostic tool to characterize the traps located in the depleted Si film (fin) of p-

channel FinFETs devices.

2. Experimental

The investigated devices are p-channel tri-gate FinFETs processed in a 32 nm technology with standard and strained SOI substrates. The gate oxide consists of a high-k dielectric (HfSiON) on top of a 1 nm interfacial SiO₂ resulting in an equivalent oxide thickness (EOT) of 1.5 nm. The metal gate consists of 10 nm TiN covered by 100 nm polysilicon. The devices have a fin width of 25 nm, fin height of 65 nm, 5 fins in parallel. The tested devices are p-channel FinFETs with fixed mask gate length of 1 μ m on standard SOI and strained sSOI substrates combined with compressive uniaxial strain (CESL) using SEG in the drain and source regions.

The low frequency noise measurements were performed directly at wafer-level using a Lakeshore TTP4 prober. The noise measurement set-up allows to bias the devices by choosing the V_{GS} and V_{DS} voltages, and also to measure the total dynamic resistance between drain and source (r_T) and the transconductance (g_m) by applying a small signal at the source and gate nodes, respectively.

3. Low frequency noise spectroscopy

Fig. 1 illustrates an example of the frequency normalized noise spectral density versus the temperature.

Considering white noise, $1/f$ and Lorentzian noise contributions, the total low frequency noise can be perfectly modeled (equation in the inset of Fig. 1). The different noise parameters, in particular the plateau (A_i) and the characteristic frequency (f_{0i}) values of the different Lorentzians contributions, can be clearly identified. According to [7], if the characteristic frequency of a Lorentzian does not change with the applied gate voltage, this Lorentzian can be assigned to a trap located in the depletion film. In this case the characteristic frequency should vary with the temperature [8] (Fig. 2). Only Lorentzians which satisfy

these two conditions were taken into account.

The variation of the characteristic time constant of the Lorentzians ($\tau_i = (2\pi f_{0i})^{-1}$) as a function of the temperature allows to plot an Arrhenius diagram; according to [6] from the slope and the y-intercept of the evolution of $\ln(\tau_i T)$ versus $(k_B T)^{-1}$ one can extract the energy difference between the appropriate band energy and the trap energy (i.e. $\Delta E = E_T - E_V$) and the capture cross section σ_p of the trap, respectively. The physical nature of these traps can be identified by comparing the energy level and the capture cross section of the traps with data in the literature.

The Arrhenius diagram for a standard SOI device is plotted in Fig. 3. Three traps can be clearly identified: one is related to hydrogen (V₂H) [9]; the second one to the interstitial carbon – interstitial oxygen complex (C_iO_i) [10,11], and the last to interstitial boron (B_i) [11,12]. The identified traps and the associated effective trap densities for all the investigated p-channel devices on different strained substrates with can be observed are plotted in the Fig. 4.

The traps related to hydrogen may be present due to hydrogen residues after annealing. All the studied devices have received a boron halo implantation in order to reduce the short channel effects. This may explain the presence of an important number of identified traps related to boron. A contamination due to the SiC liner deposition step can explain the important number of traps related to carbon. The presence of the divacancies (V-P) could be related by the evolution to a stable state of the unstable defects like Frenkel pairs, which could be generated during the implantation.

The estimated surface densities of the identified traps have the same order of magnitude to those identified on n-channels FinFET [13].

4. Conclusions

The analysis of the temperature evolution of the Lorentzian time constant allowed to identify traps in the silicon film. Three traps were identified for devices in a standard substrate. Using strain or SEG leads to an increase in the number of identified traps for a given technology. The nature of the identified traps suggests that the implantation and the SiC liner process are mainly responsible for all the observed traps. The nature of one trap was not identified. However, it can originate from dry-etching or implantation damage.

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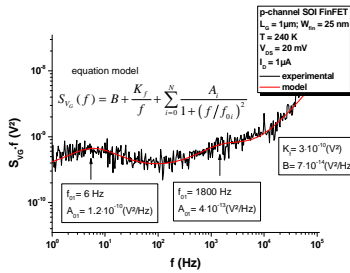


Fig. 1: Modelling of a noise spectrum

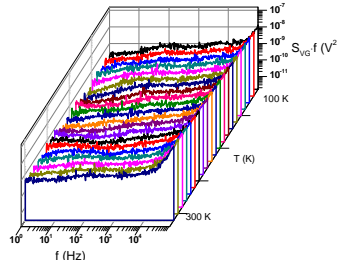


Fig. 2: $S_{VG} \cdot f$ versus all investigated temperatures

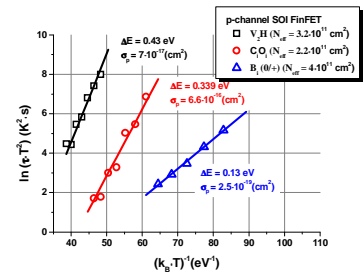
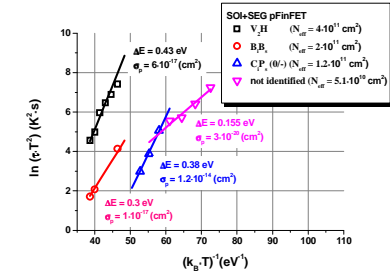
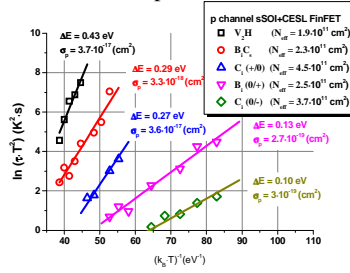


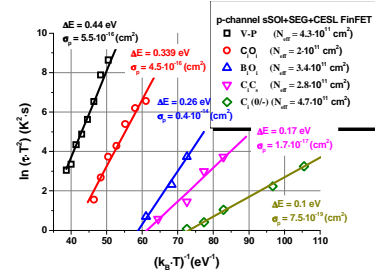
Fig. 3: Arrhenius plot for a standard device on SOI substrate



a)



b)



c)

Fig. 4: Arrhenius plot for a) SOI +SEG; b) sSOI+CESL; c) sSOI+CESL+SEG