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DC and Noise Performances of SOI FinFET at Very Low Temperature.

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1. Abstract

In this work, DC and noise measurements in strained and unstrained SOI FinFET were performed in order to evaluate the device performances at cryogenic temperatures (10 K). The main electrical parameters (threshold voltage, subthreshold swing, mobility, etc...) are investigated. The study of the low frequency noise clearly shows that the $1/f$ noise is governed by the carrier number fluctuations even at cryogenic temperatures for p-channel devices.

2. Introduction

It is well known that the temperature affects device performances and parameters especially mobility, subthreshold characteristics, threshold voltage... [1]. Number of papers have been published on static and low noise operation in strained and unstrained FinFET transistors [2] depending on the temperature but usually limited to an interval of 80 K – 300 K or higher [3-7]. However, up to now, the static performance and noise behavior in multi-gate FinFET has not investigated at very low temperature. The aim of this work is the study the DC and low frequency noise behaviors at cryogenic temperature (10 K) in standard and strained SOI FinFETs.

3. Experimental

The tested devices were n and p-channel multigate FinFETs. They have been processed in 32nm technologies on standard and strained SOI substrates. The biaxial global strain, where the stress is introduced across the whole wafer by epitaxial growth of a SiGe “buffer layer” and the uniaxial local strain, based on the use of strain across the gate stack, referred to as contact etch stop layers (CESL) will give a stress along the channel and boost up the carrier mobility. The integration of SiGe in the source and the drain regions, realized by selective epitaxial growth (SEG), leads to a reduction of the access resistances and an increase of mobility. The gate oxide consists in a high-k dielectric (HfSiON) on top of a 1nm interfacial SiO₂, resulting in an equivalent oxide thickness (EOT) of 1.5 nm.

Static measurements in linear and saturation regime of operation were performed directly on wafer-level using a “Lakeshore TTP4” probe for all investigated temperatures for a standard device (SOI) and a strained one (sSOI+SEG+CESL) with a fin-width of 25 nm, 5 fins in parallel and a gate length varying from 0.13 to 1 μ m. The low frequency noise measurements were focused on p-FinFET for two physical gate lengths (110 nm and 910 nm). This work will present only results from linear regime where the devices were biased with an applied drain voltage of $|V_{DS}| = 20$ mV. The noise measurements were performed for different applied gate voltages. The DC electrical parameters were extracted using the Y methodology, which was adapted for the very low temperatures [8]. From noise measurements, the $1/f$ noise contribution on the total noise versus the applied gate overdrive V_{GT} was extracted and modeled using the models described in [9-11].

4. Results and discussion

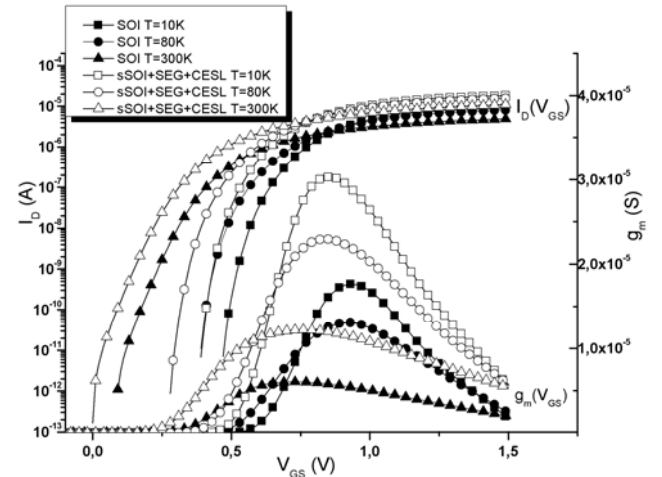


Fig. 1: Typical $I_D(V_{GS})$ and $g_m(V_{GS})$ versus temperature characteristics for standard and strained nFinFET ($L=1 \mu\text{m}$).

Fig. 1 shows an example of the drain current $I_D(V_{GS})$ and transconductance $g_m(V_{GS})$ characteristics at 10 K, 80 K and 300 K for a standard and strained nFinFET. If $g_{m\text{max}}$ always increases when the temperature becomes very low, the extracted mobility, which is still important

at 80 K (2 to 3 times higher than at 300 K) decreases at 10 K (but still keep 20-80% increase compared to 300 K). The reduction of the phonon scattering may explain the increase of the mobility with the temperature decrease, while at very low temperatures the degradation of the mobility could be related to surface roughness scattering. At 80 K and at 300 K, the values of the extracted subthreshold slope S are close to ideal values, whereas at 10 K a deviation is observed ($S \geq 8$ mV/dec at 10 K for an ideal value of 2 mV/dec). This could be related to an increase of the interface states at the band edge at low temperatures.

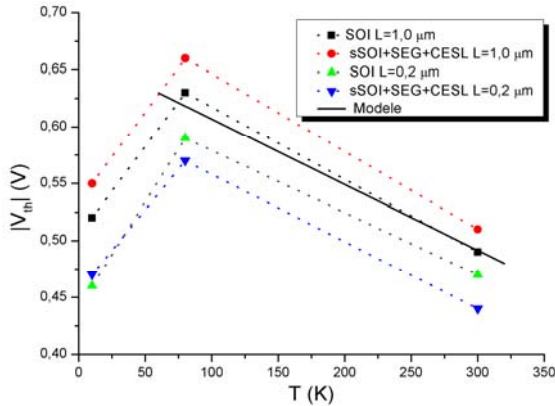


Fig. 2: The extracted threshold voltage V_{th} for standard and strained pFinFET at 10 K, 80 K and 300 K.

In Fig. 2 are plotted the extracted threshold voltage for 1 μ m gate length for p-channel unstrained and strained FinFET. In solid line, is plotted the expected tendency of the threshold voltage increase with the temperature decrease for these devices (modeled with a rate of about -0.57mV/K [12]). Improvement of the threshold voltage is observed for all the studied devices at very low temperature operation where their values are close from values which were found at room temperature. This behavior could be related with the temperature behavior of the Fermi level at very low temperatures. One can observe also that for p-FinFET, strain slightly increase the threshold voltage for large lengths and decrease it for the shortest ones. On the other side, for nFinFETs, V_{th} is always reduced by the strain for all lengths especially at low temperatures.

An example of $K_f(V_{GT})$ the frequency normalized gate voltage spectral density at 1 Hz versus V_{GT} at 10 K and 300 K is shown in figure 3 for a p-channel standard structure.

At room temperature, the carrier fluctuations due to carriers trapping/detrapping in the oxide layer dominate the 1/f noise. The increase of the noise from weak to strong inversion can be modeled (solid line in Fig. 3) by the carrier number fluctuation correlated to mobility fluctuations ($\Delta N + \Delta \mu$) and in strong inversion by the parasitic access resistance (r_{access}) noise contribution.

At 10 K, a reduction of the 1/f noise level at 1 Hz is observed for all studied devices compared to room temperature. The 1/f noise level is found to be independent of the applied gate voltage overdrive in weak inversion. This suggests that the carrier number

fluctuations (ΔN) dominate. This trend was observed for all studied devices. The contribution of the carrier number fluctuation correlated to mobility fluctuation disappears at 10 K. The increase of the noise in strong inversion can be related to the contribution of the parasitic access resistance on the total noise. This behavior was modeled by the dashed line in Fig. 3. One can notice that the access resistance noise contribution on the total noise is reduced with the temperature decrease.

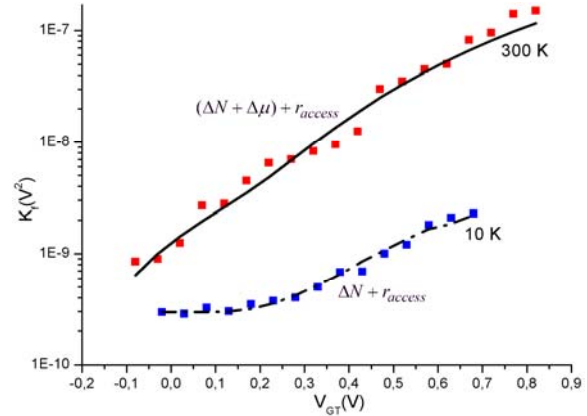


Fig. 3: Frequency normalized gate voltage 1/f noise level versus the applied gate overdrive at 10 K and 300 K.

5. Conclusion

In this work, DC and noise measurements on SOI FinFET at 3 temperatures (10, 80 and 300 K) have been performed. The reduction of the mobility at very low temperature (compared to 80 K operation) may be compensated by the decrease of the threshold voltage and the subthreshold voltage improvement.

In weak inversion, the carrier number fluctuations dominate the 1/f noise from room temperature down to 10 K operation for the p-channel FinFETs. But at 10 K there is no contribution of the carrier number correlated to mobility fluctuations. In strong inversion, the contribution of the access resistances is strongly reduced when the temperature decrease.

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