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Keywords:
UTBOX
High-k dielectric
Flicker noise
Low frequency noise spectroscopy
Traps in Si film

A B S T R A C T

In this paper, UTBOX nMOSFETs with different gate dielectrics have been studied based on their low-frequency noise (LFN) performance. Since LFN measurements have been successfully used as a characterization tool for determining the quality of the films, here, we have investigated the dielectric films used in state-of-the-art UTBOX devices in order to evaluate their performance and to identify the type of traps possibly introduced during the device processing.

High-k gate dielectric devices have shown predominantly $1/f$ noise with a two-order of magnitude higher value than the conventional SiO_2 ones which, consequently, results in higher density of traps in those devices. The carrier number fluctuations dominate the $1/f$ noise for both front and back interfaces. Due to the thin silicon film thickness there is a strong electrostatic coupling between front and back interfaces that interferes in the noise results as well as in transistor parameters. A contribution of the back interface noise source of about 14% on the measured noise in the front channel conduction was found, while the contribution of the front interface noise source is about 22% on the measured noise in the back channel conduction.

The generation–recombination (GR) noise performed at different temperatures has enabled the identification of 6 types of traps and 2 unknown ones, being originated from the dry-etching or implantation damage.

1. Introduction

The advent of the 16 nm technology node and below has demanded the appearance of new devices based on different structures, materials and designs in order to achieve the performance specifications. In these terms, there is a growing interest in the fully depleted (FD) ultra-thin buried oxide (UTBOX) technology because of its superior characteristics reported in literature [1,2]. The very thin BOX provides an extra control of the short channel effects due to the higher electrostatic coupling between gate and channel. Moreover, the threshold voltage can also be controlled by applying a back bias voltage, becoming more significant if combined with a ground plane (GP) implantation that suppress the depletion under the BOX [3–6]. Besides it has been reported that a BOX thickness of around 10 nm is necessary to avoid high bias values at the back channel [7]. Another interesting aspect about FD UTBOX technology is the non-intentionally doped channel that offers several advantages in terms of suppression of dopant-related variability [8]. Lately, these devices have been applied as one-transistor dynamic random-access memory (1T-DRAM) cells [9,10] where one of the main concerns is related to the charge retention time that is affected by defects present in the silicon and the dielectric layers. Because of that, a good process control to avoid the occurrence of defect-related carrier generation–recombination (GR) is required [11,12]. One way to characterize the defects present in the devices is based on the low frequency noise (LFN) analysis which is a non-destructive characterization tool that gives information about the quality of

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the gate oxide, the silicon/dielectric interface and Si film. Measurements at different temperatures allow to perform a noise spectroscopy that provides information on the nature of the traps [8,13]. It is well known that high-k dielectrics have been widely applied in state-of-the-art devices. Although they allow the gate leakage decrease compared to the thin silicon dioxide (SiO_2), it is also known that high-k materials suffer from increased noise behaviour due to the higher number of traps and a poorer interface quality [14–16]. Consequently, understanding the LFN in these devices is an important way to assess the device quality and to optimize the processing steps for less defects.

The aim of this work is to investigate the low frequency excess noise sources (1/*f* and Lorentzian spectra) versus temperature as a diagnostic tool in order to characterize the traps present at the front (and back) gate oxide/Si film interface and in the depletion area (Si film) of these advanced n-channel UTBOX devices, comparing different gate dielectrics.

2. Device description and methodology

The tested devices were processed at imec in 300 mm fully depleted (FD) ultra-thin buried oxide (UTBOX) wafers. In the first section, the measured devices present a BOX thickness of 18 nm and a silicon thickness (t_{Si}) of 6 nm (after the device processing). Two wafers were compared, differing from each other only by the gate stack: a conventional silicon dielectric (5 nm thermal SiO_2 + Poly) and a high-k one (1.5 nm ISSG + 4.2 nm HfSiO + 5 nm TiN + 2 nm Si-cap, resulting in an EOT = 2.6 nm). Different dies are measured in order to check the variability along the wafer but the device dimensions are kept the same, 70 nm channel length and 1 μm channel width. More process details can be found in [17]. The noise measurements have been performed using the BTA system controlled by the NoisePro software from ProPlus Design Solutions, Inc. while the DC characterization is performed on the same devices using the HP-Agilent 4156C system. The devices have been measured at room temperature along the vertical diameter of the wafer and in linear operation (drain voltage V_{DS} = 0.05 V), with the front (V_{GS}) or back gate voltage (V_{GB}) stepped from weak to strong inversion. The front-channel noise was measured with V_{GB} = 0 V and the back-channel one at V_{GS} = 0 V. The noise spectra of the studied devices present pure 1/*f* noise in the low frequency range; this allows to estimate the 1/*f* noise level at fixed frequency of 25 Hz.

In the second section, the UTBOX devices are fabricated using the same technology, but are issued from a different lot than those proposed for the study in the first section. Different gate lengths (from 55 nm up to 935 nm) have been analysed with a fixed gate width (1 μm), the equivalent gate oxide thickness (EOT) of the high-k dielectric (1.5 nm SiO_2 + 2.5 nm HfSiO with 60% Hf) is 2.6 nm and the BOX thickness about 10 nm. Further processing details are presented in [18]. The low frequency noise measurements were performed directly on wafer-level using a "Lakeshore TTP4" prober. The noise measurements have been made using two low noise DC voltage sources which allow biasing the devices by choosing the V_{GS} and V_{DS} voltages, an *I*–*V* converter and a low noise voltage amplifier. An HP3562 spectral analyser was used to obtain the noise spectral density between 10 Hz up to 100 kHz. The measuring set-up allows also to measure the total dynamic resistance between drain and source r_T and the transconductance g_m over the same frequency range by applying a small signal at the source and gate nodes, respectively. Noise is calculated at the input of the device by dividing the measured noise voltage by the square of the measured voltage gain between the gate and the output and this for different applied gate voltages avoiding the set-up bandwidth. The noise spectra of the studied devices contain GR contributions even for frequencies lower than 100 Hz. In order to properly extract the noise parameters, in particular the Lorentzian and 1/*f* contributions, the frequency dependence of the different contributions that can occur in the total noise spectral density at the input of the devices was considered. At room temperature, the front (back) gate noise was investigated as a function of the front (back) gate voltage $V_{GS}(V_{BS})$ for a fixed V_{BS} = 0*V* (V_{GS} = 0*V*). The coupling between the two interfaces was taken into account. The front gate noise measurements were performed from room temperature down to 80 K (with 10 K step), keeping the drain current constant at I_D = 9 μA, in order to investigate the traps present in the device structures.

3. Experimental analysis

3.1. Low frequency noise (LFN) in SiO_2 and HfSiO gate dielectrics

In this section, hafnium silicate (HfSiO) gate dielectric devices are confronted to the conventional silicon dioxide (SiO_2) ones in order to evaluate the low frequency noise performance and to establish a correlation with the main transistor parameters.

Initially, the threshold voltage (V_{th}) and the low-field electron mobility (μ_n) are analysed in both types of splits. Table 1 shows these values found for six samples extracted from different positions along the wafer diameter and based on the Y-function method [19]. Front and back channels are analysed due to the strong coupling between the two interfaces. The V_{th} variation is due to local silicon film thickness variation combined with possibly different effective channel lengths along the wafers [17]. One can also observe that the mobility values scatter around the average point of 60.7 cm^2/V s for the SiO_2 split and 37.8 cm^2/V s for the high-k one, underlining that conventional SiO_2 devices present higher electron mobility with an increase of around 40%. Moreover, the back-channel mobility of the high-k wafer is also better than the front side of the same devices while the SiO_2 split presents a poorer back performance mainly due to the thickening of the BOX during the shallow trench isolation (STI) processing.

No correlation has been found between the front and back channels threshold voltage unlike the mobility values as presented in Fig. 1. A linear trend can be noticed mainly for high-k transistors which mean that each interface affects the other due to the coupling between them.

The current-noise spectral density (S_I) for the front and back-channels are presented in Figs. 2 and 3, respectively, where the samples of each dielectric at the same overdrive voltage ($V_{GT} = V_{GS} - V_{th}$; and $V_{GT} \sim 0$ V) are compared. One can notice that the noise level is approximately the same in both front and back-channels. This can be associated to the interference of one channel on the other. As the back-channel consists of thermal-SiO_2 similar values in both types of wafers are expected. However, high-k devices present a back-channel noise level almost two orders of magnitude higher than the conventional dielectric samples. Pure 1/*f* behaviour can be observed for all devices for frequencies lower than 100 Hz. The occurrence of generation–recombination (GR) noise appears in the back-channel analysis of the two SiO_2 samples. This GR noise is

Table 1
Average and range of variation of V_{th} and μ_n obtained for the two studied wafers.

		Threshold voltage (V)		Low-field mobility (cm^2/V s)	
		Average	Range	Average	Range
SiO_2	Front	0.15	0.09–0.18	60.7	33.3–70.0
	Back	0.34	0.32–0.36	49.9	27.2–53.6
HfSiO	Front	0.81	0.79–0.83	37.8	21.0–45.8
	Back	4.86	4.77–4.99	62.5	47.3–84.5

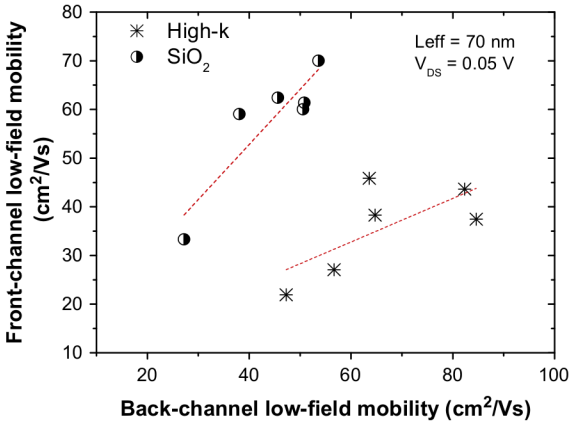

Fig. 1. Front versus back-channel mobility for the two splits. A linear tendency is observed and demonstrates a correlation between front and back mobility.

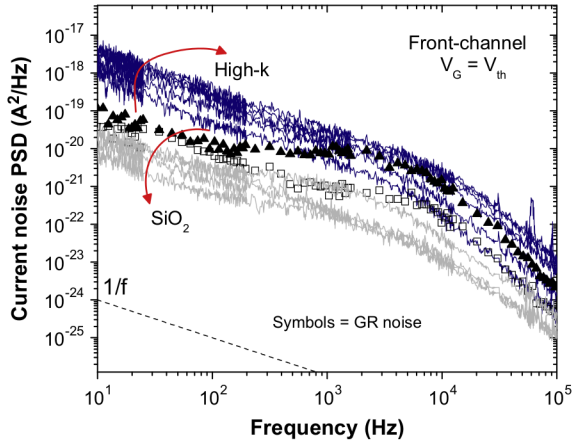

Fig. 2. Current noise PSD versus frequency for high-k and SiO_2 wafers for the front-channel. GR noise contribution is represented by square and triangle symbols.

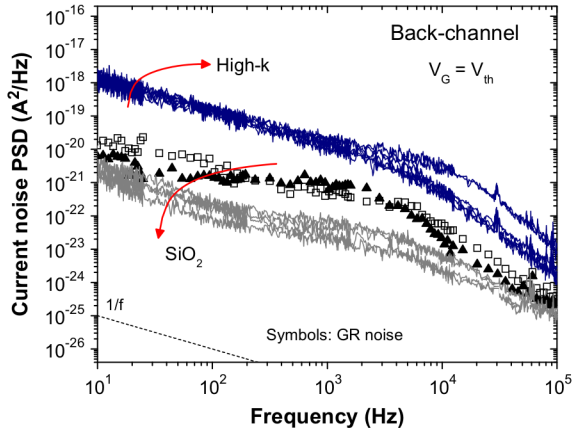

Fig. 3. Current noise PSD versus frequency for high-k and SiO_2 wafers for the back-channel. GR noise contribution is represented by square and triangle symbols.

induced by deep energy levels in the silicon film, as shown by symbols in the spectra of Fig. 2 and Fig. 3.

The $1/f$ noise levels were estimated at fixed frequency (i.e. 25 Hz). According to the normalized spectral density (S_I/I_{DS}^2), represented by Fig. 4 (front-channel) and Fig. 5 (back-channel), a plateau can be observed in weak inversion followed by a dropping off at the threshold voltage and in strong inversion, indicating that the LF is due to carrier number fluctuations [16] (see Fig. 5).

Fig. 6 presents the input-referred noise (S_{v_G}) PSD for the front (a) and back (b)-channels, comparing the two dielectrics. As expected, the use of a high-k dielectric induces an increase of the trap density in the oxide layers and results in a degraded interface profile [15]. The S_{v_G} values are about one order of magnitude higher for high-k devices at both interfaces (front and back-channels). Two points have been highlighted to indicate the occurrence of GR noise in the SiO_2 split. Except by these points the spectra of the samples are predominantly $1/f^{\gamma}$like ($\gamma \sim 1$) which means the noise is related to the oxide traps, thus an average S_{v_G} values can be obtained that will be used later to estimate the interface trap density. The front-channel average values correspond to $2.5 \times 10^{-9}\,V^2/Hz$ and $1.5 \times 10^{-10}\,V^2/Hz$ while the back-channel presents $2.3 \times 10^{-8}\,V^2/Hz$ and $1.0 \times 10s^{-9}\,V^2/Hz$ for the high-k and SiO_2 wafers, respectively.

The correlation between back and front-channel S_{v_G} is presented in Fig. 7. Except for two devices where GR noise dominates, a correlation between noise at the back and front channel is observed as already mentioned in the mobility analysis. However, the correlation is less clear and should be validated by other experiments.

Based on the average values of the $1/f$ noise levels, the oxide trap density (N_{ot}) can be determined according to Eq. (1).

$$S_{V_{FB}} = \frac{q^2 kTN_{ot}}{WLfC_{ox}^2\alpha} \tag{1}$$

with q the elementary charge, kT is the thermal voltage, f is the frequency (25 Hz), $\alpha = 10^8\ cm^{-1}$ is the tunnelling attenuation coefficient in SiO_2 and C_{ox} is the oxide capacitance per unit of area.

As a result, the density of traps for high-k devices are more than two orders of magnitude higher compared to the SiO_2 ones. The estimated values are about 7.1×10^{19} and $2.2 \times 10^{18}\ cm^{-3}\ eV^{-1}$ for front and back channels, respectively, while the SiO_2 split presents 1.7×10^{17} and $9.5 \times 10^{16}\ cm^{-3}\ eV^{-1}$ for front and back channels, respectively.

Fig. 8 shows the correlation between input-referred noise PSD and low-field mobility for the front-channel. Although there is no correlation between these parameters when the back-channel is analysed, the front channel shows that a higher mobility is associated with a lower noise level, i.e., a linear behaviour mainly for the high-k dielectric nMOSFETs. Such behaviour has been already reported in [20] and can be explained based on the Coulomb scattering of the charged oxide traps according to $1/\mu_{sc} \sim \alpha_{sc} q N_{ot}$, with N_{ot} in cm^{-2}. Considering the average values of the front-channel μ_N and N_{ot}, an energy interval of $4kT$ (~0.1 eV) and a tunnelling depth of ~2 nm, the scattering parameter, α_{sc}, is 1.2×10^6 V s/C and 2.3×10^7 V s/C for front and back channels of the high-k devices while the SiO_2 wafer presents α_{sc} equal to 3×10^8 V s/C for front and 6.8×10^8 V s/C for the back channel.

3.2. Excess noise study in UTBOX devices with HfSiO gate dielectrics

Typical frequency normalized front interface noise spectral density is illustrated in Fig. 9. It can be observed that the noise behaviour in the studied devices can contain G–R contributions, even for frequencies lower than 100 Hz. In order to perform the low frequency noise spectroscopy, one should estimate the plateau value and the characteristic frequency of each Lorentzian contribution. Moreover, the estimation of the $1/f$ noise contribution in the total noise by taking into account the noise at fixed frequency (i.e. 25 Hz) could lead to overestimations because of the G–R contributions. One issue method is to take into account the frequency dependence of the different contributions on the total noise

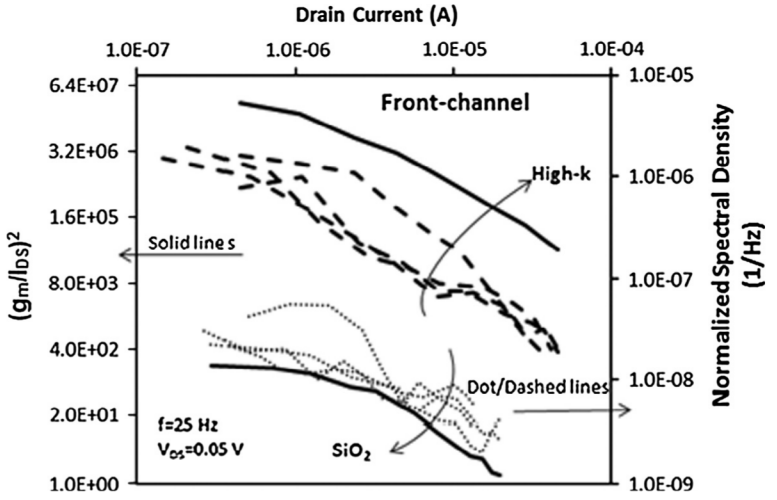

Fig. 4. The evolution of the front-channel normalized spectral density of the drain current (S_I/I_{DS}^2) and $(g_m/I_{DS})^2$ versus the drain current suggests that the carrier fluctuations dominate in the studied devices).

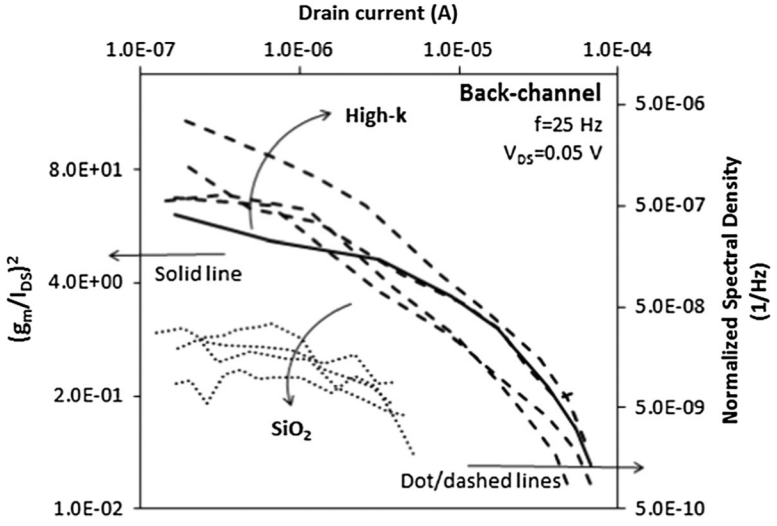

Fig. 5. The evolution of the back-channel normalized spectral density of the drain current (S_I/I_{DS}^2) and $(g_m/I_{DS})^2$ versus the drain current. In the back-channel case, both g_m/I_{DS}^2 levels are the same for SiO_2 and high-k samples.

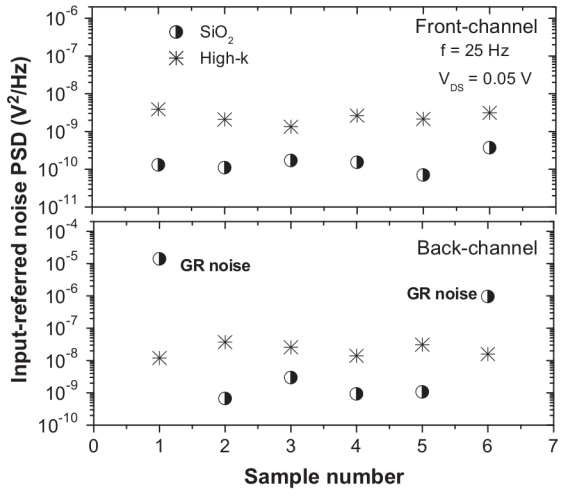

Fig. 6. Input-referred noise PSD for front and back channels and different samples at 25 Hz.

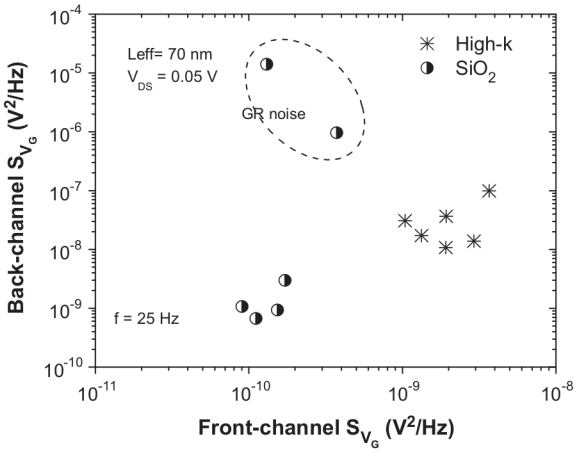

Fig. 7. Correlation between back-channel S_{v_G} and front-channel S_{v_G} at 25 Hz.

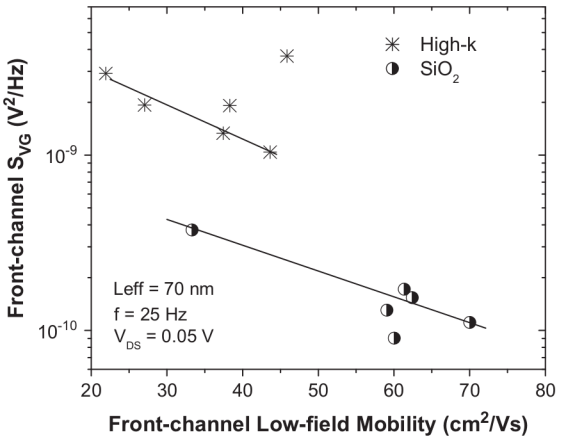

Fig. 8. Correlation of the input-referred noise (S_{v_G}) and the front-channel low-field mobility for both splits. Solid lines present the tendency.

spectral density at the input of a MOS transistor, which can be expressed as in the following equation [21]:

$$S_{V_G}(f) = B + \frac{K_f}{f^{\gamma}} + \sum_{i=0}^{N} \frac{A_i}{1 + \left(\frac{f}{f_{0i}}\right)^2}. \quad (2)$$

where B is related to the white noise level, K_f/f^{γ} presents the flicker noise (the frequency exponent γ may deviate from 1 if the trap density is not uniform in depth), and the third term of the equation presents a sum of Lorentzian components, with A_i the plateau value and f_{0i} the characteristic frequency. Assuming contributions of these three noise sources, the observed noise spectra can be perfectly modelled by Eq. (2) as shown in Fig. 9. By using plots in which the frequency normalized noise spectral density versus frequency is represented, one can identify the different noise parameters. This technique has been successfully applied for the noise parameters extraction in advanced MOSFET devices [22–23].

3.2.1. 1/f noise at room temperature

The extracted 1/*f* noise levels for the front interface is noted K_{f1} and K_{f2} for the back interface. In the case of 1/*f* noise is governed by the carrier number fluctuations, a more in-deep analysis can be made, taking into account the coupling effect on the front and back-gate input gate voltage 1/*f* noise. For fully depleted SOI devices, in [24,25] is proposed an analytical model, based on [26] that takes into account the coupling expressions derived in [27].

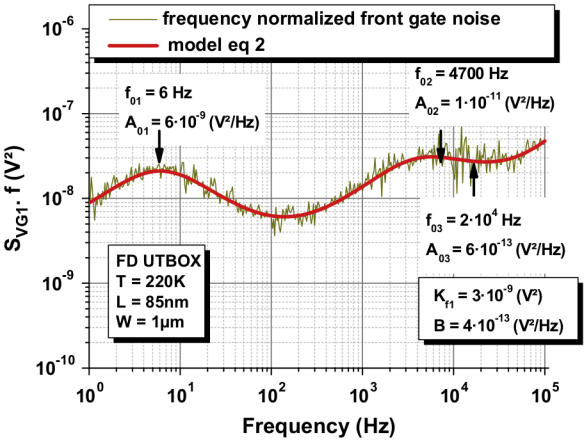

Fig. 9. Modelling of a noise spectrum using Eq. (2).

This model assumes that the noise sources are related to fluctuations of the front and back flat- band voltages, and if one channel is activated, the opposite channel is in depletion or weak inversion mode. Then, the coupling effect on the front and back interface input voltage noise ($S_{V_{G_1}}$ *and* $S_{V_{G_2}}$) can be described by:

$$\begin{aligned} S_{V_{G_1}} &= S_{V_{FB_1}} + c_1^2 S_{V_{FB_2}} \\ S_{V_{G_2}} &= c_2^2 S_{V_{FB_1}} + S_{V_{FB_2}} \end{aligned} \quad (3)$$

where $S_{V_{FB_{1,2}}}$ are the voltage spectral density in the flat-band operation for the front and the back interface defined in Eq. (1) and $c_{1,2}$ are the front (back) coupling effect parameter defined as:

$$c_{1,2} = \frac{C_{Si}}{C_{ox_{1,2}}\left(1 + \frac{C_{Si}}{C_{ox_{2,1}}}\right)} \quad (4)$$

where C_{Si}, C_{ox_1} and C_{ox_2} are respectively the capacitances of the buried silicon film, the front and the back interfaces.

It can be simply derived that the parameters K_{f1} and K_{f2} represent the input 1/*f* voltage noise $S_{V_{G_1}}$ and $S_{V_{G_2}}$ at 1 Hz. The front gate 1/*f* noise level K_{f1} is extracted from the total noise by varying the front gate voltage overdrive while the source and substrate are grounded; the back gate 1/*f* noise level K_{f2} is extracted from the total noise by varying the back gate voltage overdrive while the source and the front gate are grounded; for all measurements, the drain potential is maintained at 50 mV. The values of the C_{Si} and $C_{ox_{1,2}}$ capacitances and the coupling coefficients $c_{1,2}$ of these devices are summarised in Table 2.

The extracted K_{f1} and K_{f2} levels for the front and back interfaces are shown in Figs. 10a and 10b, respectively. For lowest applied front gate voltage overdrives (and for lowest applied back voltage overdrives $V_{BT} = V_{BS} - V_{thb}$) the 1/*f* levels K_{f1} and K_{f2} are quasi-constants. This feature clearly indicates that carrier number fluctuations due to carrier trapping in the oxide layer dominate the 1/*f* noise [28]. The increase of the noise in strong inversion could be explained by the access resistance contribution to the 1/*f* noise. Considering uncorrelated noise sources in the channel and the source/drain regions, the total low frequency noise can simply be obtained by adding to the channel noise the contribution of the excess noise originating from the access region. In linear region of operation, assuming that the drain and source access regions are symmetric, the total voltage noise spectral density can be simplified as Eq. (5) [29–31]:

$$S_{V_{G_{1,2}}} = (r_{T_{1,2}} - r_{access})^2 (S_V)_{channel_{1,2}} + \frac{K_{r_{1,2}}}{f} \frac{r_{access}^2}{2r_{T_{1,2}}^2} \frac{I_{D_{1,2}}^2}{g_{m_{1,2}}^2}. \quad (5)$$

where the subscripts 1 and 2 are related to the front interface and to the back interface, respectively; r_T is the dynamic total resistance between source and drain, r_{access} is the dynamic access resistance, K_r is the access resistance noise level, I_D is the drain current and g_m the transconductance.

The K_{f1} and K_{f2} behaviours with the applied gate overdrive and back gate overdrive, respectively, can be well modelled by Eq. (3). This suggests that the access resistance noise contribution explains the increase of the noise in strong inversion for both interfaces. It should be observed that the access resistance noise level K_r is higher for the front channel compared to the back channel ones.

The extraction of the front (back) spectral density in the flat-band operation can then be performed using Eqs. (3) and (4) and

Table 2
C_{Si}, $C_{ox_{1,2}}$ and the coupling coefficients $c_{1,2}$ for the studied devices.

C_{Si} (F/m^2)	C_{ox_1} (F/m^2)	C_{ox_2} (F/m^2)	c_1	c_2
6.58×10^{-3}	13×10^{-3}	3.43×10^{-3}	17.4×10^{-2}	1.26

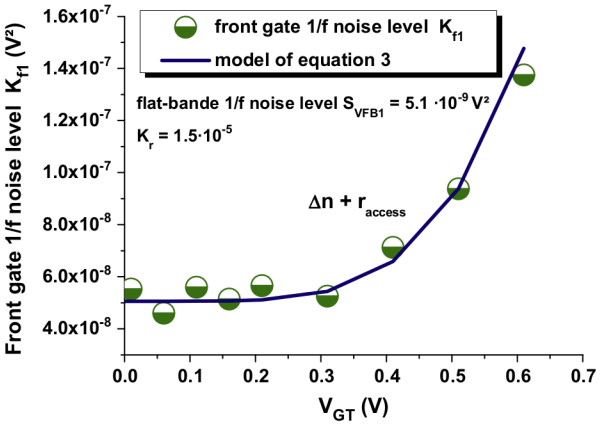

Fig. 10a. The extracted front gate 1/*f* noise level K_{f1} versus the applied front gate overdrive.

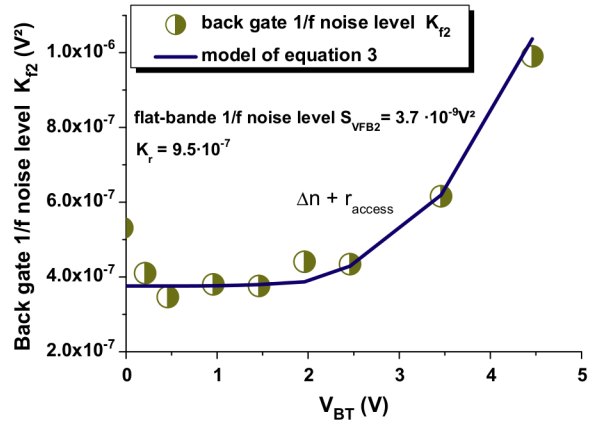

Fig. 10b. The extracted back gate 1/*f* noise level K_{f2} versus the applied back gate overdrive.

the technology parameters for the studied devices, summarized in Table 2. The slow oxide trap densities of the front oxide N_{t1} and of the back oxide N_{t2} can be extracted using Eq. (1). The obtained values are reported in Table 3:

It can be observed that the contribution of the back interface noise source is about 14% on the measured noise in the front channel conduction, while the contribution of the front interface noise source is about 22% on the measured noise in the back channel conduction. A similar contribution was observed for all investigated samples with 85 nm effective channel lengths, for which N_{t1} were found in the range of 7–12 · 10^{18} (cm^{-3} eV^{-1}) while N_{t2} was in the range of 2–6 · 10^{18} (cm^{-3} eV^{-1}).

3.2.2. Noise spectroscopy

In general, the Lorentzian component of the noise spectra can originate from traps located in the dielectric, at the interface dielectric/semiconductor or in the depletion zone. Random telegraphic signals (RTS), which are commonly attributed to individual carrier trapping at the silicon-oxide interface, can also be observed in small area devices (<1 μm^2). In this work, we will focus only on traps in the depletion region. According to [13], for a fixed temperature operation, if the characteristic frequency of a Lorentzian does not change with the applied gate bias, this Lorentzian can be assigned to a trap located in the depletion film. In this case the characteristic frequency should vary with the temperature. Only Lorentzians which satisfy these two conditions were taken into account. Fig. 11 illustrates an example of the frequency normalized noise spectral density versus the temperature, from which temperature variations of the characteristic frequency with the temperature can be observed.

In frequency normalized noise spectral density versus frequency plots, the Lorentzian contributions will exhibit bumps centred at their characteristic frequencies (Fig. 9). The front gate voltage spectral density $S_{V_{G_{lor}}}$ of a trap located in the depletion area can be expressed as:

$$S_{V_{G_{lor}}}(f) = \frac{q^2 B W_d N_{T\tau}}{WLC_{ox_1}^2} \frac{1}{1+(2\pi f\tau)^2}. \quad (6)$$

where B is a coefficient estimated to be 1/3 [32,33]; N_T is the density of the trap in the silicon film; W_d is the silicon film depletion depth (in our case the depletion depth is equal to the buried silicon film thickness t_{Si}) and τ is the relaxation time constant.

For each Lorentzian characterized by its plateau level A_i $\left(\text{defined as } A_i = \frac{q^2 BT_{Si}N_T}{WLC_{ox_1}^2}\tau_i\right)$ and its characteristic frequency f_{oi}, one can associate a trap density N_T of time constant τ_i (τ_i defined as $1/(2\pi f_{oi})$). According to [13], the variation of the characteristic frequency f_{oi} as a function of the temperature can be equated as:

$$\ln(\tau T^2) = \frac{E_C - E_T}{kT} + \ln\left(\frac{h^3}{4k\sigma_n\sqrt{6\pi^3 M_c m_e^{*1/2} m_h^{*3/2}}}\right). \quad (7)$$

where h is the Planck constant; m_e^*, m_h^* are the effective mass of electrons and holes respectively and M_c is the number of conduction band energy minima.

From the slope and the y-intercept of the evolution of $\ln(\tau T^2)$ versus $1/(kT)$ one can extract the energy difference between the appropriate band energy and the trap energy (i.e. $\Delta E = E_C - E_T$) and the electron capture cross section σ_n of the trap, respectively. The physical nature of these traps can be identified by comparing the energy and capture cross section of the traps with data in the literature.

A typical Arrhenius diagram is plotted in Fig. 12. In this example, 6 kinds of traps can be clearly identified: divacancies $V_2(+/0)$ and $V_2(-/-)$ [34–36], interstitial boron-interstitial-oxygen complex (B_iO_i), interstitial boron substitutional-boron complex (B_iB_s) [34,36], interstitial carbon-interstitial-oxygen complex (C_iO_i) and vacancies-phosphor (VP) [36–38]. In addition of these, 2 unknown traps were evidenced.

The evolution of the Lorentzian plateau A_i versus τ_i (A_i and τ_i associated to the same trap) should be linear. This is verified for all observed traps; an example is shown in Fig. 13. From the slope of A_i versus τ_i, the trap density N_T of each trap in the silicon film can be estimated. In order to make no assumption on the B coefficient, which was estimated at 1/3 for a bulk planar single gate transistor [33,39] from the evolution of the A_i versus τ_i the effective trap density, defined as $N_{eff} = BN_T T_{Si}$, was extracted. The extracted effective trap densities of each trap for this example are summarized in Fig. 14. It can be observed that the obtained values of the effective traps densities are almost 2 order of magnitude lower compared to other non-intentionally doping channel technologies [12].

For all the investigated n-channel UTBOX devices with effective channel of 85 nm 6 kinds of traps were clearly identified: divacancies $V_2(+/0)$ and $V_2(-/-)$, interstitial boron-interstitial-oxygen

Table 3
Example of noise parameters for devices with L_{eff} = 85 nm.

$S_{V_{FB_1}}$ (V²)	$S_{V_{FB_2}}$ (V²)	N_{t1} (cm^{-3} eV^{-1})	N_{t2} (cm^{-3} eV^{-1})
4.1 × 10^{-8}	3.1 × 10^{-7}	11 × 10^{18}	6 × 10^{18}

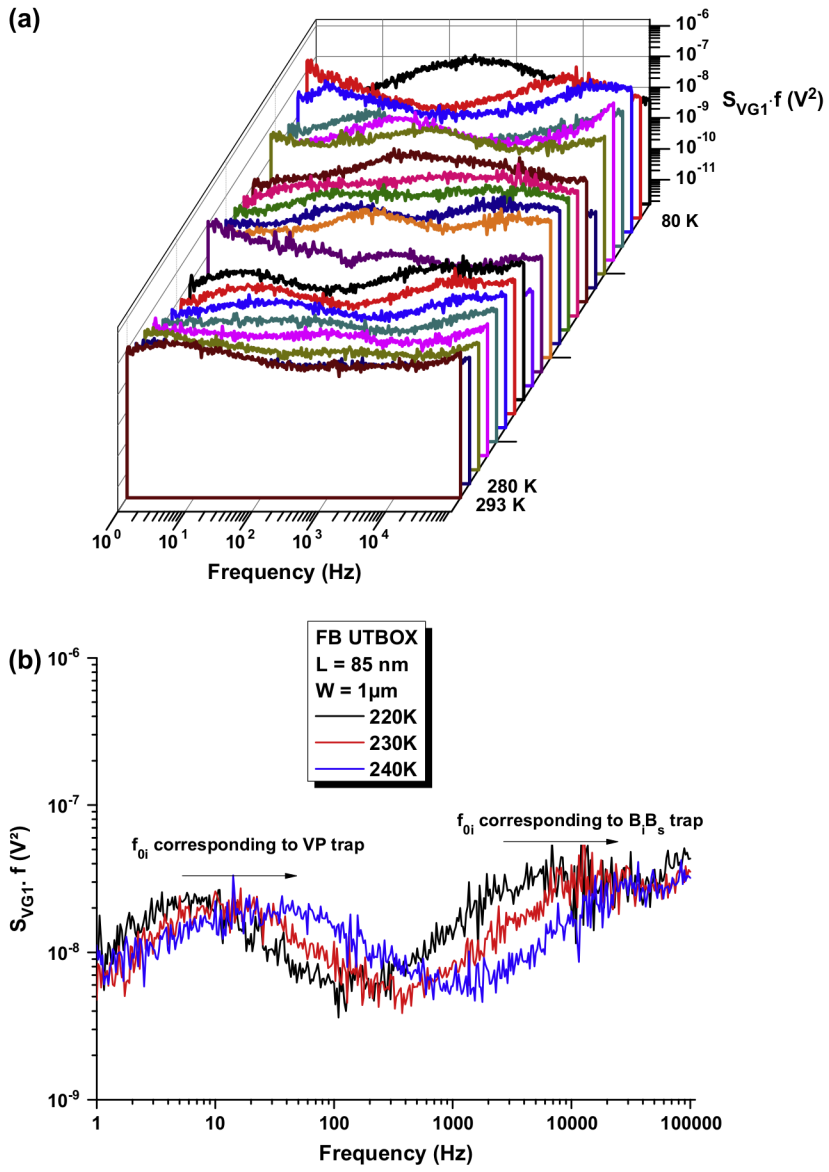

Fig. 11. Example of the front gate voltage frequency normalized noise spectral density versus temperature for a UTBOX nMOSFET with effective gate length of 85 nm: (a) for all investigated temperatures and (b) for three different temperatures in order to observe the temperature variation of Lorentzians characteristic frequency (indicated by the arrows) which are then assigned to traps located in the fully depleted film.

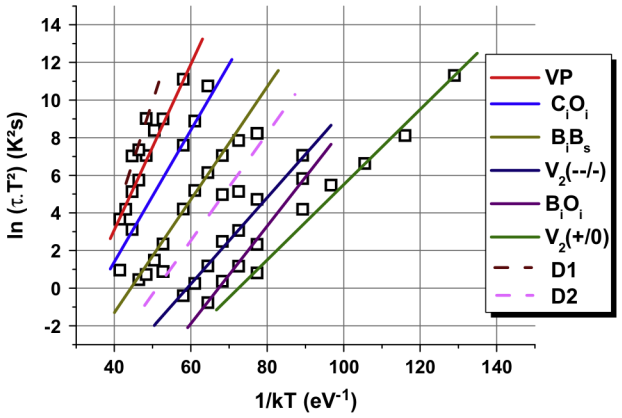

Fig. 12. Example of an Arrhenius plot for a sample with the effective gate length of 85 nm. $V_2(+/0)$: $\Delta E = 0.20$ eV, $\sigma_n = 10^{-15}$ cm^2; $V_2(-/-)$: $\Delta E = 0.23$ eV, $\sigma_n = 10^{-15}$–10^{-16} cm^2; B_iO_i: $\Delta E = 0.26$ eV, $\sigma_n = 10^{-13}$–10^{-14} cm^2; B_iB_s: $\Delta E = 0.3$ eV, $\sigma_n = 3 \times 10^{-16}$ cm^2. $C_iO_i(0/-)$: $\Delta E = 0.35$ eV, $\sigma_n = 10^{-16}$ cm^2; VP: $\Delta E = 0.44$ eV, $\sigma_n = 10^{-14}$–10^{-15} cm^2 D1: 1 $\Delta E = 0.53$ $\sigma_n = 1.5 \times 10^{-14}$ cm^2; D2: $\Delta E = 0.27$ eV; $\sigma_n = 4.8 \times 10^{-16}$ cm^2.

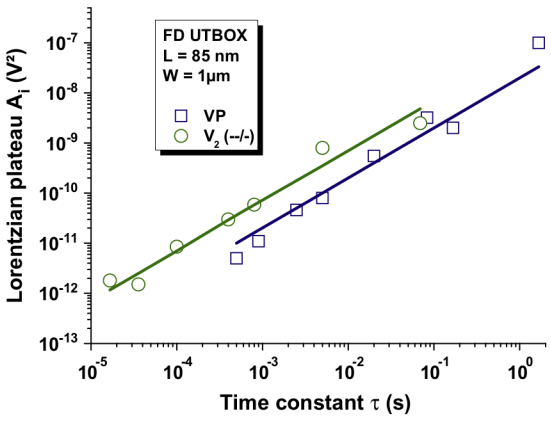

Fig. 13. Example of the evolution of the Lorentzian plateau A_i versus the time constant τ_i associated with the same trap.

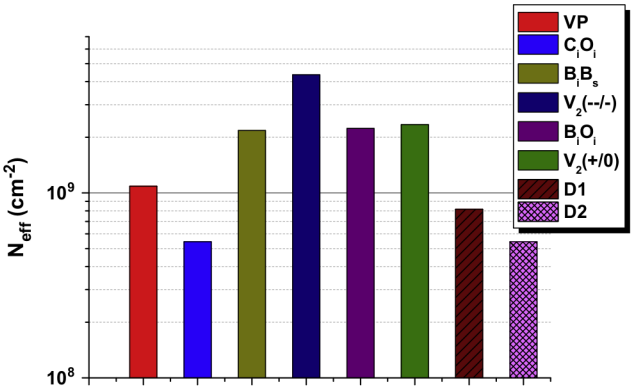

Fig. 14. Trap densities extracted from the evolution of the Lorentzian plateau A_i versus the time constant τ_i for these UTBOX device with an effective gate length of 85 nm.

complex (B_iO_i), interstitial boron-substitutional-boron complex (B_iB_s), interstitial carbon-interstitial-oxygen complex (C_iO_i) and vacancies-phosphor (VP). All the studied structures have received a boron halo implantation (used to reduce the short channel effects). This may explain the presence of the traps related to boron. The traps related to phosphor may also be related to the HHD implantation. The presence of divacancies could be explained by the recombination or the evolution to a stable state of the unstable defects like Frenkel pairs, which could be generated during the implantation. A possible carbon contamination due to the SiC liner deposition step can explain the traps related to carbon. One can notice that a variety of traps are reported in the literature. Most likely, they may originate from the dry-etching or implantation damage. The number of observed traps is important: this may be due to the relatively low value of the pure $1/f$ noise and the advanced technology used to process the devices.

4. Conclusions

In this paper we have compared UTBOX nMOSFETs with different gate dielectrics through their low frequency noise performance. A poorer oxide quality has been found mainly for HfSiO devices compared to the SiO_2 ones, which resulted in a degraded low-field mobility. Moreover, high-k devices have shown higher Coulomb scattering and also higher oxide trap density as expected. A linear trend has been found between front and back S_{v_G} for both type of dielectrics, emphasizing the influence of the strong electrostatic coupling between front and back channels for thin silicon film technologies.

The carrier number fluctuations dominate the $1/f$ noise for both front and back interface considering the different dielectric samples studied in this work. In strong inversion, the access resistance noise contribution in the total $1/f$ noise prevails. It was found that the access resistance noise level is higher for the front channel compared to back channel. Taking into account the contribution of both interfaces the interface trap densities were estimated. The quality of the front and back gate oxide interfaces was evidenced by the relatively small values of the oxide trap densities. Moreover, for all investigated devices, the contribution of the back interface noise source is about 14% of the measured noise in the front channel conduction, while the contribution of the front interface noise source is about 22% of the measured noise in the back channel conduction.

The analysis of the temperature evolution of the Lorentzian time constants allowed to identify traps in the silicon film. For all the investigated n-channel devices, 6 kinds of traps were clearly identified and 2 kinds of unknown traps have been frequently observed. However, most likely, they can originate from the dry-etching or implantation damage.

Acknowledgments

The authors would like to acknowledge the Brazilian research-funding agency CAPES, CNPq and FAPESP for the support for developing this work. The imec Core Partners are gratefully acknowledged for financial support within the frame of the FBRAM program. Part of the work has been performed in the frame of the Tournesol 2012 project (T2012.19).

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