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Low-Frequency Noise Studies on Fully Depleted UTBOX Silicon-on-Insulator nMOSFETs: Challenges and Opportunities

E. Simoen,[a,*,z] M. Aoulaiche,[a] S. D. dos Santos,[b] J. A. Martino,[b,*] V. Strobel,[c] B. Cretu,[c] J.-M. Routoure,[c] R. Carin,[c] A. Luque Rodríguez,[d] J. A. Jiménez Tejada,[d,*] and C. Claeys[a,e,]**

[a]*Imec, B-3001 Leuven, Belgium*
[b]*LSI/PSI/USP, University of São Paulo, São Paulo, Brazil*
[c]*GREYC/ENSICAEN/CNRS UMR 6072, Université de Caen, Caen, Basse Normandie, France*
[d]*Departamento de Electrónica y Tecnología de los Computadores, Facultad de Ciencias, Universidad de Granada, Granada, Spain*
[e]*EE Department, KU Leuven, B-3001 Leuven, Belgium*

The low-frequency (LF) noise behavior of Fully Depleted (FD) Ultra-Thin Buried Oxide (UTBOX) Silicon-on-Insulator (SOI) nMOSFETs is described from the perspective of the three major noise sources: 1/f-like or flicker noise, associated with carrier trapping/detrapping in the gate oxide; Generation-Recombination (GR) noise due to processing-induced defects in the thin silicon film and single-oxide-trap-related Random Telegraph Noise (RTN). It is shown that the fully depleted nature of the thin silicon films (<20 nm) offers the unique opportunity to study and demonstrate the front-back coupling of the 1/f noise. At the same time, a large variability is induced in the noise power spectral density by the presence of Lorentzian noise, related with GR events through defects in the silicon film. A method to discriminate oxide- from film-defects-related Lorentzian noise is pointed out. Finally, the implications for future fully depleted fin-type of devices will also be addressed.
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As device dimensions in Complementary Metal-Oxide-Semiconductor (CMOS) technology scale down further along the roadmap, variability of the main static parameters, like the threshold voltage V_T becomes a key issue, threatening the proper functioning of logic and memory circuits.[1–3] A major cause of device variability is the Random Dopant Fluctuations (RDF), which find their root cause in the random nature of ion implantation, used for engineering the channel doping concentration and, hence, the V_T. This can be largely avoided by going over to a fully depleted (FD) Silicon-on-Insulator (SOI) or a multiple-gate, fin-type of platform, where a natural-doped silicon layer is used instead.[4,5] Non-intentionally doped FD Ultra-Thin Buried Oxide (UTBOX) SOI offers several advantages from a viewpoint of the suppression of dopant-related variability and short-channel effects.[5] There is also interest in using such devices as capacitorless 1-transistor (1T) floating-body RAM (1T-FBRAM) cells.[6,7] For the latter applications, charge retention is one of the critical parameters, requiring a tight control of defect-related carrier generation and recombination (GR). Therefore, the analysis of electrically active defects in such FBRAM devices is of crucial importance. One of the techniques which lends itself nicely to this purpose is low-frequency (LF) noise spectroscopy, which can reveal GR centers in the gate dielectric or the silicon film.[8,9] Three main types of low-frequency noise can be distinguished, namely, 1/f-like or flicker noise, GR noise and Random Telegraph Noise (RTN).

In fact, another well-known source of dynamic fluctuations appears at the horizon, which is related to the occurrence of Random Telegraph Noise (RTN) in small-area transistors.[10–14] In the past, RTN was only relevant for analog and mixed signal applications but, currently, it can become problematic even for deeply scaled logic and memory applications as well.[3,15,16] The origin of RTN is related to charge capture and emission by a single trap, residing generally in the gate dielectric of a MOS device in the vicinity of the interface.[11] Ample evidence has been presented that the corresponding normalized amplitude of the drain current fluctuation ($\Delta I_D/I_D$) can range over several orders of magnitude in a large set of similar devices.[17–22] While this wide variation was puzzling at first, it has become clear that it can be understood in the frame of a non-uniform filamentary channel, defined by the random location of dopant atoms and fixed oxide charges, with a trap in its neighborhood.[1–3,19,20] In this picture, the spread in RTN amplitude is mainly defined by the trap position with respect to the non-uniform potential landscape of the channel.

Here, it will be demonstrated that for thin-film, fully depleted transistors, e.g., FD SOI or narrow fin-type of devices (bulk or SOI FinFETs) there is an alternative source of variability of RTN - or in general Lorentzian GR noise - which is associated with the energy level position of a GR center in the silicon film. It is shown that this is related to the fact that in FD structures, the quasi Fermi level for electrons E_{Fn} can be easily swept over a large portion of the bandgap by the front and/or back-gate voltage, so that its relative position with respect to the trap level E_T can change significantly. This gives rise to a Lorentzian noise amplitude which may vary over more than a decade with V_{GS}. This sensitivity to voltage variations helps to understand the device-to-device variation in the current noise power spectral density (PSD) at the same biasing conditions. This will be illustrated here for nMOSFETs made in UTBOX SOI wafers. If at the same time, a thin silicon film is used, coupling effects between the front and the back or buried interface start to appear.[23–25] As is shown here, for a film thickness t_{Si} < 20 nm, coupling in the LF noise (and in particular in the 1/f noise) becomes observable.[26,27] A procedure to derive the correct front-channel noise PSD will be proposed.

Experimental

The FD SOI nMOSFETs studied in this work have been fabricated on 300 mm diameter SOI substrates with nominally 10 nm BOX and 20 or 10 nm Si film thickness (t_{Si}). Transmission Electron Microscopy (TEM) reveals that the actual values for the short-channel devices are closer to 18 nm (BOX) and 14 and 6 nm for t_{Si}. A cross-section micrograph is depicted in Fig. 1, indicating the main device dimensions. Different types of gate stacks have been investigated with 5 nm thermal SiO_2 (t_{ox}) as the reference, but also HfO_2-based high-k devices have been analyzed.[28] Processing splits with or without extensions have been compared, whereby extensionless structures may offer a higher retention time.[6,7] The device width W = 1 μm and different effective lengths (105 nm or 69 nm) have been investigated. Noise measurements have been mainly performed in linear operation (V_{DS} = 0.05 V) and with the back-gate grounded, i.e., V_{GB} = 0 V. The front-gate voltage (V_{GS}) was stepped from weak to strong inversion in 50 or 100 mV steps. Also noise in the back-channel was measured with the front-gate at 0 V. In a few cases, corresponding with t_{Si} = 14 nm, the noise in the front (back) channel was evaluated with the opposite interface biased in accumulation.

*Electrochemical Society Active Member.
**Electrochemical Society Fellow.
zE-mail: eddy.simoen@imec.be

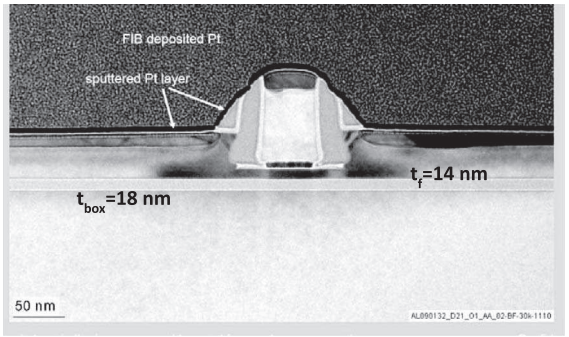

Figure 1. Transmission Electron Microscopy cross-section of a 69 nm long UTBOX nMOSFET with a 14 nm Si film and 18 nm BOX thickness.

Flicker noise and coupling

Typical front-channel noise spectra of the current noise PSD S_I versus frequency f exhibit both 1/f-like and Lorentzian noise, like in Fig. 2. The observed 1/f-like noise is dominated by number fluctuations, i.e., it originates from trapping in the gate oxide, both for the front-gate and back-gate noise PSD.[27] This is illustrated by Fig. 3, representing the normalized current PSD (S_I/I_D^2) versus I_D in linear operation and comparing it with $(g_m/I_D)^2$, with g_m the transconductance. As can be seen, both functions are proportional to each other, with a plateau in weak inversion. This is a fingerprint of the Δn or number fluctuations origin of the 1/f noise.[29,30] The presence of the Lorentzian noise at higher frequencies in Fig. 2 may also indicate noise due to border traps in the gate oxide.[31]

The fact that the flicker noise is caused by trapping implies that a density of oxide traps N_{ot} can be extracted from the input-referred voltage noise PSD ($S_{VG} = S_I/g_m^2$) at flatband voltage (V_{FB}), according to:[29,30]

$$S_{VFB_{1,2}} = \frac{q^2 kT\lambda N_{ot_{1,2}}}{f^\gamma WLC^2_{ox_{1,2}}} \quad [1]$$

with q the elementary charge, WL the device effective width times the effective length, γ the frequency exponent (~1), k Boltzmann's constant, T the absolute temperature and λ the decay length of the electron wave function in the gate dielectric (~0.1 nm for SiO_2). C_{ox} is the oxide capacitance density of the front (subscript 1) or the back (subscript 2) interface. However, in the case of thin-film fully depleted SOI, the front-channel noise PSD with the back interface in depletion ($V_{GB} = 0$ V) will be affected by coupling to the noise at the back-channel,[23,24] giving rise to:

$$S_I^{dep} \approx S_I^{acc}\left(1 + \alpha^2 \frac{C^2_{ox,1} N_{ot,2}}{C^2_{ox,2} N_{ot,1}}\right) \quad [2]$$

with α corresponding with:

$$\alpha = \frac{C_{Si} C_{ox,2}}{C_{ox,1}(C_{ox,2} + C_{Si} + C_{it,2})} \quad [3]$$

In Eq. 3, C_{Si} is the capacitance density of the silicon film ($= \varepsilon_0 \varepsilon_{Si}/t_{si}$; ε_0 is the permittivity of vacuum and ε_{Si} is the dielectric constant of silicon). In case the back-interface state capacitance density $C_{it,2}$ can be neglected, Eq. 3 is simplified to:

$$\alpha = \frac{C_{Si}}{C_{ox,1}\left(1 + \frac{C_{Si}}{C_{ox,2}}\right)} \quad [4]$$

In Eq. 2, S_I^{dep} and S_I^{acc} are the current noise PSD with the back interface in depletion or in accumulation. When the back- (or front-) interface can be biased in accumulation, the fluctuations by back- (front-) oxide traps are screened completely, so that only the noise due to traps at the front- (or back-) interface will be measured, enabling a correct extraction of $N_{ot,1,2}$, using Eq. 1. For ultra-thin silicon films, where the back-interface cannot be accumulated, Eq. 2 predicts that the measured noise at the front will be higher due to the effect of the back-oxide traps and vice versa. If the trap density is the same in the front and buried oxide, i.e., $N_{ot,1} = N_{ot,2}$ the enhancement factor will be $\alpha^2 t^2_{ox,2}/t^2_{ox,1}$.

Figure 4 represents the S_{VG} at weak inversion for the back-channel versus the front-channel 1/f noise PSD, for a set of 69 nm UTBOX nMOSFETs with t_{si}~14 nm and $t_{ox} = 5$ nm. In both cases, the channel noise was measured with the opposite interface at 0 V, thus in depletion. The dashed line represents a linear fit corresponding with a slope of 8.5,[27,28] which is smaller than the anticipated ratio of $(t_{ox,2}/t_{ox,1})^2$~13 for equal trap densities $N_{ot,1} = N_{ot,2}$. This points in the first place to the impact of the front-back coupling, i.e., $\alpha \neq 0$. The fact that a close to linear correlation is observed in Fig. 4 rules out the possibility of a widely different trap density in the front- and back-gate oxide for the same transistor. In this case, a correct evaluation of N_{ot} is possible by measuring the noise with the opposite interface in accumulation. Typical trap densities are in the range 2×10^{16} cm^{-3} eV^{-1} to 2×10^{17} cm^{-3} eV^{-1} for the front- and 2×10^{16} cm^{-3} eV^{-1} to 1.3×10^{17} cm^{-3}eV^{-1} for the back-channel.[27,28] Given the rather similar N_{ot} values for both oxides, the difference between the experimental

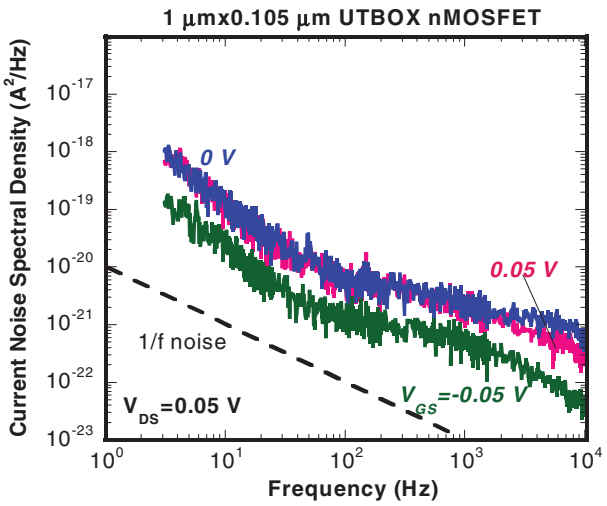

Figure 2. Low-frequency noise spectra around V_T for a 1 µm × 0.105 µm UTBOX SOI nMOSFET, exhibiting flicker noise around 10 Hz. The back-gate is at 0 V in depletion. The drain voltage $V_{DS} = 0.05$ V in linear operation.

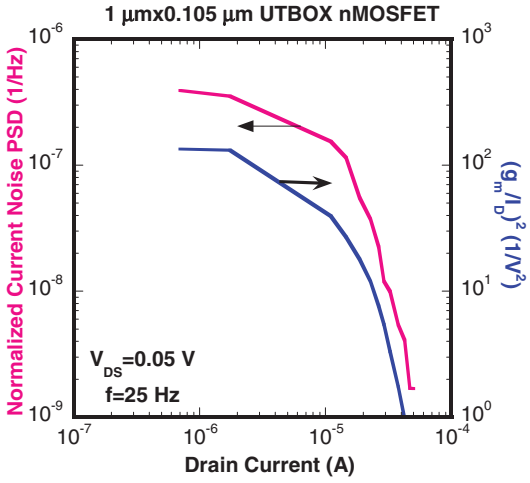

Figure 3. Normalized current noise PSD at 25 Hz versus drain current and $(g_m/I_D)^2$ versus I_D in linear operation ($V_{DS} = 0.05$ V) for a 1 µmx0.105 µm UTBOX SOI nMOSFET.

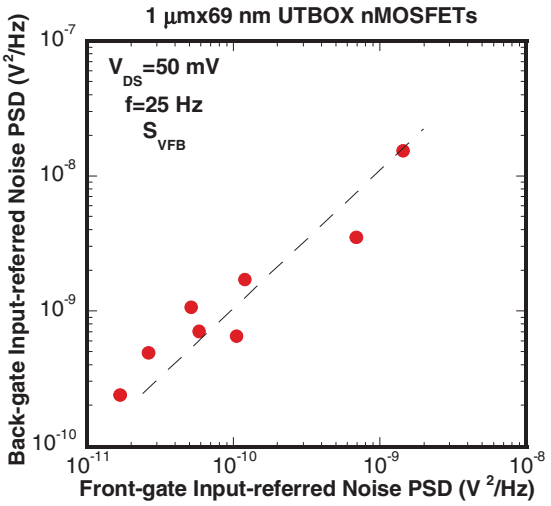

Figure 4. Back- versus front-channel average input-referred noise PSD at threshold voltage ($V_{GS}\sim V_T$), f = 25 Hz and V_{DS} = 50 mV for a set of 1 µm × 69 nm UTBOX nMOSFETs with $t_{Si} \approx 14$ nm and $t_{SiO2} = 5$ nm.

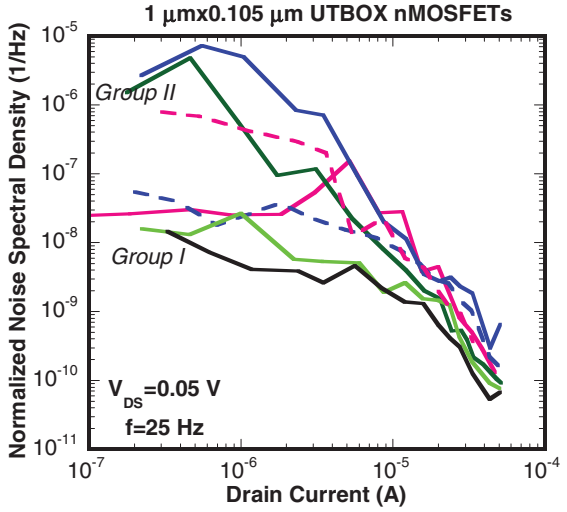

Figure 6. Normalized current noise spectral density versus drain current at f = 25 Hz and in linear operation for a set of FD SOI nMOSFETs, aligned across the vertical diameter in the center of an UTBOX wafer.

and theoretical slope can be mainly ascribed to the coupling factor α. Assuming that $S_I^{acc} = t^2_{ox,1}/t^2_{ox,2}S_{I,2}$ and that $S_{I,2}$ corresponds to the measured back-gate spectral density at V_{GS} = 0 V, a coupling factor of 0.2 is derived, which is close to the theoretical value of 0.221 in this case.

For the 6 nm film transistors studied here, it is difficult to bias the back-gate into accumulation. In that case, the coupling effect has to be accounted for both in the front- and the back-channel noise.[27,28,32,33] In the case of UTBOX nMOSFETs with a high-k front oxide, one expects a significantly higher border trap density from the flicker noise in the front-channel, compared with the SiO_2 back-channel, which is indeed observed in practice.[28,32,33]

GR noise and noise variability

As shown in Fig. 2, excess GR noise, giving rise to a gate-voltage dependent Lorentzian spectrum can be found at higher frequencies (∼1 kHz). In some devices, on the other hand, GR noise also dominates at low frequencies, overwhelming the 1/f noise (Fig. 5). The high magnitude of these Lorentzians gives rise to a strong device-to-device variation in the LF noise PSD, as shown in Fig. 6: the normalized current noise PSD of similar UTBOX SOI nMOSFETs at a frequency f = 25 Hz can vary over more than two decades at low drain currents I_D. Two groups of devices can be distinguished in Fig. 6: one with the lower PSD and corresponding with a $1/f^\gamma$ spectrum at low frequencies in Fig. 2 ($\gamma\sim1$) and a second set of devices, exhibiting a pronounced Lorentzian GR noise at low f (Fig. 5). Comparing Figs 2 and 5, it is clear that the excess GR noise is responsible for the one to two decades higher PSD observed for the Group II nMOSFETs in Fig. 6.

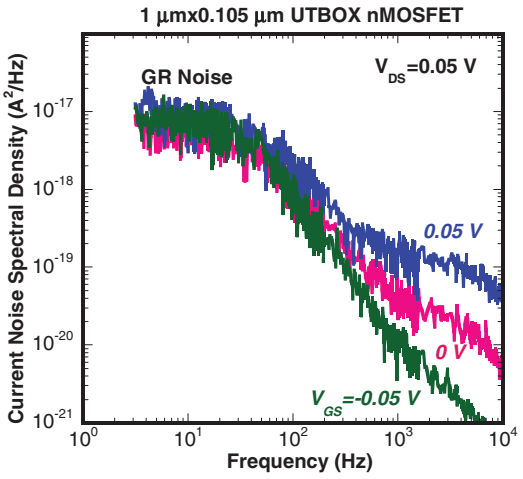

Figure 5. Low-frequency noise spectra around V_T for a 1 µm × 0.105 µm UTBOX SOI nMOSFET, exhibiting Lorentzian generation-recombination noise around 10 Hz.

First, the origin of the excess GR noise in Fig. 5 has to be established. It is clear that the main parameters of the Lorentzian around 10 Hz in Fig. 5, namely, the plateau amplitude $S_I(0)$ and the corner frequency (f_0) are fairly independent on the front-gate voltage V_{GS}. This has been used in the past as an argument to ascribe the underlying trap centers as residing in the silicon depletion region in partially depleted or bulk MOSFETs, when they are operated in strong inversion.[8,9,34,35] Another argument in favor of this assignment is the fact that very similar Lorentzian noise is observed in the front- and back-channel operation of the thin-film UTBOX FD SOI nMOSFET.[26,27] Since the same Lorentzian is observed in the front- and back-channel current noise, its origin should be common to both, i.e., the fully depleted silicon film. If it corresponded to a gate oxide trap or in other words, to RTN, then the GR noise should only be present in the spectrum of the front- or the back-channel.[36]

More recently, this interpretation of the gate-bias dependence of Lorentzian noise has been challenged for FD SOI nMOSFETs.[37,38] Based on an extension of the classical model for GR noise in the depletion region of a MOSFET,[34,39] it has been shown that the Lorentzian parameters for a deep level center, which may exist in FD SOI or narrow FinFET type of structures, can show a strong variation with gate bias. The model for the GR noise considers a PSD described by:[34,37–39]

$$S_I(f) = \frac{\overline{\delta I_d^2}}{\Delta f} = \frac{4q^2 Z}{L^2}\int_{x=0}^{L}(\mu_{n,eff}RF(x))^2 \times \int_{y=0}^{y_{max}} N_T\left(1-\frac{y}{y_{max}}\right)^2 \frac{f_t(1-f_t)\tau}{1+(2\pi f\tau)^2}dxdy \quad [5]$$

In Eq. 5, f_t is the Fermi function, defining the electron occupation of the trap level E_T, with concentration N_T and electron capture cross section σ_n. Z and L are the transistor width and length, respectively, while the integral of the Lorentzian spectrum is carried out over the thickness of the silicon film, from the front interface at y = 0 to the buried interface at y_{max}, which corresponds to the film (or fin) thickness. The first integral runs over the length of the transistor in

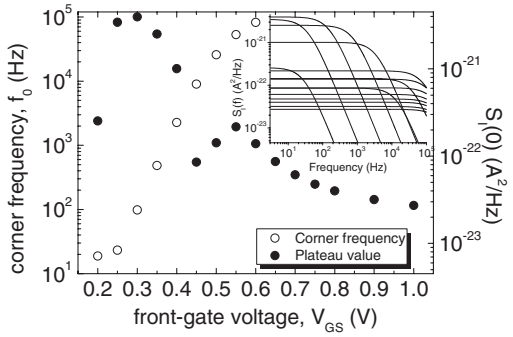

Figure 7. Simulated corner frequency f_0 and plateau value $S_I(0)$ of the Lorentzian component as a function of the front-gate voltage. The back-gate voltage is 0 V. Inset: detail of the variation of the corresponding Lorentzian spectra with gate voltage. E_T-E_i = 0.16 eV; $\sigma_n = 2.5 \times 10^{-19}$ cm^2 and $N_T = 10^{17}$ cm^{-3}.

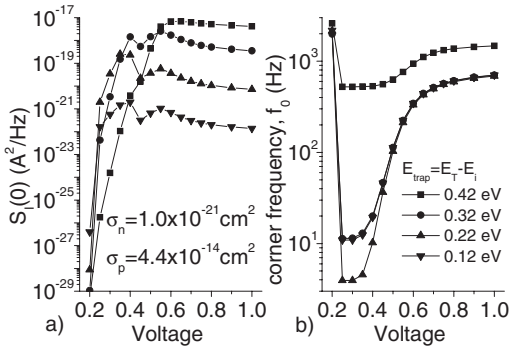

Figure 8. Simulated plateau amplitude (a) and corner frequency (b) as a function of the front-gate voltage at zero back-gate, corresponding with different trap level positions with respect to the intrinsic Fermi level E_i. An electron capture cross section of 1.0×10^{-21} cm^2 and a hole capture cross section $\sigma_p = 4.4 \times 10^{-14}$ cm^2 has been considered in the calculations. The existence of minority traps, such as the one analyzed in this figure can boost the noise variability. In this case, the peak seen at low voltages in (b) reflects the fact of a small number of electrons in the silicon and that the term related to hole capture and emission cannot be neglected.

the x direction and includes non-uniformities of the electric field F(x) and the effective electron mobility $\mu_{n,eff}$. For a channel with uniform doping profile and in linear operation, F(x) becomes V_{DS}/L. Finally, the coupling factor R equals $C_N/(C_N + C_{ox,1} + C_{Si})$, with C_N, $C_{ox,1}$ and C_{Si} the capacitance densities of the inversion channel, the front-oxide and the depletion region (Si film) and is included to avoid divergence of the PSD of Eq. 5.[37,39]

The GR time constant in Eq. 5 is given by the Shockley-Read-Hall (SRH) expression:

$$\tau(x, y) = [c_n(n(x, y) + n_t) + c_p(p(x, y) + p_t)]^{-1} \quad [6]$$

with n(x,y), p(x,y) the position-dependent free electron and free hole concentration, respectively; n_t (p_t) the electron (hole) concentration when the Fermi level coincides with the trap level and c_n and c_p are the capture rates for electrons and holes, equal to the product of the respective capture cross section and thermal carrier velocity. The free carrier concentration profiles have been obtained from well-calibrated 2-dimensional device simulations of the UTBOX SOI nMOSFET input characteristics.[37] For normal operation conditions of the nMOSFETs, the second term related to hole capture and emission in Eq. 6 can generally be neglected.

As exemplified by Fig. 7, the Lorentzian parameters exhibit a strong variation with the front-gate bias V_{GS}. This is explained by the pronounced dependence of the free electron concentration n(x,y) on the Fermi level (Eq. 6), which is modulated by the gate voltage. In case of UTBOX devices (or for independent double-gate FinFETs), also the back-gate bias can be used as an additional variable to change the Fermi level position with respect to the trap level. In turn, this will impact on the free carrier density n(x,y) in Eq. 6, which defines the SRH time constant. One can observe in Fig. 7 that the corner frequency of the Lorentzian given by $f_0 = 1/2\pi\tau$ drastically increases going from low V_{GS} in weak inversion to high inversion. At the same time, the plateau amplitude also increases significantly until a maximum is reached when E_F crosses the trap level E_T. In principle, this can be used to perform trap spectroscopy at room temperature, by using the gate-voltage-modulation of the Lorentzian spectrum.[37]

The point of interest here is the strong variation of the amplitude of the PSD calculated from Eq. 5 with gate voltage, further illustrated by Fig. 8 for traps in a FD silicon film with different activation energy. In other words, according to Fig. 8a, the amplitude of the Lorentzian noise at a fixed V_{GS} can change over several orders of magnitude depending on the trap position with respect to the intrinsic Fermi level (E_i) and set by the front- and/or back-gate voltage. Conversely, by changing the gate voltage, the Lorentzian PSD can be maximized when E_F crosses E_T, giving a maximum contribution to the noise spectrum. This immediately implies that depending on the activation energy of the trap level, a significantly different Lorentzian noise can be obtained. In other words, a much higher Lorentzian amplitude will be obtained when traps in the silicon bandgap are closer to the conduction band edge (E_T-E_i = 0.42 eV) than when they are near midgap (E_T-E_i = 0.12 eV) in Fig. 8b. This corresponds with a significant source of variability in the low-frequency noise amplitude which differs from the one related with the standard RTN mechanism. It is typical for device structures with a FD silicon region between two gates, like in FD SOI or FinFETs on bulk or SOI substrates. Given the importance of the fin architecture for 22 nm and below CMOS nodes, this is expected to become an important source of noise variability and should be accounted for in a similar way as the impact of RTN-induced dynamic variability. In addition, an interplay between static (V_T) and dynamic (GR noise) variability can be expected, as a small shift along the horizontal axis in Fig. 8 can have a major impact on the GR noise PSD for the same trap level, in particular at gate voltages in weak inversion ($V_{GS} < V_T$).

On the other hand, there is no direct correlation between the static and dynamic variability, as evidenced for example by Fig. 9, representing the input-referred voltage noise PSD at threshold voltage and f = 25 Hz versus the low-field electron mobility (μ_n) in linear operation.[40] However, when dividing the noise data into Group I and II (Fig. 6), corresponding with nMOSFETs with predominantly (low) 1/f noise or (high) GR noise below 1 kHz a clear trend becomes

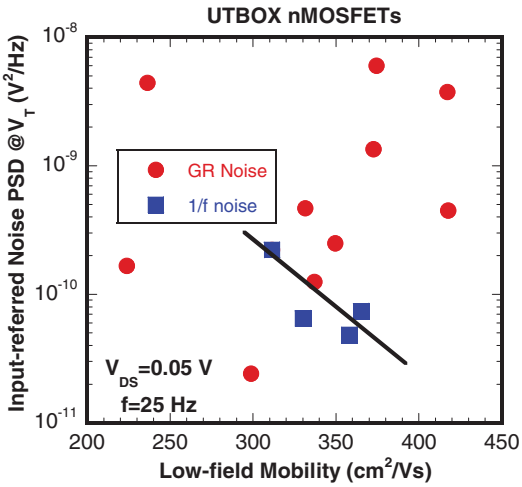

Figure 9. Input-referred voltage noise PSD at threshold voltage versus electron mobility in linear operation (V_{DS} = 50 mV) for a set of 1 μm × 0.135 μm UTBOX nMOSFETs belonging to the same wafer.

obvious. The devices with mainly flicker noise exhibit now an inverse correlation with μ_n, which has been frequently seen in the past for other types of MOSFETs.[41–45] It can be explained by the Coulomb scattering associated with charged border traps in the oxide, which reduces the mobility. In other words, "noisy" devices correspond also with a lower carrier mobility. At the same time, the range of the noise magnitude is much tighter (factor of 4) for the 1/f noise dominated devices than for the Group II ones (at least two decades), indicating that the trap density in the gate oxide also follows a tighter distribution. This is confirmed by the 1 decade spread in border trap densities derived from the 1/f noise in the previous section. It is evident that the LF noise variability is mainly associated with the presence of GR noise, associated with defects in the silicon film. At the same time, it is shown above that the two decades spread in magnitude is not related to a variation in the trap density in the fully depleted silicon film but can be explained by the difference in the kind of deep level, defined by the activation energy (see Fig. 8).

Finally, a more systematic study of the LF noise variability for a higher number of devices and for different geometries should be performed in order to quantify the dispersion and to investigate whether the impact of the GR noise due to silicon film defects becomes more pronounced for shorter lengths, like in the case of standard RTN.

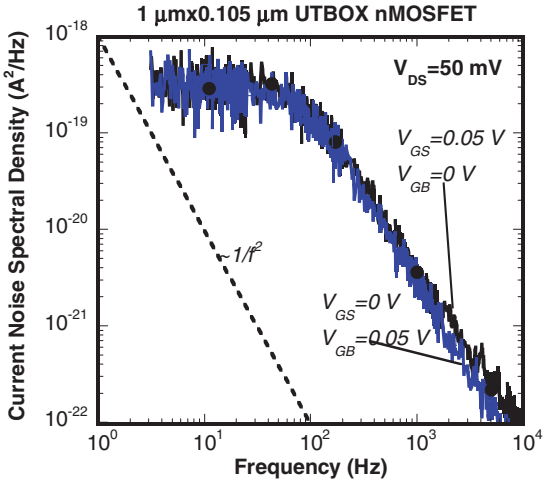

Figure 11. Low-frequency noise spectra for a UTBOX SOI nMOSFET, operated at the front-gate with the back-gate V_{GB} at 0 V or at the back-gate with the front-gate at 0 V.

Random Telegraph Noise and deep-level spectroscopy

From the extracted bulk trap concentrations typically in the range of 10^{15} cm^{-3},[28,37] it is clear that the GR noise in the silicon film is generated by only a handful of traps – similar as the retention time, with a similar activation energy.[7] It is well-known that if only a few traps are present in the gate oxide, the 1/f noise transforms into so-called Random Telegraph Noise (RTN), also giving rise to a Lorentzian spectrum.[11] A typical time domain measurement for an UTBOX SOI nMOSFET reveals the presence of some fast RTN-like switching in Fig. 10, with an amplitude of a few tenths of a percent and up and down times in the range of ~0.1 ms. The relative amplitude of the fast switching is of the same order of magnitude as the ratio of the trap density with respect to the average electron density in the fully depleted channel (~10^{18} cm^{-3}), derived from device simulations. Also the time constants agree well with typical corner frequencies of the Lorentzians associated with the GR noise of Figs 2, 5 or 11. The question arises: how to distinguish RTN due to oxide or border traps from GR noise in the silicon film?

It has recently been proposed that studying the noise in both the front- and back-channel enables to identify the different cases:[26,27] when a similar Lorentzian is present in both spectra, like in Fig. 11, one can assume that the traps are present in the silicon film. If on the contrary, the Lorentzian is only found in the front- or back-gate spectrum with the other channel accumulated, then one can conclude that the trap resides in the front- or back-gate oxide. An example of what corresponds most likely with an RTN in the front-gate oxide is illustrated by Fig. 12: while the front-channel noise spectra exhibit a dominant Lorentzian at low frequencies, the spectra are more 1/f-like for the back-channel. In each case, the opposite channel was biased in accumulation for this t_{Si} = 14 nm nMOSFET, so that the effect of the corresponding traps on the noise was fully screened. In this case, it is concluded that RTN in the front-oxide gives rise to this Lorentzian component.[27,36] Notice also the much higher amplitude of the noise PSD, confirming the role of RTN in enhancing the noise variability. In fact, in order to further clarify this issue, two-dimensional device simulations will be instructive to derive the front/back-gate and drain voltage dependence of the RTN and associated GR noise. It will also clarify whether the trap position in the silicon film, i.e., near the source or drain, in the middle of the silicon channel, near the front or back interface, will have an impact on the corresponding Lorentzian noise parameters and variability. Device simulations will become even more necessary for the identification of RTNs in ultra-thin film FD

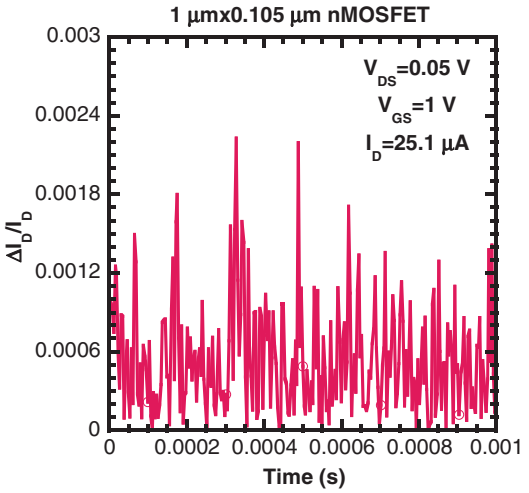

Figure 10. Time domain measurement of a 1 µm × 0.105 µm UTBOX SOI nMOSFET in linear operation at V_{GS} = 1 V and I_D = 25.1 mA. The back-gate is at 0 V.

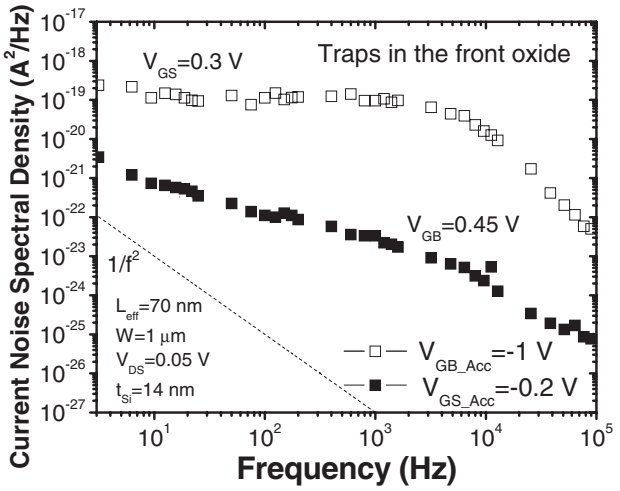

Figure 12. Current noise spectra measured with the back-channel in accumulation ($V_{GS,acc}$) or with the front-channel in accumulation ($V_{GB,,acc}$) for a L = 70 nm and t_{Si} = 14 nm FD SOI nMOSFET.

SOI transistors, where it is hard to bias the opposite interface in accumulation.

In order to obtain an idea of the activation energy of the responsible trap(s), the Lorentzian noise can for example be studied as a function of the temperature, as reported elsewhere for the devices under investigation.[28,33,46] Recent studies at cryogenic temperatures reveals the presence of several deep levels in the silicon film, which have a processing-induced character, i.e., some can be associated with implantation-related defects.[33] At the same time, the activation energy derived from temperature-dependent measurements is in good agreement with the data derived from the GR-noise spectroscopy method proposed in the previous section.[37] Moreover, the thermal activation of the retention time of the UTBOX nMOSFETs, operated as 1-transistor floating-body RAM memories, gives similar values, in the range of 0.3 to 0.5 eV, depending on the processing details.[7] In other words, GR noise spectroscopy of deep levels in the silicon film can be used to identify the traps responsible for the retention time in FBRAM devices. Moreover, also the radiation response of such devices will be sensitive to defects in the silicon film,[47] indicating that GR noise studies can also be very helpful in this context.

Conclusions

It has been demonstrated that the LF noise PSD of ultra-thin film FD UTBOX SOI nMOSFETs exhibits both flicker noise and Lorentzian noise components, in the front- and the back-channel spectra. The flicker noise can be generally ascribed to trapping in the gate dielectric, whereby the magnitude depends on the gate oxide quality and type (SiO_2, high-k). The origin of the Lorentzian noise can be assigned either to individual traps in the front- or back-gate dielectric or to defects residing in the fully depleted silicon film. This Lorentzian noise is the main origin of the wide sample-to-sample dispersion in the noise PSD of the studied devices. This may generally be extrapolated to other types of ultra-thin film or narrow-fin fully depleted architectures, like SOI or bulk FinFETs. Such Lorentzian components can be exploited to study the parameters of the deep levels in silicon or the gate oxide either by analyzing the gate-voltage or the temperature dependence. At the same time, such analysis reveals useful information for the understanding of the retention time in UTBOX 1T FBRAM devices.

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