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***Abstract*—DC and low frequency noise measurements on strained and unstrained n-channel FinFET transistors processed on silicon on insulator (SOI) substrates were performed at 10 K in order to evaluate the device performances and study the low frequency noise mechanisms. The main electrical parameters are investigated and compared to those found at room temperature. The low frequency noise analysis shows that at 10 K, the carrier number fluctuations dominate the flicker noise in weak inversion, while the access resistance noise contributions prevails in strong inversion.**

Keywords: FinFET, DC performances, low frequency noise, very low temperature operation

I. Introduction

The multi-gate FinFET has been considered as a promising structure for the future technology nodes, because the 3D geometry offers an improved control of the short-channel effects through a better electrostatic control of the gate over the conduction channel, allowing to achieve a higher I_{on}/I_{off} ratio, and providing an enhanced mobility due to the undoped channel [1-2]. However, the FinFETs still need to reach a higher I_{on} to meet the technology requirements. Strain engineering can further boost the device mobility without adding major process complexity [3-4].

Among all parameters that characterize these devices, the impact of the low frequency noise now plays a major role because its level increases continuously with the miniaturization. However, up to now, the noise behaviour in multi-gate n-channel FinFETs has never been investigated at 10 K.

This work is focused on a thorough characterization on unstrained and strained SOI n-channel FinFETs at very low temperature operation in terms of short channel effects and low frequency noise performances.

II. Devices and Experimental

A. Devices

The investigated devices are n-channel tri-gate FinFETs processed in a 32 nm technology with standard and strained SOI substrates. The gate oxide consists of a high-k dielectric (HfSiON) on top of a 1 nm interfacial SiO_2 resulting in an equivalent oxide thickness (EOT) of 1.5 nm. The metal gate consists of 10 nm TiN covered by 100 nm polysilicon. The devices have a fin width of 25 nm, fin height of 65 nm, 5 fins in parallel and a mask gate length (L_G) varying from 130 to 1000 nm. The tested devices are n-channel FinFETs on standard SOI substrates (SOI) and on biaxial globally strained substrates sSOI combined with uniaxial local strain by CESL (Contact Etch Stop Layers) and using SEG (Selective Epitaxial Growth) in the drain and source regions (sSOI + CESL +SEG).

B. Experimental

The DC and the low frequency noise measurements were performed directly at wafer-level using a Lakeshore TTP4 prober at 10 K and at room temperature. Static measurements were performed using an HP4156B semiconductor parameter analyser. In linear regime operation, the devices were biased with an applied drain voltage V_{DS} = 20 mV. In saturation regime, $I_D(V_{DS})$ measurements were performed for different applied gate voltage V_{GS} from 0.6 V up to 1 V.

The noise measurement set-up allows to bias the devices by choosing the V_{GS} and V_{DS} voltages, and also to measure the total dynamic resistance between drain and source r_T and the transconductance g_m by applying a small signal at the source and gate nodes, respectively. Drain current fluctuations are amplified and the noise spectral density is calculated using a FFT spectral analyser. Noise is reported at the input of the device by dividing by the square of the measured voltage gain

between the gate and the output and this for different applied gate voltages.

The linear regime operation measurements were performed for all available gate lengths. The saturation regime operation was investigated for all available gate lengths at room temperature, while at 10 K the measurements were focused only on three mask gate lengths of 130 nm, 250 nm and 700 nm. The low frequency noise measurements were focused only on two mask gate lengths (200 nm and 1000 nm).

III. Results and Discussion

A. Static measurements

Typical drain current $I_D(V_{GS})$ and transconductance $g_m(V_{GS})$ characteristics for a standard and strained n-channel FinFET at 10 K for various gate lengths are shown in Fig. 1(a) and (b). Good behavior is obtained and one can note that the benefit of the use of strain seems to be preserved at this cryogenic temperature.

In order to eliminate the effects of the mobility gate voltage dependence at very low temperature operation, as proposed in [5], an adapted function defined as $(I_D)^{2/3}/(g_m)^{1/3}$ was constructed. As expected, linear dependence of this function (noted Y_{10K}) with the applied gate voltage is observed (Fig. 2), allowing us, by following the technique described in [5] to extract at 10 K operation the main electrical parameters of the transistors. At room temperature operation the electrical parameters are extracted following the technique using the Y function proposed in [6].

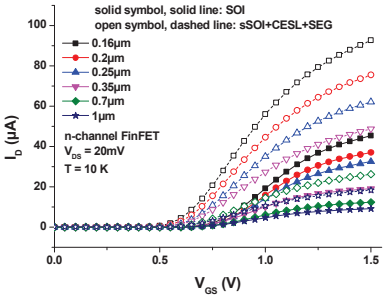
In Fig. 3 are plotted the extracted threshold voltage (V_t) for all the investigated mask gate lengths. Short channel effects are only slightly ameliorated with the temperature reduction: V_t(long-channel) – V_t(short-channel) for standard SOI devices is about 52 mV @ 300 K compared to 49 mV @ 10 K, while for strained ones it is about 67 mV @ 300 K compared to 53 mV @ 10 K. Moreover, by reducing the temperature, the shift of the threshold voltage V_t(300 K) - V_t(10 K) for the SOI devices is about 110 mV for L_G = 1000 nm and 93 mV for L_G = 160 nm, while in sSOI device it is about 41 mV for L_G = 1000 nm and 35 mV for L_G = 160 nm, resulting in a lower threshold voltage for the strained channels at 10 K. These threshold voltage shift values are lower than expected by the reduction of the temperature from 300 K down to 10 K (i.e. about 165 mV [7]). This could be related to the temperature behaviour of the Fermi level and of the surface potential at very low temperatures which are caused primarily by the temperature dependence of the intrinsic carrier concentration.

As provided by the extraction techniques, the low field mobility can be estimated at room temperature, while at 10 K it is the maximum of the effective mobility (see Table 1). As expected, a boost in the extracted low field mobility is observed for the strained devices at room temperature. At 10 K, due to reduced phonon scattering, an enhanced mobility is expected. By reducing the temperature from 300 K to 10 K, one observes that the increase of the mobility is more pronounced for standard devices compared to the strained ones. This trend can be justified by a more pronounced impact of the surface roughness mechanism in strained devices at this cryogenic temperature.

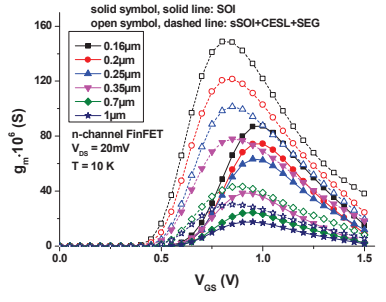
One of the problems related with the use of narrow nFinFETs is the increase of the parasitic series resistance. The access resistance and the difference between mask and effective gate length ($\Delta L = L_m - L_{eff}$) are extracted following the total resistance technique described in [8]. Compared with standard devices, the introduction of SEG allows to obtain a significant reduction of the access resistance of about 60% at room temperature and of about 50% at 10 K. For a given temperature, the obtained values of ΔL are quite similar for standard and strained devices. This suggests that the charge sharing effect is not significantly affected by the use of the strain. However, as expected, amelioration is observed at very low temperature operation.

	SOI		**sSOI+CESL+SEG**	
	10 K	**300 K**	**10 K**	**300 K**
μ (cm^2/Vs)	490	220	653	530
R_{access} (Ω)	178	210	84	123
ΔL (nm)	18	54	22	49

TABLE 1. Summary of the extracted values for the mobility, access resistance and ΔL at room and 10 K operation.



a)



b)

Figure 1. Typical $I_D(V_{GS})$ and $g_m(V_{GS})$ characteristics for various gate lengths at 10 K.

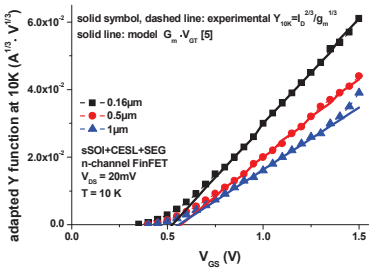


Figure 2. Typical $Y_{10K}(V_{GS})$ characteristics for various gate length at 10 K

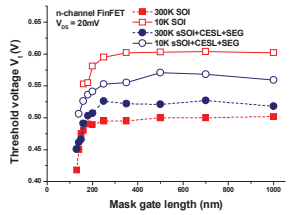


Figure 3. Extracted threshold voltage at 10 K and room temperature

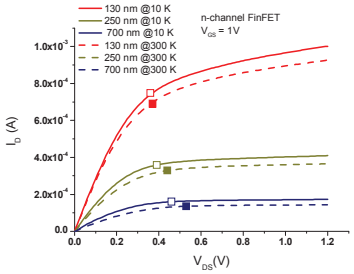


Figure 4. Typical $I_D(V_{DS})$ characteristics for various gate lengths at 10 K and 300 K

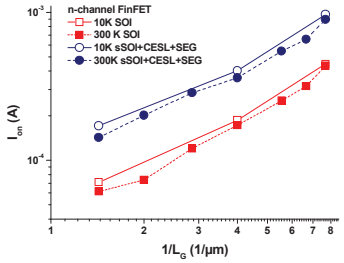


Figure 5. I_{on} versus the mask gate length at 10 K and 300 K

Fig. 4 shows typical drain current $I_D(V_{DS})$ characteristics for a fixed applied gate voltages of 1 V and for different channel mask gate lengths at the two investigated temperatures. Reducing temperature leads to a slight increase of the saturation drain current I_{Dsat} and a small reduction of the saturation voltage V_{Dsat}. The I_{on} currents, defined as $I_{on} = I_{DS}$ @ $V_{DS} = V_{GS} = 1V$ are plotted in Fig. 5. It is worth noting that I_{on} is higher in strained devices compared to standard ones. A temperature reduction leads to an enhancement of the I_{on} current. This increase is more pronounced for short-channel transistors (about 17 - 20%) compared to long channel transistors (about 8 - 10%) for both structures.

The drift velocity can be defined as $v_d = g_m/(W\ C_{ox})$. This drift velocity increases with the drain voltage and reaches a maximum at high electric field. For an applied drain voltage higher than the saturation voltage, this maximum is weakly dependent on the applied gate bias. The extracted values corrected by access resistance influence are shown in Fig. 6. As expected from theory, v_d is found to vary as the inverse of the channel length even for the short devices due to prevailing mobility limited transport. The use of strain leads to enhanced values of the saturation velocity. Therefore, reducing temperature increases the drift velocity for both devices due to the reduced phonon scattering contribution. It may be noted that at 10 K, the estimated drift velocity for the short – channel strained devices (about $10.9 \cdot 10^6$ cm·s^{-1} for $L_G = 130$ nm) is very close to the value of the non-stationary regime at this temperature (i.e. $13.2 \cdot 10^6$ cm·s^{-1} [9]).

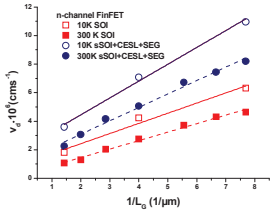


Figure 6. Intrinsic drift velocity versus gate length at 10 K and 300 K.

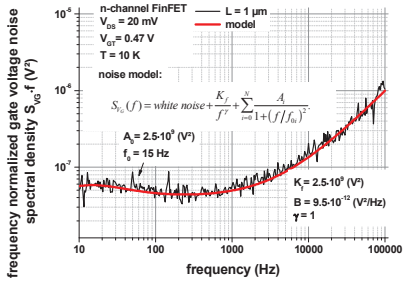


Figure 7. Comparison between noise measurement and model using inset equation. In this example, 1/f noise, white noise and one Lorentzian contribution were used to obtain the best adjustment between the model and the measurement.

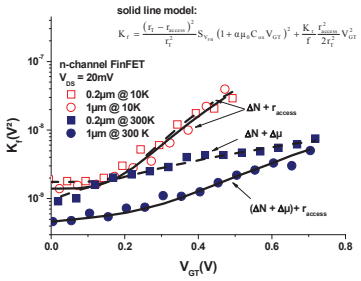


Figure 8. The extracted $K_f(V_{GT})$ for the standard device for two channel lengths at 10 K and 300 K.

B. Low frequency noise

In Fig. 7 is represented an example of the frequency normalized gate voltage noise spectral density at 10 K. The total noise can be perfectly modelled by considering three uncorrelated noise sources: white noise, 1/f and Lorentzian noise (see equation in the inset of Fig. 7), and each contribution can be identified. The extracted 1/f noise level (K_f) variations with the applied gate voltage overdrive ($V_{GT} = V_{GS} - V_t$) are illustrated in Fig. 8 for two mask gate lengths of the standard devices at the two investigated temperatures.

At room temperature, the 1/f noise behaviour was already discussed in [10] and attributed to carrier number fluctuations due to carrier trapping in the oxide layer. At 10 K operation, the extracted 1/f noise level is found to be independent on the variations of the applied gate overdrive in weak inversion. This suggests that carrier number fluctuations dominate the 1/f noise [11] even at this cryogenic temperature. The increase of the noise in strong inversion can be modelled by taking into account only parasitic access resistance contributions for both investigated channel lengths. The solid line in Fig. 8 represents the 1/f noise model which takes into account carrier number fluctuation and parasitic access resistance contributions (see equation in the inset of Figure 8).

	T (K)	L (µm)	$S_{VFB}\cdot10^{-9}$ (V^2/Hz)	$K_r\cdot10^{-5}$	$\alpha\cdot10^4$ (Vs/C)	$N_{it}\cdot10^{17}$ ($cm^{-3}eV^{-1}$)
SOI	10 K	0.2	1.75	1.5		610
		1	1.25	18		2630
	300K	0.2	0.96	0	0.5	11
		1	0.45	6.5	0.14	29

TABLE 2. Summary of the extracted noise parameters for standard devices at 10 K and 300 K.

In Table 2 are summarized the main extracted noise parameters. It was already reported that reducing the temperature can lead to enhanced noise levels in n-MOSFETs [12]. An increase of the flat-band noise level is observed in our devices with temperature reduction from 300 K down to 10 K. This increase is more important for the long - channel devices (a factor of about 2.7) compared to short - channel ones (a factor of about 1.8).

The impact of the carrier number fluctuations correlated to mobility fluctuations are observed only at room temperature. The estimated values of the scattering coefficient suggest that the $\Delta N + \Delta\mu$ noise mechanism is more important in short-channel devices. However, they are lower than typical values reported for planar bulk n-channel transistors (i.e. 10^4 Vs/C).

The relatively small values of the slow insulator trap density are a good indication of the quality of the oxidation process despite the using of high-k dielectrics in such advanced devices. At 10 K, the increase of the trap densities is observed, this trend was already reported [12] and can be justified by models which take into account the structure of the high-k dielectric stack considering two tunnelling barriers through the dielectric, corresponding to the interfacial layer and to the high-k layer, respectively.

IV. CONCLUSION

Good I-V characteristics were evidenced even at 10 K. Better behaviour of the strained devices has been observed for many electrical parameters at 10 K operation: lower threshold voltage, smaller access resistance, higher carrier mobility, higher I_{on} current and higher saturation drift velocity. For short-channel strained devices, the values of the saturation velocity are very close to those of the non-stationary regime. The use of strain seems to have no significant impact on the charge sharing effect. However, the benefit of the strain engineering is maintained at this cryogenic temperature.

The carrier number fluctuations dominate the 1/f noise also at very low temperature. The correlated mobility fluctuations contributions were not observed at 10 K. In strong inversion, more impact of the access resistance noise contribution to the total 1/f noise is found at 10 K. The quality of the oxidation process was proved by the small values of the oxide trap density.

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