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► **To cite this version:**

Rachida Talmat, H. Achour, Bogdan Cretu, Jean-Marc Routoure, A. Benfdila, et al.. Low frequency noise characterization in n-channel FinFETs. Solid-State Electronics, 2012, p20-26. hal-00994184

**HAL Id: hal-00994184**

**<https://hal.science/hal-00994184>**

Submitted on 21 Jul 2014

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# Low frequency noise characterization in n-channel FinFETs

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## ABSTRACT

In this paper, the low frequency noise was studied from 100 K up to room temperature in n-channel triple-gate FinFET transistors fabricated on silicon on insulator (SOI) substrates. It was found that the noise spectra contain  $1/f$  and Lorentzian components, which can be analyzed using the standpoint of the number fluctuation by generation–recombination of carriers due to traps that can be located either at the gate oxide/Si film interface or in the silicon depletion film. The variations of the low frequency noise versus temperature allow to evaluate the quality of the gate oxide interface, to identify traps in the silicon film and to make a correlation between the observed traps and some technological steps. Moreover, some additional process steps used to boost the device performances seem to increase the trap densities in the film with no significant impact at the gate oxide/Si film interface.

### Keywords:

FinFET  
SOI  
Strain  
Low frequency noise  
Lorentzian  
Temperature

## 1. Introduction

The continuous evolution of semiconductor devices to smaller dimensions causes a degradation of the signal-to-noise ratio. The low frequency noise is becoming a major concern for the scaled down devices, due to its inverse dependence with the gate area and it could lead to serious limitations of the functionality of the analog and even digital circuits [1–13]. According to the ITRS roadmap for 2020 [1], the RF and analog/mixed-signal CMOS technology requirement for low-stand-by-power devices provide a gate length of 11 nm and a noise level of  $30 \mu\text{V}^2 \mu\text{m}^2/\text{Hz}$ . Such advanced technologies, in order to improve the performance require layers/films or interfaces of semiconductors and insulators with increasingly high-quality. Moreover, the improvement in the quality of materials is not always in agreement with the evolution of device down-scaling.

An important aspect of assessing the material quality and device reliability is the use of fast, non-destructive and accurate electrical characterization techniques to determine the important transistor parameters. Due to its sensitivity to defects and imperfections in the current path, the low frequency noise has been proposed as a good tool for predicting device quality or reliability, both from an application and process optimization viewpoint [2–11]. The low frequency noise measurements versus temperature can be used as a non-destructive device characterization tool

in order to evaluate the quality of the gate oxide interface and to identify the traps in the depletion area of the transistors. One of the methods used for material characterization is provided by the study of the generation–recombination (GR) noise, corresponding to a Lorentzian type of spectra and allowing to do the so-called noise spectroscopy when performed as a function of temperature [12,13].

The multiple-gate FinFET transistors on an SOI substrate are considered as promising candidates for future technology nodes, due to the better control of the short channel effects by the 3D geometry, the low leakage current, and the higher mobility due to the undoped channel [14–17]. Strain engineering can further boost the device performances without adding major process complexity [18–23].

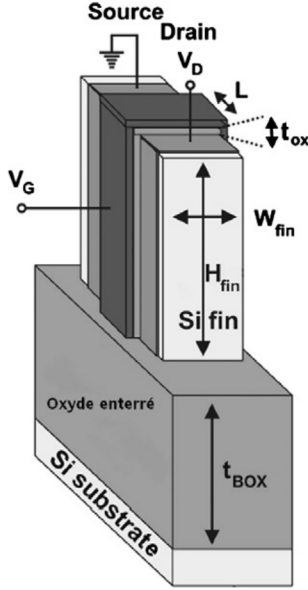
The aim of this work is to investigate the low frequency excess noise sources ( $1/f$  and Lorentzian spectra) versus temperature as a diagnostic tool to characterize the traps present at the gate oxide/Si film interface and in the depletion film of advanced n-channel FinFETs.

## 2. Experimental

The tested devices were n-channel tri-gate FinFETs. They have been processed in 32 nm technologies on standard and strained SOI substrates. The biaxial global strain (sSOI), where the stress is introduced across the whole wafer by epitaxial growth of a SiGe “buffer layer”, and the uniaxial local strain, based on the use of compressively strained (for p-channels) or tensile (for n-channels)

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**Fig. 1.** Schematic representation of the main geometrical dimensions (the gate length  $L$ , the fin-height  $H_{fin}$  and the fin-width  $W_{fin}$ ) of the FinFET structure (modified figure from Rafi JM, et al. Solid-State Electron 2007; 51: 1201–10).

across the gate stack, referred to as contact etch stop layers (CESL) will give a stress along the channel and boost up the carrier mobility. The integration of SiGe in the source and the drain regions, realized by selective epitaxial growth (SEG), leads to a reduction of the access resistances [18–23].

Fig. 1 are represented the main geometrical dimensions of the FinFET structure. The gate oxide of the tested devices consists of a high-k dielectric (HfSiON) on top of a 1 nm interfacial SiO<sub>2</sub>, resulting in an equivalent oxide thickness (EOT) of 1.5 nm. The metal gate consists of 10 nm TiN covered by 100 nm polysilicon. The physical gate lengths studied were from 60 nm to 910 nm with a fin-height of 65 nm, fin-width of 25 nm and five fins in parallel. Further processing details can be found in [24].

The low frequency noise measurements were performed directly on wafer-level using a “Lakeshore TTP4” prober from 100 K up to room temperature. The devices were biased in the linear regime with an applied drain voltage  $V_{DS} = 50$  mV. The measurement set-up allows to measure the total dynamic resistance between drain and source  $r_T$  (the small signal output resistance) defined as  $(r_T)^{-1} = \frac{\partial I_D}{\partial V_{DS}} \Big|_{V_{GS}=\text{const.}}$ .

The noise measurements were performed as a function of the gate voltage  $V_{GS}$  and at fixed drain current (the gate voltage was adjusted in order to keep the drain current constant at  $I_D = 1 \mu\text{A}$ ) over the whole temperature range using a step of 10 K.

### 3. Noise model

In general, the low frequency noise observed in devices can contain a combination of three noise sources: white noise, flicker noise ( $K_f/f^\gamma$ ) and Lorentzian noise. The following equation enables to model the frequency dependence of the noise spectral density at the input:

$$S_{V_G}(f) = B + \frac{K_f}{f^\gamma} + \sum_{i=0}^N \frac{A_i}{1 + \left(\frac{f}{f_{0i}}\right)^2} \quad (1)$$

where  $B$  presents the white noise level,  $K_f/f^\gamma$  presents the flicker noise (the frequency exponent  $\gamma$  may deviate from one if the trap density is not uniform in depth), and the third term of the equation

presents a sum of Lorentzian components, with  $A_i$  the plateau value and  $f_{0i}$  the characteristic frequency.

As shown in Fig. 2, the noise spectra in the studied devices contain a combination of these three noise sources and can be perfectly modeled by Eq. (1).

The evolution of  $K_f$ ,  $A_i$  and  $f_{0i}$  versus the applied gate voltage overdrive  $V_{GT} = V_{GS} - V_{th}$  has been investigated for all structures, where  $V_{th}$  is the threshold voltage. It was found that the noise behaviors can be analyzed using the point of view of the number fluctuations by generation recombination of carrier due to traps that can be located either at the gate oxide/Si film interface or in the depletion Si film.

For generation–recombination phenomena, the noise spectral density of carrier number fluctuations  $dS_N(f)$  for a trap of energy  $E_T$ , with a trap density  $N_T$  in the case of a single time constant  $\tau$  in an elementary surface  $dS$  is described by the formula [25,26]:

$$dS_N(f) = N_T(E_T) f_i(E_T) [1 - f_i(E_T)] \frac{4\tau}{1 + (2\pi f \tau)^2} \quad (2)$$

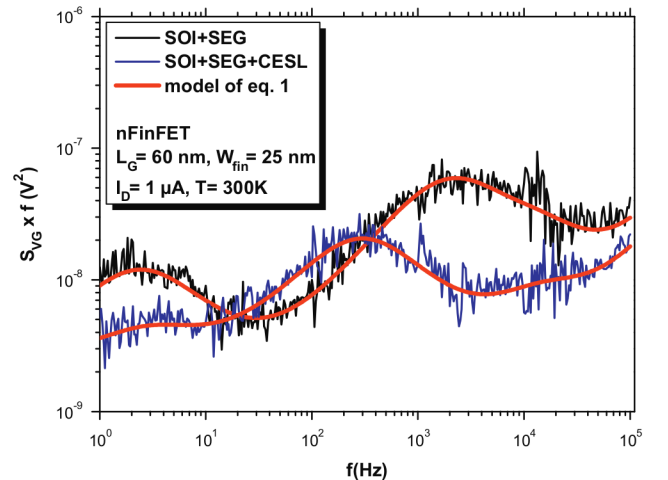
#### 3.1. Carrier number fluctuation 1/f model

The physical mechanism behind the number fluctuations 1/f noise in MOSFET is the variation of the interfacial oxide charge after dynamic trapping and detrapping of free carriers into slow oxide traps which lead to fluctuations in the surface potential, giving rise to fluctuations in the inversion charge density. The fluctuations in the interfacial oxide charge density are equivalent to a variation in the flat-band voltage  $\delta V_{FB} = -\delta Q_{it}/(WLC_{ox})$ .

Considering that the trapping and detrapping occurs through tunneling processes; and assuming that the trapping time constant is given as  $\tau = 10^{-10} e^{z/\lambda}$ , where  $\lambda$  is predicted by the Wentzel–Kramers–Brillouin (WKB) theory [27] as  $\approx 1 \text{ \AA}$  for a Si/SiO<sub>2</sub> interface, from Eq. (2) one can derive the McWhorter model [27,28]:

$$S_{V_{FB}} = \frac{q^2 k T \lambda N_{it}}{f^\gamma W L C_{ox}^2} \quad (3)$$

where  $k$  is the Boltzmann constant,  $T$  is the temperature,  $C_{ox}$  is the gate oxide capacitance,  $N_{it}$  is the density of traps in the gate dielectrics at the quasi-Fermi level ( $\text{cm}^{-3} \text{eV}^{-1}$ ) since only these traps contribute to the fluctuations (due to the factor  $f_i(E_T)[1 - f_i(E_T)]$  in Eq. (2), with  $f_i(E_T)$  the Fermi–Dirac occupation function). The McWhorter



**Fig. 2.** Example of typical low frequency noise spectra normalized by the frequency in n-channel FinFETs at 300 K. All the measurements in this paper have been fitted using Eq. (1).

theory predicts that the input noise spectral density does not depend on the gate voltage.

A general expression of the input gate voltage noise that can be derived without any necessary assumptions about the exact mechanism behind the fluctuations in the flat-band voltage and which takes into account the supplementary mobility change  $\delta\mu_{eff}$  due to the modulation of the scattering rate induced by the interface charge fluctuations is described by the formula [29,30]:

$$S_{V_G} = S_{V_{FB}} \left( 1 + \alpha \mu_{eff} C_{ox} \frac{I_D}{g_m} \right)^2 \quad (4)$$

where  $g_m$  is the transconductance,  $\mu_{eff}$  is the effective mobility,  $\alpha$  is the Coulomb scattering coefficient ( $\approx 10^4$  V s/C for electrons).

Considering uncorrelated noise sources in the channel and the source/drain regions, the impact of the access resistances on the low frequency noise can simply be obtained by adding to the channel noise the contribution of the excess noise originating from the access region. Based on the small-signal model of the transistor the expression of the total noise spectral density can be expressed as in Eq. (15) of Ref. [10]. It can be easily demonstrates that in linear region of operation, assuming that the drain and source access regions are symmetrical, we obtain for the total drain current noise spectral density the simplified equation:

$$(r_T)^2 S_{I_D} = (r_T - r_{access})^2 (S_{I_D})_{channel} + 2 \left( \frac{r_{access}}{2} \right)^2 (S_{I_D})_{access \ resistance} \quad (5)$$

where  $r_{access}$  is the dynamic access resistance and  $r_T$  is the dynamic total resistance between source and drain.

The noise of the access resistance can be modeled by  $(S_{I_D})_{access \ resistance} = \frac{K_f}{f} I_D^2$  [31]. In the linear region operation, we obtain for the total gate voltage spectral density:

$$S_{V_G} = \frac{(r_T - r_{access})^2}{r_T^2} S_{V_{FB}} (1 + \alpha \mu_0 C_{ox} V_{GT})^2 + \frac{K_f}{f} \frac{r_{access}^2}{2r_T^2} \frac{I_D^2}{g_m^2} \quad (6)$$

Assuming that in linear region, in first approximation  $\frac{\partial I_D}{\partial V_{GS}} \approx \frac{I_D}{V_{GS}}$  and  $g_m = \frac{\partial I_D}{\partial V_{GS}} \approx \frac{I_D}{V_{GS}}$ , the second term of Eq. (6), which expresses the access resistance contributions on the total noise, shows a dependence on  $\sim (V_{GT})^4$ , while the first term, which express the channel contribution on the total noise, shows a quadratic dependence with the applied gate overdrive.

### 3.2. Lorentzian model

In general, the Lorentzian component of the noise spectra can originate from traps located in the dielectric, at the interface dielectric/semiconductor or in the depletion zone. In small areas devices ( $< 1 \mu m^2$ ) random telegraphic signals (RTS), which are commonly attributed to individual carrier trapping at the silicon-oxide interface, can be observed. In this work, we will focus only on traps in the depletion region which, according to the theory developed in [9], give rise to Lorentzian for which the characteristic frequency does not change with the applied gate voltage.

The spectral density of the carrier number fluctuations due to a trap characterized by its relaxation time constant  $\tau$  can be obtained from Eq. (2):

$$S_N(f) = \frac{\tau N_{eff}}{1 + (2\pi f \tau)^2} WL, \quad (7)$$

where  $N_{eff} = BN_t W_d$ , with  $B$  a coefficient estimated to be  $1/3$  [32,33],  $N_t$  is the density of the trap;  $W_d = \sqrt{4\epsilon_0 \epsilon_{Si} kT \ln(N_A/n_i)/(q^2 N_A)}$  is the silicon film depletion depth,  $n_i$  is the intrinsic carrier density,  $N_A$  is the silicon film doping concentration,  $\epsilon_0$  is the permittivity of vacuum and  $\epsilon_{Si}$  is the relative silicon permittivity. In the linear operation regime, the drain current is proportional to the number of

carriers; one finally obtains for the gate voltage spectral density [32]:

$$S_{V_{GAT}}(f) = \frac{q^2 W_d N_T \tau}{3WLC_{ox}^2} \frac{1}{1 + (2\pi f \tau)^2} \quad (8)$$

For each Lorentzian characterized by its plateau level  $A_i$  (defined as  $A_i = \frac{q^2 N_{eff}}{WLC_{ox}^2}$ ,  $\tau = \frac{q^2 W_d N_T}{3WLC_{ox}^2} \tau$ ) and its characteristic frequency  $f_{oi}$ , one can associate a trap density  $N_T$  of time constant  $\tau$  ( $\tau$  defined as  $1/(2\pi f_{oi})$ ).

The variation of the characteristic frequency  $f_{oi}$  as a function of the temperature allows to plot an Arrhenius diagram; according to [12] one can write:

$$\ln(\tau T^2) = \frac{E_C - E_T}{kT} + \ln \left( \frac{h^3}{4k\sigma_n \sqrt{6\pi^3 M_c m_e^{1/2} m_h^{3/2}}} \right), \quad (9)$$

where  $h$  is the Planck constant;  $m_e^*$ ,  $m_h^*$  are the effective mass of electrons and holes respectively and  $M_c$  is the number of conduction band energy minima.

From the slope and the y-intercept of the evolution of  $\ln(\tau T^2)$  versus  $1/(kT)$  one can extract the energy difference between the appropriate band energy and the trap energy (i.e.  $\Delta E = E_C - E_T$ ) and the capture cross section  $\sigma_n$  of the trap, respectively. The physical nature of these traps can be identified by comparing the energy and capture cross section of the traps with data in the literature.

## 4. Results and discussion

### 4.1. 1/f noise

The extracted  $K_f$  level is found independent of the applied gate voltage overdrive  $V_{GT} = V_{GS} - V_{th}$  in weak inversion for standard devices on an SOI substrate, as illustrated in Fig. 3. This suggests that carrier number fluctuations due to carrier trapping in the oxide layer dominate the 1/f noise in weak inversion.

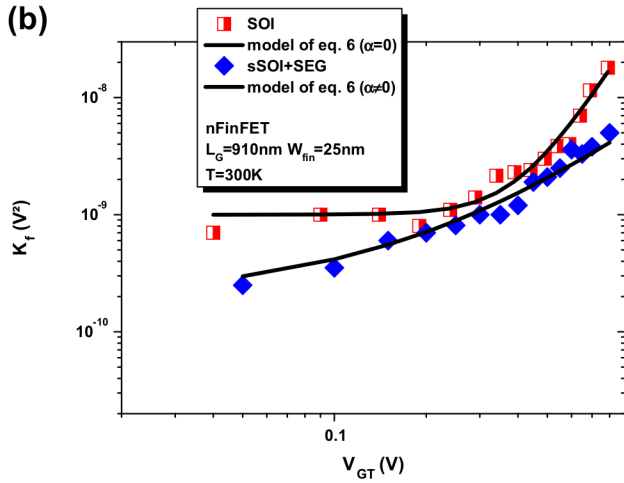
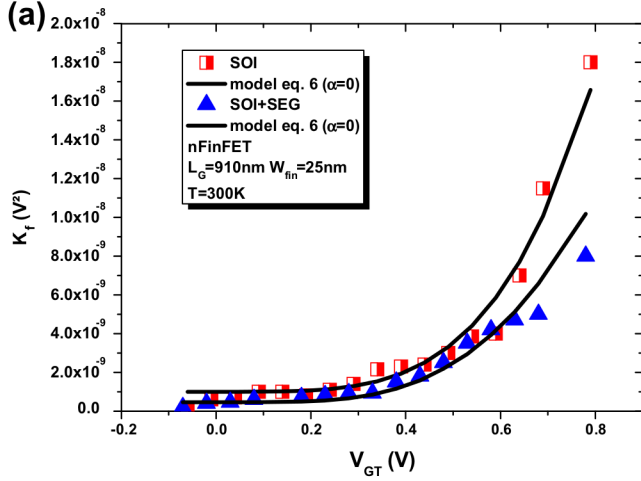
The increase of the noise from weak to strong inversion may be related to the carrier number fluctuations correlated to mobility fluctuations (dependency on  $(1 + \alpha \mu_0 C_{ox} V_{GT})^2$ ) and to the parasitic access resistances of the devices (dependency on  $I_D^2/(g_m^2 r_T^2)$ ). The access resistance contribution to the 1/f noise explains the behavior in strong inversion in standard SOI substrates (Fig. 3a). We can notice that the use of SEG leads to a reduction of the access resistance contribution on the 1/f noise in strong inversion.

A reduction of the 1/f low frequency noise level is observed in studied devices with sSOI substrates compared to standard SOI substrates (as shown in Fig. 3b). This is in agreement with other observation: a reduction with a factor of two of the 1/f noise level was reported for thermal Si/SiO<sub>2</sub> interfaces in sSi bulk MOSFET compared to devices with a standard substrate [34].

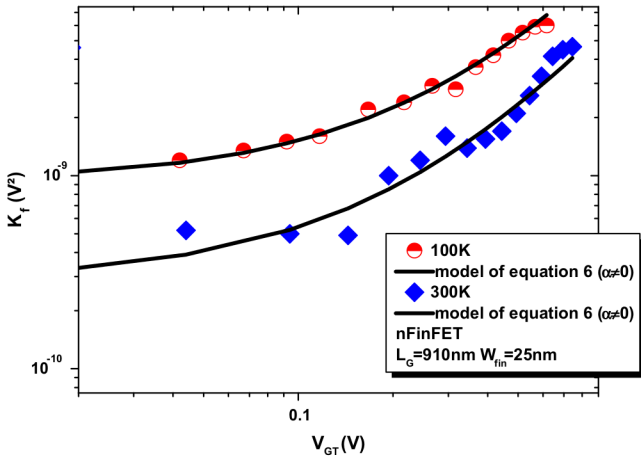
For devices with sSOI substrate, taking into account only the access resistance contribution is not sufficient to model the 1/f noise level evolution. Assuming also the carrier number fluctuations correlated to mobility fluctuations contribution, the model described in Eq. (5) can perfectly model the  $K_f$  evolution versus the gate bias for all temperatures and all investigated devices as shown in Figs. 3b and 4.

The Coulomb scattering coefficient  $\alpha$  is found between  $(0.45 - 0.8) \times 10^4$  V s/C at room temperature for all devices where the carrier number fluctuations correlated to mobility fluctuations are observed. These values are lower than for the pure SiO<sub>2</sub> dielectric (i.e.  $10^4$  V s/C). A reduction of  $\alpha$  was already reported for devices with HfO<sub>2</sub> gate dielectric [35,36]. It could be related to the deeper trap location in the HfSiON dielectric, resulting in a more remote behavior of the Coulomb scattering, leading to a smaller value of the Coulomb scattering coefficient.





**Fig. 3.** Gate voltage frequency normalized  $1/f$  noise level versus the applied gate overdrive at 300 K for different FinFET structures. (a) SOI and SOI + SEG and (b) SOI and SOI + SEG. Carrier number fluctuations correlated to mobility fluctuations have to be taken into account for sSOI + SEG devices.



**Fig. 4.** Gate voltage frequency normalized  $1/f$  noise level versus the applied gate overdrive at two different temperatures for sSOI + SEG + CESL nFinFET. Carrier number fluctuations correlated to mobility fluctuations have to be taken into account for sSOI + SEG + CESL devices.

The access resistance contribution is reduced at low temperature operation. However, as shown in Fig. 4 for sSOI + SEG + CESL

devices, an unexpected increase of the  $K_f$  noise level can be observed in intermediate biases and low temperature operation. This evolution can be modeled only considering an increase of the contribution to the total noise of the number fluctuations correlated to mobility fluctuations. An increase of  $\alpha$  from  $0.45 \times 10^4$  V s/C at room temperature to  $0.6 \times 10^4$  V s/C at 100 K allows to fulfill the evolution of the  $K_f$  noise level for sSOI + SEG + CESL devices (Fig. 4). At low temperature operation the inversion layer may be more confined at the interface, leading to more effective scattering by charged centers in the oxide (closer to the interfacial SiO<sub>2</sub> layer) and this may lead to a slightly increase of the Coulomb scattering coefficient.

The trap density  $N_{it}$  was extracted from the  $1/f$  noise contribution in flatband operation, using classical expression of Eq. (3). The results obtained at 300 K are summarized in Table 1. We can notice that the obtained values are lower than those found in FinFETs with a HfO<sub>2</sub> gate oxide at room temperature [37,38]. The

**Table 1**

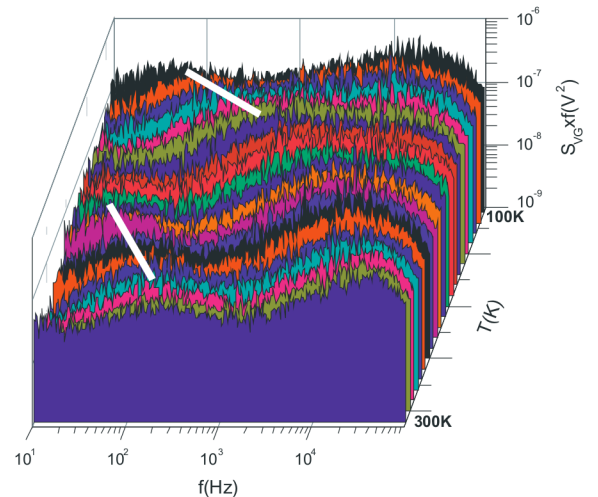
$N_{it}$  trap density extracted from the  $1/f$  noise contribution in flatband operation at 300 K.

Structures	$N_{it}$ (cm <sup>-3</sup> eV <sup>-1</sup> )
SOI	$2.7 \times 10^{18}$
SOI + SEG	$2.4 \times 10^{18}$
SOI + SEG + CESL	$1.7 \times 10^{18}$
sSOI	$1.5 \times 10^{18}$
sSOI + SEG	$1.1 \times 10^{18}$
sSOI + CESL	$1.3 \times 10^{18}$
sSOI + SEG + CESL	$1.2 \times 10^{18}$

**Table 2**

$N_{it}$  trap density extracted from the  $1/f$  noise contribution in flatband operation at different temperatures for sSOI + SEG + CESL FinFET.

sSOI + SEG + CESL	$N_{it}$ (cm <sup>-3</sup> eV <sup>-1</sup> )
300 K	$1.2 \times 10^{18}$
160 K	$3.1 \times 10^{18}$
100 K	$6.5 \times 10^{18}$



**Fig. 5.** Gate voltage frequency normalized noise spectral density versus temperature for a sSOI + SEG FinFET with physical gate length of 60 nm. The white lines represent examples of the temperature variation of Lorentzians characteristic frequency assigned to traps located in the depletion film.

relatively small values of the oxide trap density are a good indication of the quality of the HfSiON and can be related to the hafnium oxide nitridation which can prevent the penetration of dopants in the oxide as proved in previous observations in planar transistors [39].

One can note that the  $N_{it}$  values increase with the temperature decreases, as showed for example by Table 2 for an sSOI + SEG + -CESL device. In the model developed in [40,41], based on the one detailed in Ref. [29], are taken into account the structure of the high-k dielectric stack considering two tunneling barriers through the dielectric, corresponding to the interfacial layer and to the high-k layer, respectively. As the time constant of traps depends on the depth and on the tunnel parameter, it must be modeled differently in the two considered layers. The density of traps, typically taken uniform in space and in energy, is replaced in this model by an exponential dependence on the position in energy with a spatial distribution of traps in the high-k layer. This model could allow us to explain the observed variations of the  $N_{it}$  as a function of temperature in the studied devices.

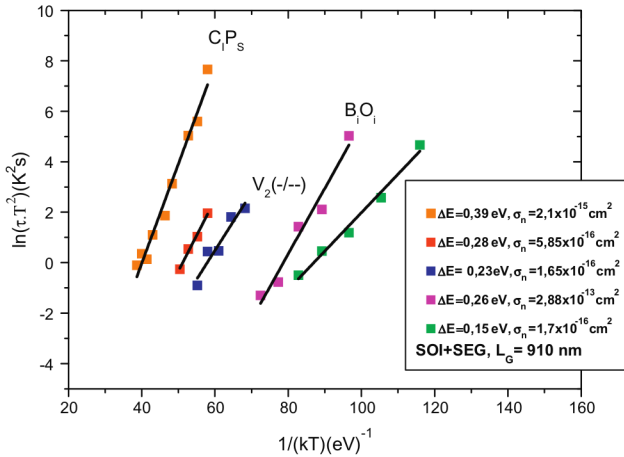


Fig. 6. Example of an Arrhenius plot for an SOI + SEG nFinFET with physical gate length of 910 nm.

Table 3

The identified traps for all studied devices; the gray line indicate the structures that are processed with a SiC liner.

n-channel structures	$V_2(0/-)$	$V_2(-/-)$	H1	$B_iO_i$	$C_iP_s(0/-)$	D1	D2	D4	D5	D7	D8	D9	D10
S0		xX		X	xX				x	x	xX	x	x
S1	xX	X			X			X	x		X	x	
S2	X		x	X	X			X		X	x	x	X
S3		xX	x	X	x	X		x	X	X	xX		
S4		X	x		X			X	xX	xX	xX	xX	x
S5		x	X	X						X	x		X
S6	x	x		x		xX	xX			X	x	x	X

D1:  $\Delta E = 0.5$  eV,  $\sigma_n = 1.3 \times 10^{-15}$  cm<sup>2</sup>.

D2:  $\Delta E = 0.4$  eV,  $\sigma_n = 9.5 \times 10^{-17}$  cm<sup>2</sup>.

D4:  $\Delta E = 0.29$  eV,  $\sigma_n = 2 \times 10^{-17}$  cm<sup>2</sup>.

D5:  $\Delta E = 0.29$  eV,  $\sigma_n = 1.8 \times 10^{-19}$  cm<sup>2</sup>.

D7:  $\Delta E = 0.23$  eV,  $\sigma_n = 1.8 \times 10^{-17}$  cm<sup>2</sup>.

D8:  $\Delta E = 0.19$  eV,  $\sigma_n = 7.9 \times 10^{-18}$  cm<sup>2</sup>.

D9:  $\Delta E = 0.15$  eV,  $\sigma_n = 2.1 \times 10^{-18}$  cm<sup>2</sup>.

D10:  $\Delta E = 0.2$  eV,  $\sigma_n = 1.8 \times 10^{-15}$  cm<sup>2</sup>.

$V_2(0/-)$ :  $\Delta E = 0.42$  eV,  $\sigma_n = 10^{-15}$  cm<sup>2</sup>.

$V_2(-/-)$ :  $\Delta E = 0.23$  eV,  $\sigma_n = 10^{-15}$ - $10^{-16}$  cm<sup>2</sup>.

$B_iO_i$ :  $\Delta E = 0.26$  eV,  $\sigma_n = 10^{-13}$ - $10^{-14}$  cm<sup>2</sup>.

H1:  $\Delta E = 0.32$  eV,  $\sigma_n = 10^{-15}$  cm<sup>2</sup>.

$C_iP_s(0/-)$ :  $\Delta E = 0.38$  eV,  $\sigma_n = 10^{-15}$  cm<sup>2</sup>.

S0: SOI; S1: SOI + SEG, S2: SOI + SEG + CESL, S3: sSOI, S4: sSOI + SEG, S5: sSOI + CESL S6: sSOI + SEG + CESL.

x: found in  $L_G = 60$  nm; X: found in  $L_G = 910$  nm.

## 4.2. Lorentzian spectra

Fig. 5 illustrates an example of the frequency normalized noise spectral density versus the temperature. Our study focuses on Lorentzians originating from traps in the film depletion region. According to [9], if the characteristic frequency of a Lorentzian does not change with the applied gate voltage, this Lorentzian can be assigned to a trap located in the depletion film. In this case the characteristic frequency should vary with the temperature. Only Lorentzians which satisfy these two conditions were taken into account.

For each Lorentzian originating from traps in the depletion area, the characteristic frequency  $f_{oi}$  and of the plateau value  $A_i$  were extracted using the model of Eq. (1). A typical Arrhenius diagram is presented in Fig. 6. In this example, three kinds of traps can be clearly identified for the SOI + SEG device.

For all the investigated n-channel technologies, five kinds of traps were identified: divacancies  $V_2(0/-)$  and  $V_2(-/-)$ , traps related to hydrogen (noted H1), interstitial boron–interstitial–oxygen complex ( $B_iO_i$ ) and interstitial carbon–substitutional-phosphor complex ( $C_iP_s$ ). In addition to these, almost 10 kinds of unknown traps have been frequently observed. The identified traps for all studied devices are summarized in Table 3. One can notice that there are a number of traps which are frequently found but which are not reported in the literature. Most likely, they may originate from the dry-etching or implantation damage.

From Eqs. (7) and (8) the density of the traps can be estimated. For the FinFET devices, which have undoped films, and in the case of smaller width of the fin  $W_{fin}$ , we can approximate the depletion depth as  $W_{fin}/2$  for all the investigated temperatures. Consequently, the evolution of the Lorentzian plateau  $A_i$  versus  $\tau$  ( $A_i$  and  $\tau$  associated to the same trap) should be linear. This is verified for all observed traps; an example is showed in Fig. 7. From the slope of  $A_i$  versus  $\tau$ , the effective trap density  $N_{eff}$  of each trap can be extracted with no necessary assumption on the  $B$  coefficient and on the depletion film width. The extracted effective trap densities of each trap for two different lengths are summarized in Fig. 8. The figure clearly shows the impact of the length on the kind of traps observed in the film: in short channel, the traps may originate from process steps used for the drain and source realization

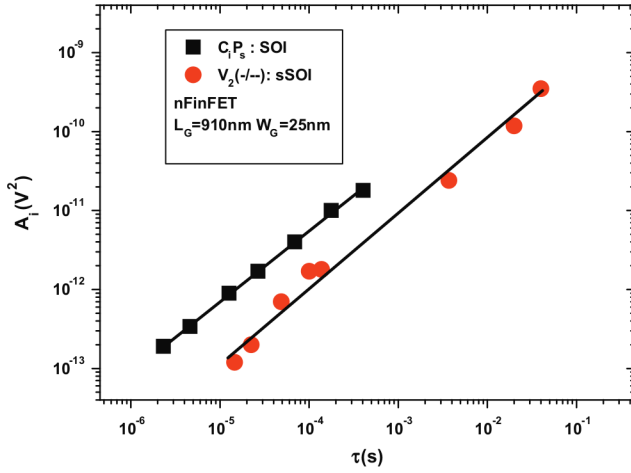


Fig. 7. Example of the evolution of the Lorentzian plateau  $A_i$  versus the time constant  $\tau$  associated to the same trap.

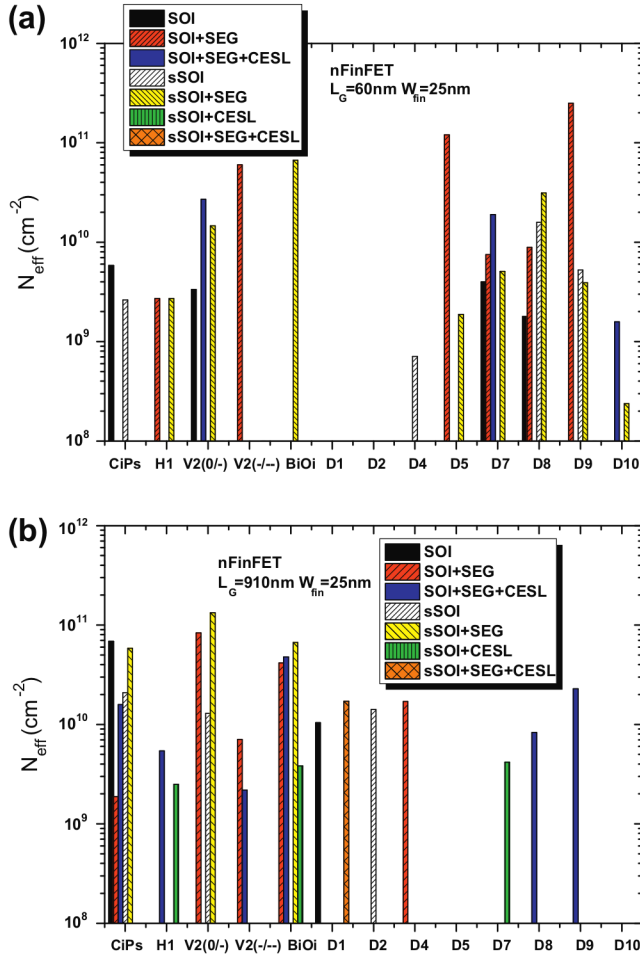


Fig. 8. Trap densities extracted from the Lorentzian plateau  $A$  for two physical gate length of 60 nm (a) and 910 nm (b).

whereas for long channel devices, the traps may be related to the process steps used for the channel optimizations.

The traps related to hydrogen may be present due to hydrogen residues after annealing. For structures which use the CESL process, the increase of the hydrogen trap density with a factor of

three compared to devices without CESL may be linked additionally to the presence of the CESL process of a  $\text{SiN}_x$  layer, containing a significant amount of hydrogen.

All the studied structures have received a Boron halo implantation (used to reduce the short channel effects). This may explain the presence of the interstitial boron–interstitial–oxygen complex ( $\text{B}_i\text{O}_i$ ) trap. The relatively higher value of the effective density of this trap can be related to the high capability of the boron diffusion.

The interstitial carbon–substitutional phosphor complex ( $\text{C}_i\text{P}_s$ ) trap is found in all structures that are processed by using a SiC liner such as in standard SOI, SOI + SEG and strained sSOI. This suggests a possible carbon contamination due to the SiC liner deposition step.

The number of observed traps is important: this may be due to the relatively low value of the pure  $1/f$  noise and the advanced technology used to process the devices. One can distinguish traps that are observed for some process condition(s), like D1 and D2 which are observed only in sSOI + SEG + CESL devices; and traps that seem to be common for all investigated technologies, like D7 and D8. This suggests that these traps may be commonly found in silicon technologies, despite that we cannot identify them yet, because of the lack of available bibliographical data. An increase with a factor of minimum two of the effective trap density of D7 and D8 can be observed for the 60 nm physical gate length between the standard SOI devices and devices that use strain or SEG. This suggests that the additional process steps used to boost the device performance (sSOI, CESL, SEG), as expected [42], leads to increase the effective trap densities in the film.

## 5. Conclusion

In this work, a systematic study of the low frequency noise versus temperature has been performed on n-channel FinFET transistors. The carrier number fluctuations dominate the  $1/f$  noise in the studied transistors for all the investigated temperatures. Low temperature operation leads to a reduction of the contribution of the access resistances and seems to increase the contribution of the carrier number correlated to mobility fluctuations to the  $1/f$  noise. The quality of the gate oxide interface was evidenced by the relatively small values of the oxide trap density deduced from  $1/f$  noise measurement.

The analysis of the temperature evolution of the Lorentzian time constants allowed to identify traps in the silicon film. For all the investigated technologies, five kinds of traps were clearly identified and almost 10 kinds of unknown traps have been frequently observed. In some cases, due to the lack of bibliographical data on strained silicon, it was not possible to identify the trap and to make a link to the related technological step. However, most likely, they can originate from the dry-etching or implantation damage. The traps density seems to be sensitive to the use of additional process steps employed to boost the device performances (sSOI, CESL, SEG).

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