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# DC and low frequency noise performances of SOI p-FinFETs at very low temperature

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## A B S T R A C T

In this paper, DC and noise measurements on strained and unstrained SOI p-FinFETs were performed at cryogenic temperatures (10 K) in order to evaluate the device performances and study the low frequency noise mechanisms. The main electrical parameters (threshold voltage, subthreshold swing, mobility, etc.) are investigated and compared to those found at 80 K and 300 K. The low frequency noise analysis clearly shows that from 300 K to 10 K, the carriers number fluctuation dominates the flicker noise in the channel in weak inversion, while the access resistances noise contribution prevails in strong inversion.  $1/f^{\gamma}$  noise has been observed with  $\gamma$  varying with the temperature, which implies a non-uniformity of the active trap density in the oxide depth. The noise of the access resistances at 300 K originates from mobility fluctuations, while at low temperature operation it seems to have a trapping–detrapping origin.

## 1. Introduction

The multiple-gate FinFET transistors on SOI substrate are considered as promising candidates for future technology nodes, due to the better control of the short channel effects by the 3D geometry, the low leakage current, and the higher mobility due to the undoped channel [1–4]. Strain engineering can further boost the device performances without adding major process complexity [5–8]. The impact of temperature on devices fabricated with an ultimate gate dielectric has to be thoroughly evaluated, in particular in order to analyze the transport properties at very low temperature.

Among all parameters that characterize these devices, the impact of the low frequency noise now plays a major role because its level increases continuously with the miniaturization. The temperature also influences the noise in the devices. It is reported that increasing temperature increases the noise in p-MOSFETs and decreases it in n-MOSFETs [9].

Several papers have been published on low frequency noise in FinFET transistors [10,11], including the impact of temperature in

the 80 K–300 K range [12–14]. The  $1/f^{\gamma}$  noise usually follows the model of McWorther for the channel with a contribution of the access resistance at high gate voltage [15].

The exponent  $\gamma$  of the  $1/f^{\gamma}$  noise spectrum is generally close to 1 (usually in the range 0.7–1.3 [16]). In some works, a temperature, a gate voltage and/or a frequency dependence of the exponent  $\gamma$  has been reported [9,16–19]. It is explained by a non uniform spatial distribution of traps in the oxide and a trap density which increases towards the interface and in this case, the  $\gamma$  parameter is lower than 1.

However, up to now, works addressing the noise in MOSFETs at temperatures lower than 10 K are rare [20] and the noise behavior in multi-gate FinFETs has never been investigated at this temperature. This paper concerns the DC and low frequency noise improvements in p-channel SOI FinFET device performance that can be realized by operating the device at very low temperature, i.e. 10 K.

## 2. Devices and experiments

The studied devices are p-channel multi-gate FinFETs (see Fig. 1). They have been processed in a 32 nm technology with standard and strained SOI substrates. The biaxial global strain (sSOI), where the stress is introduced across the whole wafer by epitaxial growth of a SiGe “buffer layer” and the uniaxial local strain, based

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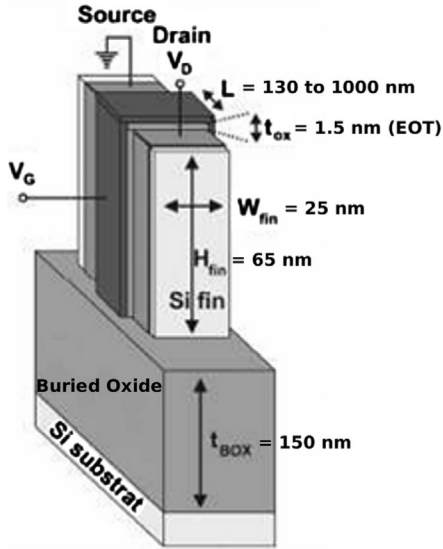


Fig. 1. Schematic SOI FinFET structure.

on the use of strain across the gate stack, referred to as Contact Etch Stop Layers (CESL) will give a stress along the channel and boost up the carrier mobility. The implementation of SiGe in the source and the drain regions, realized by Selective Epitaxial Growth (SEG), leads to a reduction of the access resistances. The gate oxide consists of a high-k dielectric (HfSiON) on top of a 1 nm interfacial SiO<sub>2</sub> resulting in an equivalent oxide thickness (EOT) of 1.5 nm. The metal gate consists of 10 nm TiN covered by 100 nm polysilicon. The devices have a fin width of 25 nm, five fins in parallel and a metallic gate lengths varying from 130 to 1000 nm.

DC and low frequency noise measurements were performed directly on wafer-level using a Lakeshore TTP4 probe at 10 K, 80 K and at room temperature. The devices were biased in the linear regime with an applied drain voltage  $|V_{DS}| = 20$  mV. Static measurements were performed using an HP4156B semiconductor parameter analyzer and the electrical parameters such as the threshold voltage  $V_{th}$ , the mobility at low field  $\mu_0$ , the access resistance  $r_{access}$  and the channel length reduction  $\Delta L$  were extracted using the Y-function [21]. At 10 K, an adapted Y-function for very low temperature was used [22–24].

The noise measurement set-up allows to bias the devices by choosing the  $V_{GS}$  and  $V_{DS}$  voltages. The drain current is then measured. It allows also to measure the total dynamic resistance between drain and source  $r_T$  and the transconductance  $g_m$  by applying a small signal at the source and gate nodes, respectively. Drain current fluctuations are amplified and the noise spectral density is calculated using a FFT spectral analyzer. Noise is reported at the input of the device by dividing by the square of the measured voltage gain between the gate and the output and this for different applied gate voltages. The tested devices are p-channel FinFETs on SOI substrate (SOI) and on sSOI substrate using SEG in the drain and source regions combined with CESL (sSOI + SEG + CESL). The low frequency noise measurements were focused for two metallic gate lengths (200 nm and 1000 nm).

### 3. Dc results and discussion

Fig. 2a and b shows respectively typical drain current  $I_D(V_{GS})$  and transconductance  $g_m(V_{GS})$  characteristics for a standard and strained p-FinFET at 10 K for various gate lengths. Fig. 3 shows an example of the drain current  $I_D(V_{GS})$  and the transconductance  $g_m(V_{GS})$  characteristics at 10 K, 80 K and 300 K for a standard and

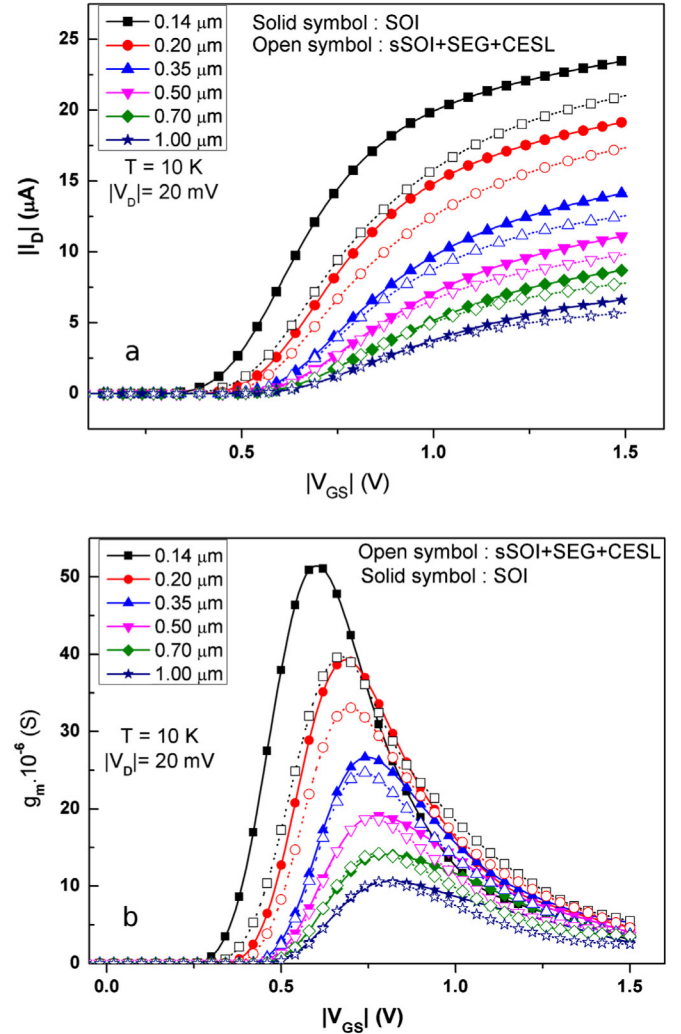


Fig. 2. Typical  $I_D(V_{GS})$  and  $g_m(V_{GS})$  characteristics for various gate lengths at 10 K.

strained p-FinFET. Although  $g_{mmax}$  the maximum of the transconductance always increases when the temperature becomes very low, the extracted mobility (see Fig. 4), which is still important at 80 K (about 150% (standard)–250% (strained) higher than at 300 K) decreases at 10 K but still has a 75% (standard)–100% (strained) increase compared to 300 K. In Fig. 4, the extracted values of the low field mobility at room temperature and 80 K are represented, while at 10 K the maximum of effective mobility are showed. The reduction of the phonon scattering may explain the increase of the mobility with the temperature decrease, while at very low temperature the degradation of the mobility could be related to surface roughness scattering [25]. At 10 K, the expected boost of the mobility for strained devices compared to standard ones is strongly reduced; this trend can be justified by a more pronounced impact of the surface roughness mechanism in strained devices at this temperature.

The subthreshold slope  $S$  is an important electrical design parameter, in particular for dynamic switching circuits. The slope could be substantially increased only by lowering the temperature operation. In Fig. 5 one see the effect of the reduction of the temperature on the subthreshold slope. At 80 K and 300 K, the values of the extracted subthreshold slope  $S$  are close to ideal values, whereas at 10 K a deviation is observed ( $S$  is higher than 8 mV/dec at 10 K for an ideal value of about 2 mV/dec). This could be related to an increase of the interface states at the band edges at low temperatures [26].

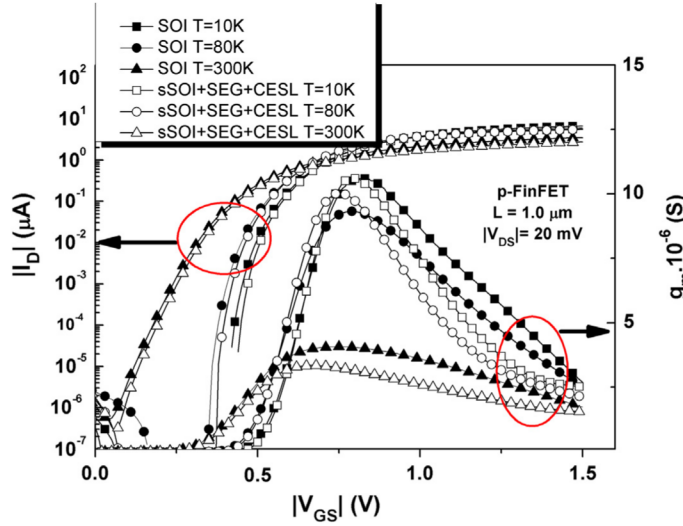


Fig. 3. Typical  $I_D(V_{GS})$  and  $g_m(V_{GS})$  characteristics for  $L = 1 \mu\text{m}$  at 10 K, 80 K and 300 K.

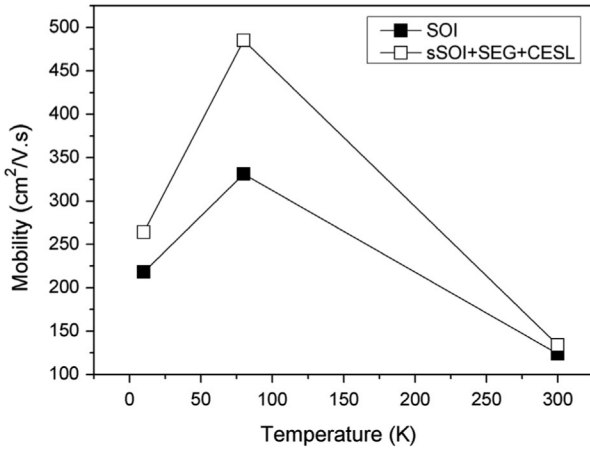


Fig. 4. The mobility versus the temperature.

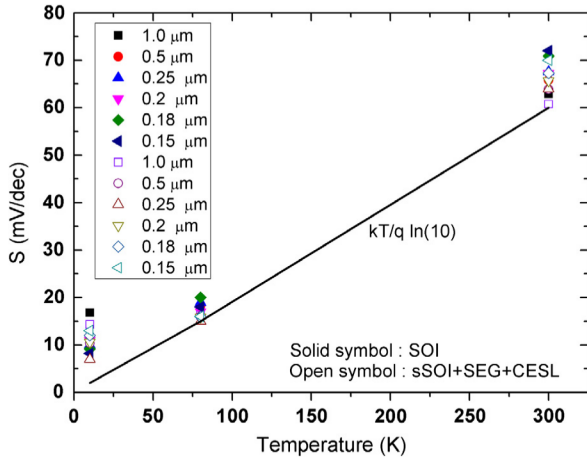


Fig. 5. Subthreshold slope  $S$  versus the temperature. The solid line indicates the ideal values.

In Fig. 6 are plotted the extracted threshold voltage for the 0.2 and 1  $\mu\text{m}$  gate lengths for unstrained and strained p-FinFETs. The solid line gives the expected trend of the threshold voltage increase with the temperature decrease (modeled with a rate of about

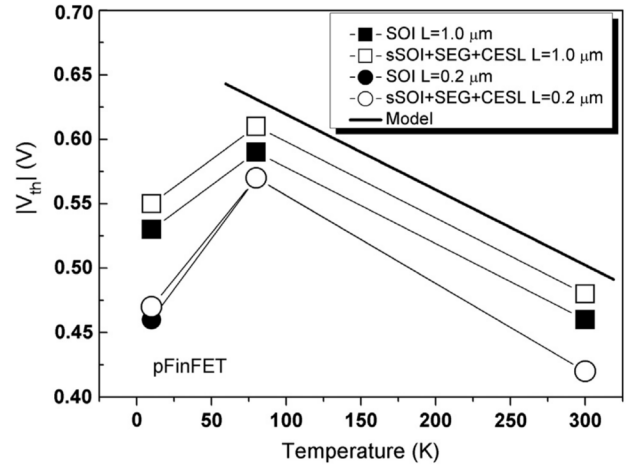


Fig. 6. Threshold voltage  $V_{th}$  versus the temperature for strained and unstrained devices for two different gate lengths (0.2 and 1  $\mu\text{m}$ ).

–0.57 mV/K [27]). Improvement of the threshold voltage is observed for all the studied devices at very low temperature operation where their values are close to the room temperature values. This behavior could be related to the temperature behavior of the Fermi level and of the surface potential at very low temperatures which are caused primarily by the temperature dependence of the intrinsic carriers concentration [28]. One can also observe that for p-FinFETs, mechanical strain slightly increases the threshold voltage for larger lengths.

#### 4. Noise model

In general, the low frequency noise is governed by the following equation which enables to model the frequency dependence of the noise spectral density at the input of a MOS transistor, taking into account three uncorrelated noise sources [29]:

$$S_{VG}(f) = B + \frac{K_f}{f^\gamma} + \sum_{i=1}^N \frac{A_i}{1 + \left(\frac{f}{f_{0i}}\right)^2} \quad (1)$$

In Eq. (1)  $B$  presents the white noise level,  $K_f/f^\gamma$  presents the flicker noise and the parameter  $K_f$  quantify the  $1/f^\gamma$  gate voltage noise spectral density level at 1 Hz. The frequency exponent may

deviate from 1 if the active trap density is not uniform in the oxide depth. The third term of the equation presents a sum of Lorentzian components, with  $A_i$  the plateau value and  $f_{oi}$  the characteristic frequency. Fig. 7 shows an example of a spectrum (normalized by the frequency) obtained at 10 K and modeled using Eq. (1). This allows to identify clearly the different noise parameters especially the Lorentzian contribution represented by bumps centered at their characteristic frequencies.

In the framework of the carrier number fluctuations, the fluctuations in the interfacial oxide charge density are equivalent to a variation in the flat-band voltage  $\delta V_{FB} = -\delta Q_{it}/(WLC_{ox})$ . A general expression of the flicker noise can be derived without any necessary assumptions about the exact mechanism behind the fluctuations in the flat-band voltage. It takes into account the supplementary mobility change due to the modulation of the scattering rate induced by the interface charge fluctuations. The impact of the access resistances  $r_{access}$  on the low frequency noise is simply obtained by adding to the channel noise the contribution of the excess noise originating from the access region [20,30,31]. So, in linear operation, the flicker noise spectral density at the input is given by:

$$\frac{K_f}{f^\gamma} = S_{V_{FB}}(1 + \alpha\mu_0 C_{ox} V_{GT})^2 + \frac{K_r}{2r_T^2} V_{GT}^2 \quad (2)$$

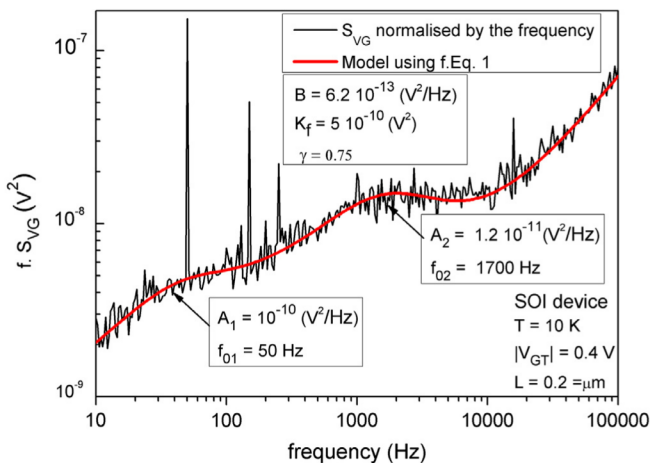
where  $\alpha$  is the Coulomb scattering coefficient,  $C_{ox}$  is the gate oxide capacitance,  $K_r$  is the access resistance noise level. Further, considering that the trapping and detrapping occurs through tunnelling processes; one can derive using the McWhorter model the expression of the noise spectral density at flatband condition  $S_{V_{FB}}$  [32]:

$$S_{V_{FB}} = \frac{q^2 k T \lambda N_{it}}{f^\gamma W L C_{ox}^2} \quad (3)$$

where  $q$  is the elementary charge,  $k$  is Boltzmann's constant,  $T$  is the absolute temperature,  $W$  and  $L$  are the effective device width and length, respectively,  $N_{it}$  is the density of traps in the gate dielectrics at the quasi-Fermi level ( $\text{cm}^{-3} \text{eV}^{-1}$ ) and  $\lambda$  is predicted by the Wentzel-Kramers-Brillouin (WKB) theory [33] as to be close to 1 Å for a Si/SiO<sub>2</sub> interface.

## 5. Noise results and discussion

Typical noise spectra measured at room temperature and at 10 K for the same applied gate voltage overdrive ( $V_{GT} = -0.5 \text{ V}$ )

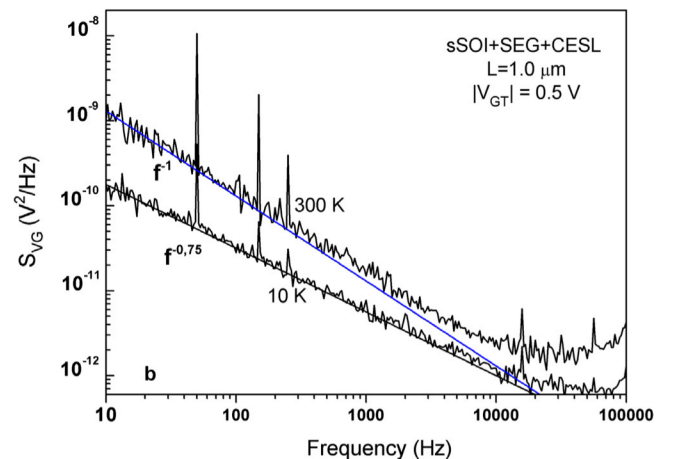
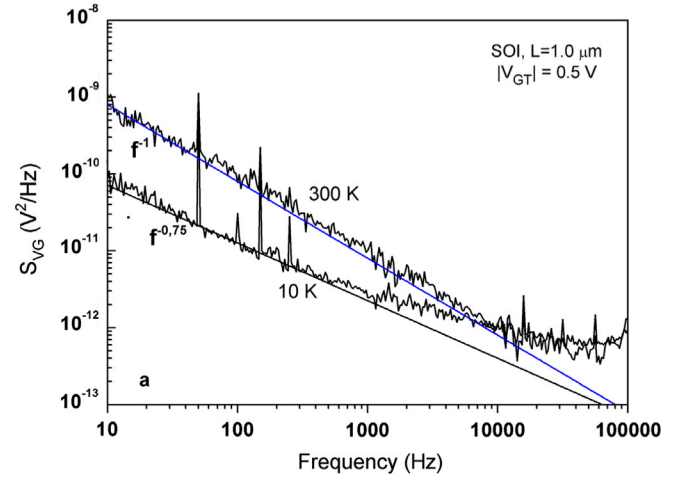


**Fig. 7.** Comparison between noise measurement and model using Eq. (1). In this figure, the  $1/f^\gamma$  contribution with  $\gamma \neq 1$ , the white noise and two Lorentzians were used to obtain the best adjustment between the model and the measurement.

are shown in Fig. 8. One can observe that the slope of the frequency dependence of the noise magnitude ( $\gamma$  in  $1/f^\gamma$ ) is lower than 1 at 10 K operation. One can also notice that  $\gamma$  is independent of strain and gate length. An example of the extracted  $K_f$  (extracted from Eq. (1)) versus  $V_{GT}$  at 300 K and 10 K is shown in Fig. 9 for a p-channel standard device. At room temperature,  $\gamma$  being equal at 1, the increase of the noise from weak to strong inversion can be modeled (using Eq. (2), the solid line in Fig. 9) by the carrier number fluctuations correlated to mobility fluctuations ( $\Delta N + \Delta \mu$ ) in the channel and in strong inversion by the parasitic access resistance ( $r_{access}$ ) noise contribution.

On the contrary at 10 K and 80 K, the noise spectra follow a  $1/f^\gamma$  dependence with the  $\gamma$  value lower than 1, whatever the applied gate voltage is. At 10 K, Fig. 9 shows that the flicker noise level is independent of the applied gate voltage overdrive in weak inversion. This suggests that the carrier number fluctuations ( $\Delta N$ ) in the channel dominates. The value of the slope of the frequency dependence of the noise magnitude ( $\gamma$  in  $1/f^\gamma$ ) lowers than 1 suggests a non-homogenous active trap distribution in the oxide, with an increase of the trap density towards the interface [16]. No contribution of the carrier number fluctuations correlated to mobility fluctuations is observed at 10 K operation. This could be correlated to the volume inversion effect around threshold, whereby the carriers populate the center of the fin body [34].

The increase of the noise in strong inversion exhibits a  $V_{GT}^2/r_T^2$  dependence (the dashed line in Fig. 9). Moreover, this behavior is



**Fig. 8.** Comparison of noise spectral density  $S_{VG}(f)$  at the device input for standard substrate (a) and strained devices (b) for the same  $V_{GT}$  voltage for two temperatures  $T = 10 \text{ K}$  and  $T = 300 \text{ K}$ .

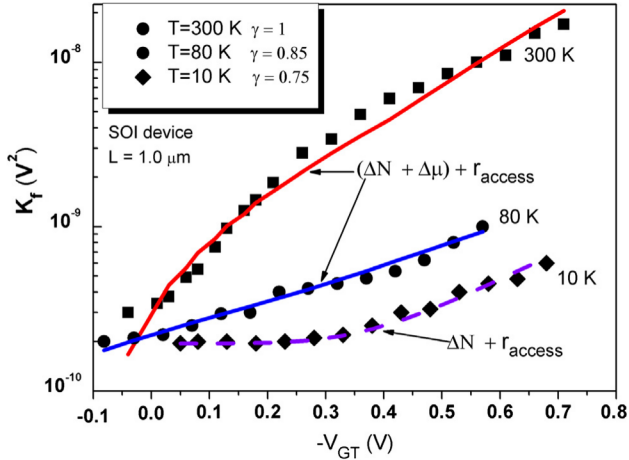


Fig. 9. The extracted  $K_f(V_{GT})$  for the standard device with length  $L = 1 \mu\text{m}$ .

observed whatever the frequency used to extract the  $K_f$  noise level (see Fig. 10). These suggest that in strong inversion the access resistance fluctuations dominate. The same behavior is observed at 80 K. This could be surprising because the access resistance fluctuations are generally supposed to be located in the deep – LDD region and the noise originates from mobility fluctuations and is usually modeled by the Hooge empirical formula [35], which gives pure  $1/f$  dependence. The  $1/f^\gamma$  dependence for the access resistances contribution suggests that the noise of the access resistance with  $\gamma \neq 1$  at 10 K may have a trapping–detrapping origin, and the noise should now be located in the region where the spacer oxide covers the main part of the LDD region.

Due to the FinFET structure itself, in particular for a large number of fins, when the distance between the fins is smaller ( $0.2 \mu\text{m}$  in our case) the region where the spacer oxide covers the LDD region is larger. For our devices, the charge sharing effect presents no significant improvement with temperature reduction. This suggests that the region controlled by the gate voltage does not significantly change with temperature. The access resistance regions are a degenerately doped region, where the scattering mechanisms also play a role. By reducing the temperature, the mobility increases due to phonon scattering reduction, while Coulomb scattering and surface roughness remain. These suggests that the access resistances noise originates from the mobility fluctuations at 300 K (with  $\gamma = 1$ ), while at low temperature operation it seems

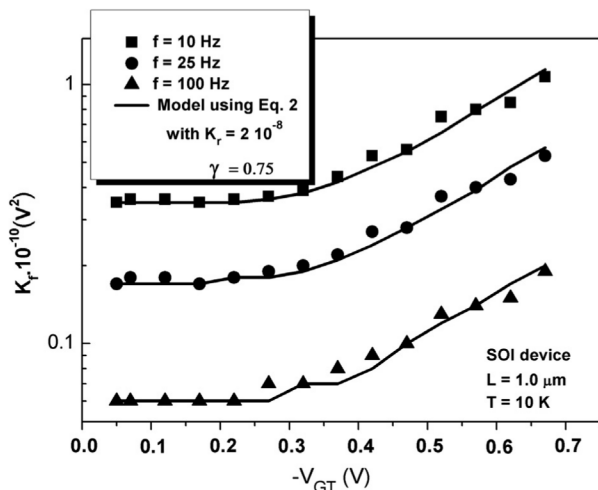


Fig. 10. The extracted  $K_f(V_{GT})$  at 10, 25 and 100 Hz, modeled by Eq. (2) with a dependence on  $1/f^\gamma$  for the access resistances contribution.

Table 1

Noise parameters  $N_{it}$ ,  $K_r$ ,  $S_{V_{FB}}$ ,  $\alpha$ ,  $\gamma$  obtained for the two lengths investigated and strained and unstrained devices.

| Tested devices    | $T$<br>(K) | $L$<br>( $\mu\text{m}$ ) | $S_{V_{FB}}$<br>$10^{-10}$<br>( $\text{V}^2/\text{Hz}$ ) | $K_r$<br>$10^{-8}$ | $\alpha$<br>$10^4$<br>( $\text{Vs}/\text{C}$ ) | $N_{it} 10^{17}$<br>( $\text{cm}^{-3} \text{eV}^{-1}$ ) | $\gamma$ |
|-------------------|------------|--------------------------|--|--------------------|--|---|----------|
| SOI               | 10         | 0.2                      | 2.95   | 0.55               |  | 57  | 0.75     |
|                   |            | 1.0                      | 1.95   | 2.0                |  | 273   | 0.75     |
|                   | 80         | 0.2                      | 5.0  | 0.9                | 0.06   | 13.6  | 0.85     |
|                   |            | 1.0                      | 2.2  | 7.5                | 0.12   | 40  | 0.85     |
|                   | 300        | 0.2                      | 9.0  | 55                 | 1.0  | 8   | 1        |
|                   |            | 1.0                      | 3.4  | 650                | 1.7  | 19  | 1        |
| sSOI + SEG + CESL | 10         | 0.2                      | 2.5  | 0.75               |  | 65  | 0.75     |
|                   |            | 1.0                      | 2.15   | 8.80               |  | 375   | 0.75     |
|                   | 80         | 0.2                      | 3.8  | 1.5                | 0.09   | 8.8   | 0.85     |
|                   |            | 1.0                      | 1.9  | 1.2                | 0.17   | 34  | 0.85     |
|                   | 300        | 0.2                      | 18.0   | 150                | 0.3  | 14  | 1        |
|                   |            | 1.0                      | 1.6  | 400                | 3.0  | 7.7   | 1        |

to have a trapping–detrapping origin (and thus leading to a  $\gamma$  parameter lower than 1).

As expected, the values of the  $K_r$  parameter (Table 1), shows a substantial reduction in the access resistance noise contribution on the total noise when the temperature decreases. For the shortest gate length and strained devices, a reduction with a factor of about 100 between 300 K and 80 K is observed, while between 80 K and 10 K the reduction is only about 2. The substantial reduction between 300 K and 80 K (observed for all devices) could be related to the phonon scattering reduction, while between 80 K and 10 K the scattering mechanisms may play an important role (Coulomb and surface roughness scattering).

Table 1 lists the main extracted noise parameters. A reduction by a factor of 1.7–3 of the  $1/f^\gamma$  noise level at 1 Hz in flatband operation at 10 K compared to room temperature for the standard device is observed. This reduction seems to be more important for smaller channel lengths and for the strained devices. On the contrary, in case of strained devices no significant variation of the noise level is observed for the larger gate length compared to standard devices.

The quality of the gate oxide interface was evidenced by the relatively small values of the oxide trap density  $N_{it}$  deduced from the  $1/f^\gamma$  noise contribution in flatband operation. Increase of the trap density can be observed at low temperature operation; this behavior being more pronounced for the higher gate length. Similar temperature variations of the  $N_{it}$  (down to 80 K) were already reported in [15] for n-channel FinFETs and can be justified by models which take into account the structure of the high- $k$  dielectric stack considering two tunneling barriers through the dielectric, corresponding to the interfacial layer and to the high- $k$  layer, respectively [36–38].

## 6. Conclusion

In this work, DC and noise measurements on SOI p-FinFETs, performed at three temperatures (10 K, 80 K and 300 K), are reported. DC performances at 10 K are good with a mobility still higher than at 300 K and threshold voltage values close to those obtained at room temperature.

The low frequency noise versus  $V_{GS}$  bias at very low temperature (10 K) has been studied on a short and long length device and compared with the observations at 80 K and 300 K. It is worth noting that for p-FinFETs, the excess noise performances are improved when the temperature decreases. The carrier number fluctuations dominate completely the  $1/f^\gamma$  noise in weak inversion and the correlated mobility fluctuations contribution decreases with

temperature reduction to finally disappear at 10 K. The  $\gamma$  parameter variation with the temperature (independent from strain and gate length) shows that the spatial distribution of traps in the oxide is not homogenous and that the active trap density increases towards the interface. The access resistance noise contribution on the total noise, which prevail in strong inversion operation, originates from mobility fluctuations at 300 K while at low temperature operation it seems to have a trapping–detrapping origin.

These first results motivate the use of the SOI p-FinFET at very low temperature applications.

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