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Low Frequency Noise Spectroscopy in Advanced nFinFETs

R. Talmat^{1,2}, H. Achour^{1,2}, B. Cretu¹, J-M. Routoure¹, A. Benfdila², R. Carin¹, N. Collaert³, A. Mercha³, E. Simoen³ and C. Claeys^{3,4}.

¹GREYC, UMR 6072 CNRS / ENSICAEN / University of Caen, 6 Bd Marechal Juin, Caen, France

²GRMNT, Mouloud Mammeri University of Tizi-Ouzou, Algeria

³Imec, Kapeldreef 75, B-3001 Leuven, Belgium

⁴E.E. Dept. KU Leuven, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium

1. Abstract

In this paper, the low frequency noise is studied from 100 K to room temperature in n-channel triple-gate FinFET transistors with 25 nm fin-width and 65 nm fin-height, a high-k dielectric, metal gate and strained and unstrained substrates. These investigations allow to identify defects in the silicon film and to make a correlation with some technological steps.

2. Introduction

The multiple-gate FinFET transistors on a Silicon-On-Insulator substrate are considered as a promising candidate for the CMOS nanometer era, due to the controlled short channel effect by the 3D geometry, the low leakage current, and the higher mobility due to the undoped channel ($10^{15}/\text{cm}^3$). Strain engineering is used to increase the mobility which is one of the enabling techniques to boost the device performance further along the ITRS roadmap [1]. In this work, low frequency noise measurements versus temperature are used as a device characterization tool in order to identify the defects present in the transistors. A powerful method for characterizing materials is provided by the Generation - Recombination (GR) noise, corresponding to a Lorentzian type of spectra and allowing for so-called noise spectroscopy when performed as a function of temperature [2,3].

3. Experimental

The n-channel transistors have been fabricated on standard and strained-SOI (sSOI) substrates. Additional splits use tensile stress induced by Contact Etch Stop Layers (CESL) across the gate stack and Selective Epitaxial Growth (SEG) for source and drain regions. The different wafers are indicated by SOI, SOI + SEG, SOI + SEG + CESL, sSOI, sSOI + SEG, sSOI + CESL, sSOI + SEG + CESL. The gate stack consists of a high-k dielectric (HfSiON) on top of a 1 nm interfacial SiO₂, resulting in an equivalent oxide thickness (EOT) of 1.5 nm. The gate metal consists of 10 nm TiN covered by 100 nm polysilicon. Further processing details can be found in [4].

The gate lengths studied were $L_G = 60$ nm and $L_G = 910$ nm with 5 fins in parallel. The

measurements were performed under linear operation at $V_{DS} = 50$ mV, the gate voltage was adjusted in order to keep the drain current constant at $I_D = 1 \mu\text{A}$ over the whole temperature range, from 100 K to room temperature. The temperature was changed by a step of 10 K.

4. Results and discussion

Figure 1 presents a frequency normalized spectrum for standard (SOI) and strained nFinFETs with different strain techniques (sSOI + SEG + CESL) for a $L_G = 60$ nm. One can notice that the studied devices have a large number of Lorentzians (GR), giving rise to bumps in the spectra when they are normalized by the frequency. This has been observed for all studied devices and for all temperatures. It has been verified that the characteristic frequency of the Lorentzians does not change with the applied gate voltage; thus, the Lorentzians originate from defects in the depletion area. For each Lorentzian, the extraction of the characteristic frequency as a function of the temperature allows to plot an Arrhenius diagram; i.e. the evolution of $\ln(\tau \cdot T^2)$ versus $1/(kT)$ where τ is given by the inverse of the characteristic frequency. The energy difference between the conduction band energy and trap energy ΔE ($\Delta E = E_c - E_T$) and the capture cross section σ_n are extracted from the slope and the y intercept of the linear fit, respectively. The physical nature of these defects can be identified by comparing the energy and capture cross section of the traps with data in the literature [5]. For each device, several defects were found. Some of them are clearly identified. Many other defects are still to be identified. However, the lack of data in the literature for these advanced materials and the fact that strain engineering may have an impact on the energy level and capture cross section, make it more challenging to identify all defects.

Figure 2 presents a typical Arrhenius diagram for a SOI nFinFET with SEG for $L_G = 910$ nm. In this example, three kinds of defects can be clearly identified: interstitial carbon-substitutional-phosphor complex (C_iP_s), interstitial boron interstitial-oxygen complex (B_iO_i) and divacancies V_2 (-/-).

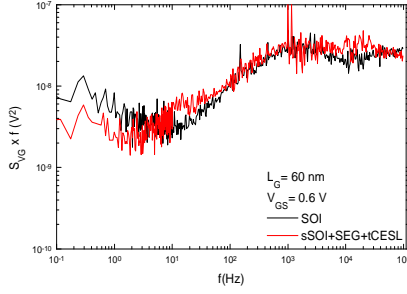


Fig.1: Frequency normalized noise for unstrained (SOI) and strained (sSOI + SEG + CESL) for nFinFETs with $L_G = 60$ nm at $V_{GS} = 0.6$ V ($V_{DS} = 50$ mV).

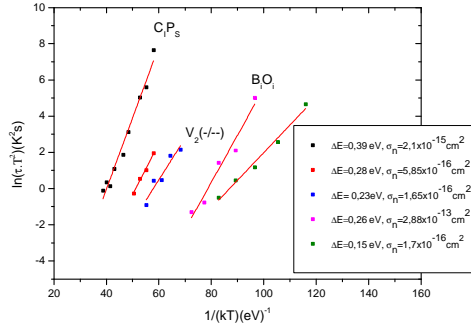


Fig.2: Arrhenius plot of a strained nFinFET (SOI + SEG) with $L_G = 910$ nm.

Table 1 shows the identified defects for all studied devices. One can notice that there are a number of defects which are frequently found in all studied devices but that not have been reported in the literature. For all the investigated technologies, 5 kinds of traps were identified: divacancies $V_2(0/-)$ and $V_2(-/-)$, traps related to hydrogen (noted H1), interstitial boron-interstitial-oxygen complex (B_1O_1) and interstitial carbon-substitutional-phosphor complex (C_1P_s). In addition to these, almost 10 kinds of unknown traps have been frequently observed. One can remark that the defect interstitial carbon-substitutional phosphor complex (C_1P_s) is found in all structures that are processed by using a SiC liner such as in standard (SOI) and strained (sSOI, SOI + SEG). This suggests a possible carbon contamination due to the SiC liner deposition step. The trap density of this defect can be evaluated; it was found that it varies from one structure to another ($5 \cdot 10^{15}$ - $3 \cdot 10^{17}/\text{cm}^3$). The number of observed traps is important: this may be due to the relatively low value of the pure $1/f$ noise and the advanced technology used to process the devices. One can also notice that some traps (D7, D8) are observed in almost all the technologies studied; this suggests that these traps may be commonly found in silicon technologies. However, they could not be identified and therefore, might be related to the strain techniques which could modify the capture cross sections and the energy levels. On the other hand, D1, D2 are only observed in sSOI+SEG+CESL. A more detailed analysis of the

process steps used in this technology could reveal the technological steps responsible for the creation of these defects.

Structure	$V_2(0/-)$	$V_2(-/-)$	H1	B_1O_1	C_1P_s	D1	D2	D4	D5	D7	D8	D9	D10
S0		X		x	X				x	x	X	x	x
S1	X	x			x			x	x		x	x	
S2	x		x	x	x			x		x	x	x	x
S3		X	x	x	x	x		x	x	x	X		
S4		x	x		x			x	X	X	X	X	x
S5		x	X	x						x	x		x
S6	x	x		x		X	X			x	x	x	x

Table 1: The identified defects for all studied devices, the gray lines indicate the structures that are processed with a SiC liner.

- D1: $\Delta E = 0.5$ eV, $\sigma_n = 1.3 \cdot 10^{15} \text{cm}^2$. $V_2(0/-)$: $\Delta E = 0.42$ eV, $\sigma_n = 10^{15} \text{cm}^2$.
D2: $\Delta E = 0.4$ eV, $\sigma_n = 9.5 \cdot 10^{17} \text{cm}^2$. $V_2(-/-)$:
 $\Delta E = 0.23$ eV, $\sigma_n = 10^{15} \cdot 10^{16} \text{cm}^2$.
D4: $\Delta E = 0.29$ eV, $\sigma_n = 2 \cdot 10^{17} \text{cm}^2$.
D5: $\Delta E = 0.29$ eV, $\sigma_n = 1.8 \cdot 10^{19} \text{cm}^2$.
D7: $\Delta E = 0.23$ eV, $\sigma_n = 1.8 \cdot 10^{17} \text{cm}^2$.
D8: $\Delta E = 0.19$ eV, $\sigma_n = 7.9 \cdot 10^{18} \text{cm}^2$.
D9: $\Delta E = 0.15$ eV, $\sigma_n = 2.1 \cdot 10^{18} \text{cm}^2$.
D10: $\Delta E = 0.2$ eV, $\sigma_n = 1.8 \cdot 10^{15} \text{cm}^2$.
S0: SOI; S1: SOI + SEG, S2: SOI + SEG + CESL, S3: sSOI,
S4: sSOI + SEG, S5: sSOI + CESL S6: sSOI + SEG + CESL.
X: found for both studied gate lengths;
x: found for one gate length only.

5. Conclusions

In this work, a systematic study of the low frequency noise versus temperature has been performed on nFinFETs transistors. The analysis of the temperature evolution of the Lorentzians time constant allowed to identify the defects in the silicon film. For all the investigated technologies, 5 kinds of traps were clearly identified and almost 10 kinds of unknown traps have been frequently observed. In some cases, due to the lack of bibliographic data on strained silicon, it was not possible to identify the defect and to make a link to the related technological step. However, most likely, they can originate from the dry-etching or implantation damage. Finally, a carbon contamination probably due to the use of a SiC liner was revealed.

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