Assessment of temperature dependence of the low frequency noise in unstrained and strained FinF

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Assessment of temperature dependence of the low frequency noise in unstrained and strained FinFETs

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***Abstract*— This paper aims at the studying the low frequency noise from 100 K up to room temperature in n- and p-channel triple-gate FinFET transistors with 25 nm fin-width, 65 nm fin-height, a high-k dielectric / metal gate stack, strained and unstrained substrates. These investigations allow evaluating the quality of the gate oxide interface, to identify defects in the silicon film and to make a correlation between the observed defects and some technological steps.**

Keyword: FinFET, SOI, strain, low-frequency noise, Lorentzian, temperature

I. INTRODUCTION

Multiple-gate FinFET transistors on a Silicon-On-Insulator substrate are considered as a promising candidate for the future technology nodes, due to the better control of the short channel effects by the 3D geometry, the low leakage current and the higher mobility due to the undoped channel. Strain engineering can further boost the device performance [1].

In this work, low frequency noise measurements versus temperature are used as a device characterization tool in order to evaluate the quality of the gate oxide interface and to identify the defects in the depletion zone of the transistors. One of the methods used for material characterization is provided by the study of the Generation - Recombination (GR) noise, corresponding to a Lorentzian type of spectra and allowing to do the so-called noise spectroscopy when performed as a function of temperature [2,3].

II. EXPERIMENTAL

The n- and p-channel transistors have been fabricated on standard (and strained) SOI (and sSOI) substrates. Additional splits use tensile stress induced by Contact Etch Stop Layers (CESL) across the gate stack and Selective Epitaxial Growth (SEG) for source and drain regions. The different wafers are indicated by SOI, SOI + SEG, SOI + SEG + CESL, sSOI, sSOI + SEG, sSOI + CESL, sSOI + SEG + CESL. The gate oxide consists of a high-k dielectric (HfSiON) on top of a 1 nm interfacial SiO_2, resulting in an equivalent oxide thickness (EOT) of 1.5 nm. The metal gate consists of 10 nm TiN covered by 100 nm polysilicon. The physical gate lengths studied were L_G = 60 nm and L_G = 910 nm and devices with a fin-width of 25 nm and 5 fins in parallel were analyzed. Further processing details can be found in [4].

The low-frequency noise measurements were performed directly on wafer-level using a "Lakeshore TTP4" prober from 100 K up to room temperature. The devices were biased in the linear regime with an applied drain voltage $|V_{DS}| = 50$ mV. The measurement set-up allows to measure the total dynamic resistance between drain and source r_T. The noise measurements were performed as a function of the gate voltage and at fixed drain current (the gate voltage was adjusted in order to keep the drain current constant at I_D = 1 µA) over the whole temperature range using a step of 10 K.

III. RESULTS AND DISCUSSION

In general, the typical noise spectral density can contain a combination of three noise sources: white noise, flicker noise $\left(K_f / f^{\gamma}\right)$ and Lorentzian noise. Assuming $\gamma = 1$, the following equation enables to model the frequency dependence of the noise spectral density at the input:

$$S_{V_G}(f) = B + \frac{K_f}{f} + \sum_{i=0}^{N} \frac{A_i}{1 + \left(\frac{f}{f_{oi}}\right)^2} \qquad (1)$$

where B presents the white noise level, K_f / f presents the flicker noise when $\gamma = 1$, and the third term of the equation presents a sum of Lorentzian components, with A_i the plateau value and f_{oi} the characteristic frequency of the Lorentzian noise components. As shown in Figure 1, the noise spectra in the studied devices contain a combination of these three noise sources and can be perfectly modeled by the model of equation (1). The extracted K_f level is found to be independent of the applied gate voltage overdrive $V_{GT} = V_{GS} - V_{th}$ in intermediate inversion for n- and p-channel devices for all investigated temperatures. An example for a p-channel FinFET is illustrated in Figure 2. This suggests that carrier number fluctuations due to carrier trapping in the oxide layer dominate the 1/f noise in intermediate inversion. The increase

of the noise in strong inversion may be related to the parasitic access resistance of the devices. According to this hypothesis, a model based on the McWhorter theory and access resistance contribution is described by the equation (2):

$$S_{VG} = \left(\frac{r_T - r_{acces}}{r_T} \right)^2 \cdot \frac{q^2 \cdot k \cdot T \cdot N_t}{C_{ox}^2 \cdot W \cdot L \cdot \alpha_t \cdot f} + \frac{r_{access}^2}{2 \cdot r_T^2} \cdot \frac{K_r}{f} \cdot V_{GT}^2 \quad (2)$$

Where k is the Boltzmann constant, C_{ox} is the oxide capacitance, N_t is the density of the traps which effectively contribute to McWhorter trapping at temperature T, α_t is the tunneling parameter, q is the electron charge and r_{access} is the total access resistance extracted by DC measurements. One can note that equation (2) can perfectly model the K_f evolution versus the gate bias as shown in figure 2.

The trap density N_t can be extracted from the 1/f noise contribution in flatband operation. For n-channel FinFET, we obtain values between $2 \cdot 10^{17}$ - $2 \cdot 10^{18}$ $eV^{-1}cm^{-3}$ and for p-channel values between $2 \cdot 10^{17}$ - $5 \cdot 10^{17}$ $eV^{-1}cm^{-3}$. These values are lower than those found in FinFETs with a HfO_2 gate oxide [5,6]. The relatively small values of the oxide trap density are a good indication of the quality of the HfSiON. One can note that the nitridation of the hafnium oxide prevents the penetration of dopants in the oxide. This has been proven in previous observations in planar transistors [7].

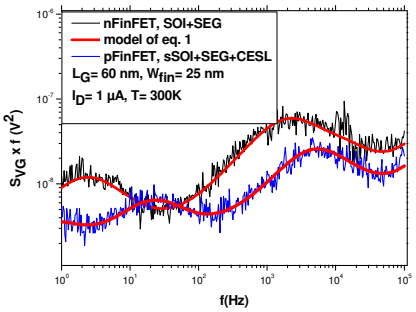

Figure 1. Example of typical low-frequency noise spectra normalized by the frequency in n- and p-channel devices at 300K.

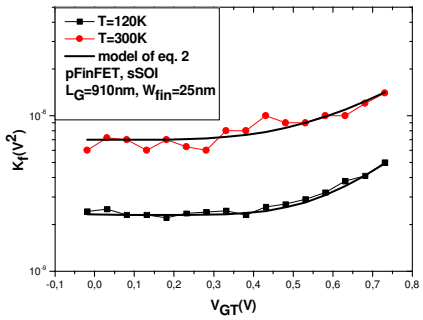

Figure 2. Frequency normalized input-referred noise spectral density K_f at different temperatures.

Figure 3 and 4 illustrate examples of the frequency normalized noise spectral density versus temperature behavior for a p and n-channel device. Generally, the Lorentzians component of the noise spectra can originate from traps (at the interface or in the depletion zone) and in small areas from random telegraphic signals (RTS). If the characteristic frequency of the Lorentzians does not change with the applied gate voltage, the Lorentzians originate from defects in the depletion region. An example is given in Figure 5, where the characteristic Lorentzian frequency versus the applied gate voltage is plotted in weak inversion for an n-channel device. In strong inversion, one may observe Lorentzians for which the characteristic frequency depends on the applied gate voltage and sometimes for small area devices even RTS is observed.

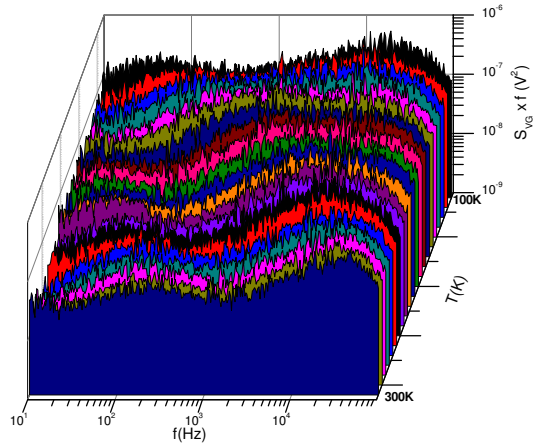

Figure 3. Frequency normalized noise spectral density versus temperature for a p-channel sSOI+CESL FinFET with L_G=60 nm.

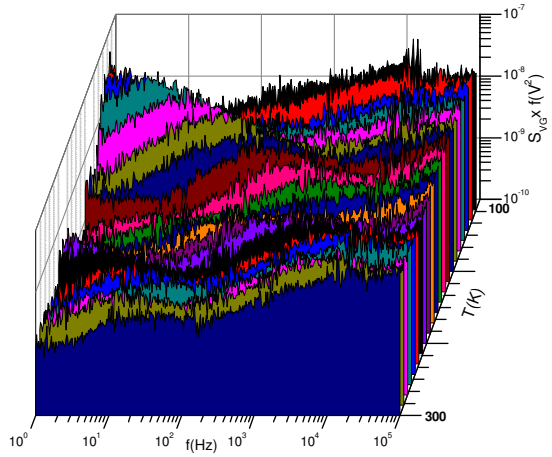

Figure 4. Frequency normalized noise spectral density versus temperature for a n-channel sSOI+SEG FinFET with L_G=60 nm.

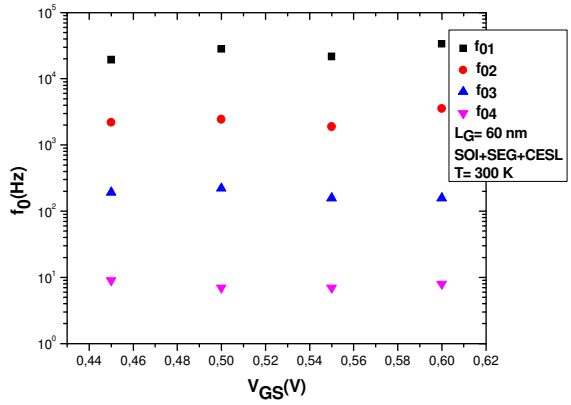

Figure 5. Example of the evolution of the Lorentzian characteristic frequency versus the applied gate voltage in weak inversion for a n-channel SOI+SEG+CESL FinFET.

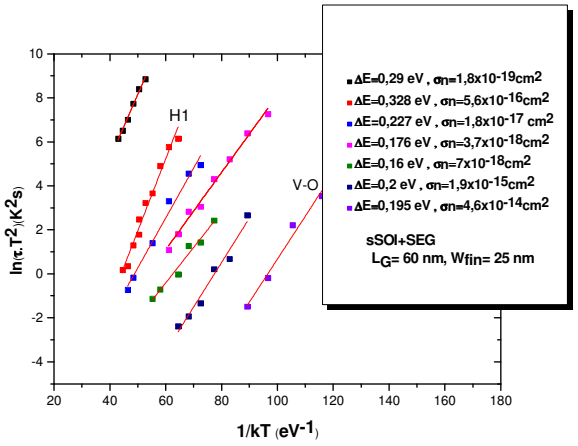

Figure 6. Arrhenius plot for a n-channel sSOI + SEG FinFET with L_G = 60 nm.

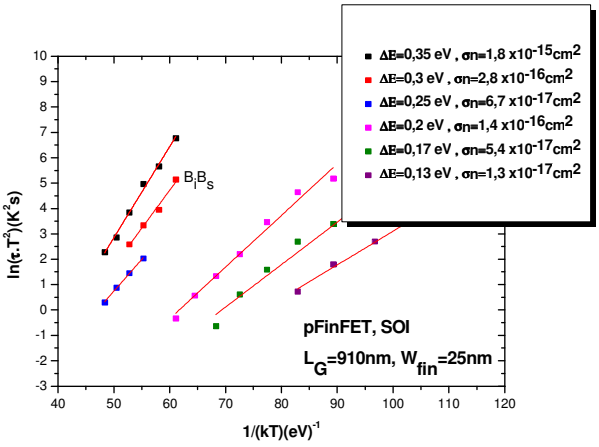

Figure 7. Arrhenius plot for a p-channel SOI FinFET with L_G = 910 nm.

For each Lorentzian originating from defects in the depletion area, the extraction of the characteristic frequency as a function of the temperature allows to plot an Arrhenius diagram; i.e. the evolution of $\ln(\tau \cdot T^2)$ versus 1/(kT) where τ is given by the inverse of the characteristic frequency multiplied by 2π. Using the model of [2], summarized in equation (3), the energy difference between the appropriate band energy and the trap energy (i.e. $\Delta E = E_C - E_T$ or $\Delta E = E_T - E_V$) and the capture cross section σ_n (nMOS) or σ_p (pMOS) are extracted from the slope and the y-intercept of the linear fit, respectively.

$$\begin{aligned} &if\ E_T - E_i > 0,\ \ln(\tau T^2) = \frac{E_C - E_T}{kT} + \ln\left(\frac{h^3}{4k^2\sigma_n\sqrt{6\pi^3 M_c m_e^{*1/2} m_h^{*3/2}}}\right) \\ &if\ E_T - E_i < 0,\ \ln(\tau T^2) = \frac{E_T - E_V}{kT} + \ln\left(\frac{h^3}{4k^2\sigma_p\sqrt{6\pi^3 M_c m_e^{*3/2} m_h^{*1/2}}}\right) \end{aligned} \quad (3)$$

Where h is the Planck constant, k is the Boltzmann constant $m_e^{*1/2}$, $m_h^{*3/2}$ are the effective mass of electrons and holes respectively and M_c is the number of conduction band energy minima. The physical nature of these defects can be identified by comparing the energy and capture cross section of the traps with data in the literature [8]. Figure 6 and 7 present typical Arrhenius diagram for n- and p-channel FinFETs. In these examples, 2 kinds of defects can be clearly identified for the n-channel sSOI + SEG device and only 1 defect in the case of the p-channel SOI device.

For all the investigated n-channel technologies, 5 kinds of traps were identified: divacancies $V_2(0/-)$ and $V_2(-/--)$, traps related to hydrogen (noted H1), interstitial boron-interstitial-oxygen complex (B_iO_i) and interstitial carbon-substitutional-phosphor complex (C_iP_s). In addition to these, almost 10 kinds of unknown traps have been frequently observed.

For all the investigated p-channel technologies, 6 kinds of traps were identified: interstitial carbon – interstitial oxygen complex C_iO_i (+/0), interstitial carbon C_i (+/0), interstitial carbon - substitutional phosphor complex C_iP_s (0/+), interstitial carbon-substitutional carbon complex C_iC_s (+/0), interstitial boron - substitutional carbon complex (B_iC_s), interstitial boron - substitutional boron complex (B_iB_s). In addition to these, almost 5 kinds of unknown traps have been frequently observed.

Tables I and II summarize the identified defects for all studied devices. One can notice that there are a number of defects which are frequently found in all studied devices but which are not reported in the literature. Most likely, they originate from the dry-etching or implantation damage. One can remark that the defect interstitial carbon -substitutional phosphor complex (C_iP_s) is found in all structures that are processed by using a SiC liner such as in standard (SOI) and strained (sSOI, SOI + SEG). This suggests a possible carbon contamination due to the SiC liner deposition step. However, all devices seem to suffer from the carbon and boron diffusion. Hydrogen may come from the CESL processing (a SiN_x layer containing a significant amount of hydrogen).

n –channel Structures	V_2 (0/-)	V_2 (-/--)	H1	B_iO_i	C_iP_s (0/-)	D1	D2	D4	D5	D7	D8	D9	D10
S0		x X		X	x X				x	x	x X	x	x
S1	x X	X			X			X	x		x	x	
S2	X		X	X	X			X		X	x	x	X
S3		x X	X	X	x	X		x	X	X	x X		
S4		X	x		X			X	x X	x X	x X	x X	x
S5		x	x X	X						X	x		
S6	x	x		x		x X	x X		x	X	x	x	X

TABLE I. THE IDENTIFIED DEFECTS FOR N-CHANNEL DEVICES, THE GRAY LINES INDICATE THE STRUCTURES THAT ARE PROCESSED WITH A SIC LINER.

p –channel Structures	C_iO_i (+/0)	C_i (+/0)	C_iP_s (0/+)	C_iC_s (+/0)	B_iC_s	B_iB_s	D11	D12	D13	D14	D15
S0						X		X			X
S1	x	x	x	x		X		x	X		x
S4			x	x X			x X	X		x	x
S5			x X	x				X		x	X
S6	X	X		x X	x	x	x		X		X

TABLE II. THE IDENTIFIED DEFECTS FOR P-CHANNEL DEVICES, THE GRAY LINES INDICATE THE STRUCTURES THAT ARE PROCESSED WITH A SIC LINER.

n-channel:
D1: ΔE=0.5eV, σ_n=1.3x10^{-15}cm^2.
D2: ΔE=0.4eV, σ_n=9.5x10^{-17}cm^2.
D4: ΔE=0.29eV, σ_n=2x10^{-17}cm^2.
D5: ΔE=0. 29eV, σ_n=1.8x10^{-19}cm^2.
D7: ΔE=0. 23eV, σ_n=1.8x10^{-17}cm^2.
D8: ΔE=0.19eV, σ_n=7.9x10^{-18}cm^2.
D9: ΔE=0. 15eV, σ_n=2.1x10^{-18}cm^2.
D10: ΔE=0.2eV, σ_n=1.8x10^{-15}cm^2.

p-channel:

D11: ΔE=0.1eV, σ_p=10^{-19}-10^{-20} cm^2
D12: ΔE=0.13eV, σ_p=10^{-19}-10^{-20}cm^2
D13: ΔE=0.44eV, σ_p=10^{-15}-10^{-16}cm^2
D14: ΔE=0.55eV, σ_p =10^{-14}cm^2
D15: ΔE=0.16eV, σ_p =10^{-19}-10^{-20}cm^2

***V_2(0/-):** ΔE=0.42 eV, σ_n=10^{-15}cm^2.*
***V_2(-/--):** ΔE=0.23 eV, σ_n=10^{-15}-10^{-16}cm^2.*
***B_iO_i:** ΔE=0.26 eV, σ_n=10^{-13}-10^{-14}cm^2.*
***H1**: ΔE=0. 32 eV, σ_n=10^{-15}cm^2.*
***C_iP_s**(0/-): ΔE=0. 38 eV, σ_n≈10^{-15}cm^2.*

***C_iO_i** (+/0) : ΔE=0.35 eV, σ_p =10^{-16}cm^2*
***C_i** (+/0) : ΔE=0.27 eV, σ_p =10^{-17}cm^2*
***C_iP_s** (0/+) : ΔE=0.48 eV, σ_p≈10^{-15}cm^2*
***C_iC_s** (+/0) : ΔE=0.09 eV, σ_p ≈10^{-18}cm^2*
***B_iC_s** : ΔE=0.29eV σ_p =8x10^{-17}cm^2*
***B_iB_s** : ΔE=0.30 eV σ_p ≈10^{-16}cm^2*

S0: SOI; S1: SOI + SEG, S2: SOI + SEG + CESL, S3: sSOI, S4: sSOI + SEG, S5: sSOI + CESL S6: sSOI + SEG + CESL.
x: found in L_G = 60 nm; X: found in L_G = 910 nm.

The number of observed traps is important: this may be due to the relatively low value of the pure 1/f noise and the advanced technology used to process the devices. One can distinguish traps that are observed punctually, like D1 and D2 which are observed only in n-channel sSOI + SEG + CESL devices; and traps that seem to be common for all investigated technologies, like D7, D8 for n-channel devices and like D12, D15 in p-channel technologies. This suggests that these traps may be commonly found in silicon technologies, despite that we cannot identify them yet, because of the lack of bibliographical data.

IV. CONCLUSION

In this work, a systematic study of the low frequency noise versus temperature has been performed on n- and p-channel FinFET transistors. The carrier number fluctuations dominate the 1/f noise in the studied n and p-channel transistors for all the investigated temperatures. The noise contribution of the access resistances on the 1/f noise is reduced at lower temperature operation. The quality of the gate oxide interface was evidenced by the relatively small values of the oxide trap density. The analysis of the temperature evolution of the Lorentzian time constants allowed to identify the defects in the silicon film. For all the investigated technologies, 5 kinds of traps were clearly identified in n-channel devices and 6 kinds of traps in the p-channel devices. Almost 15 kinds of unknown traps have been frequently observed. In some cases, due to the lack of bibliographical data on strained silicon, it was not possible to identify the defect and to make a link to the related technological step. However, most likely, they can originate from the dry-etching or implantation damage.

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