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# Low-Frequency Noise Behavior in P-channel SOI FinFETs Processed With Different Strain Techniques

W. Guo, R. Talmat, B. Cretu, J-M. Routoure, R. Carin,  
A. Mercha<sup>a</sup>, E. Simoen<sup>a</sup> and C. Claeys<sup>a, b</sup>

*GREYC, UMR 6072 CNRS / ENSICAEN / University of Caen, 6 Bd Marechal Juin, Caen, France*

*<sup>a</sup>IMEC, Kapeldreef 75, B-3001 Leuven, Belgium,*

*<sup>b</sup>E.E. Dept. KU Leuven, B-30001 Leuven, Belgium*

**Abstract.** The aim of this paper is to investigate the low-frequency noise behavior in p-channel SOI FinFETs processed with different strain techniques. An unusual noise behavior was observed for all devices studied. This unusual noise was investigated for different applied gate voltages and different channel lengths at room temperature. The carrier number fluctuations explain the flicker noise for all devices. The different strain techniques employed have no significant impact in the noise level.

**Keywords:** FinFET, SOI Substrate, Strain techniques, Low-frequency noise

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## INTRODUCTION

The main advantages of multi-gate FinFET (MuGFET) devices include the improvement of the short channel effects, the leakage currents, the threshold voltage dopant fluctuations, and eventual higher mobility due to the undoped channels [1-4].

The transistor performances depend on the semiconductor-dielectric interface quality. The low-frequency noise analysis is one of the tools used to analyze the quality of the gate oxide. For a better understanding of the device physics a study of the low-frequency noise is required.

In this work, the low-frequency noise performance of p-channel tri-gate FinFETs is investigated. We have first evidenced an unusual noise behavior for all the tested devices. The impact of the channel length on the unusual noise behavior is analyzed at room temperature. This unusual behavior was already observed in [5] for n-channel FinFETs only in devices processed with selective epitaxial growth. Finally, we have shown that the different strain techniques used to enhance the performances of MOS devices have no significant impact on the noise level.

## EXPERIMENTAL

The available devices are p-channel FinFETs, with gate mask length  $L_{\text{Fin}}$  varying from  $0.15\mu\text{m}$  up to  $1\mu\text{m}$ , mask width  $W_{\text{Fin}}$  from  $0.15\mu\text{m}$  to  $3\mu\text{m}$ , fixed fin height  $H_{\text{Fin}} = 65\text{nm}$ , and having five fins in parallel. The high-k gate stack consists of TiN/TaN/HfO<sub>2</sub>/SiO<sub>2</sub>, with a measured equivalent oxide thickness (EOT) of 1.9 nm. The device fabrication details can be found in [6].

The standard FinFETs on an SOI substrate were used as a reference (noted SOI). Other analyzed structures are: FinFETs using selective epitaxial growth (SEG) in order to reduce the access resistance by increasing the height of the source and drain regions (noted SOI+SEG), as well as FinFETs using SEG combined with a CESL (contact etch stop layer) strain technique (noted SOI+SEG+CESL).

Low-frequency noise measurements were performed directly on wafer using a 2 inch "Lakeshore TTP4" prober. The devices were biased in the linear regime with an applied drain voltage  $V_D = -20\text{ mV}$ . The experimental set-up sweeps a range from 0.1 Hz to 100 kHz.

## RESULTS AND DISCUSSION

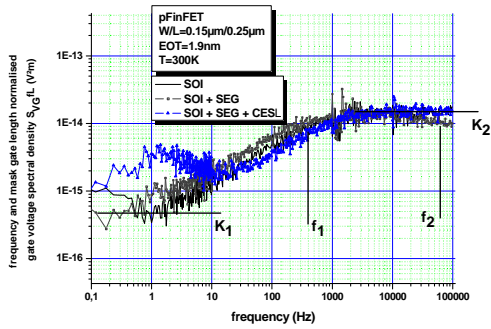
An unusual noise behavior was already highlighted for the n-channel FinFETs [5] and an empirical model was proposed (equation 1) assuming two 1/f noise levels: the one with the higher level shows an unusual frequency dependence at the two corner frequencies  $f_1$  and  $f_2$ , and it is noted by "K<sub>2</sub> 1/f noise"; the one with the lowest level is noted "K<sub>1</sub> 1/f noise":

$$S_{v_g} = \text{white noise} + \frac{K_1}{f} + \frac{K_2}{f} \frac{1}{1 + \frac{f_1}{f}} \frac{1}{1 + \frac{f}{f_2}} \quad (\text{equation 1})$$

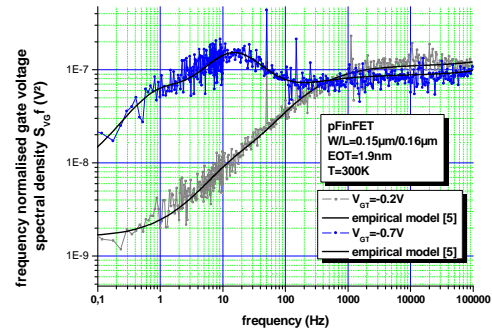
In [5] it was also demonstrated that the K<sub>2</sub> 1/f noise component could be attributed to the carrier number fluctuations in the channel. Moreover, it was clearly pointed out that in the case of the n-channel FinFETs, the unusual noise behavior is observed only for the SEG devices.

Examples of the frequency normalized gate voltage spectral density in p-channel FinFETs are showed in Figure 1 for  $L_{\text{mask}} = 0.25\mu\text{m}$  for all tested structures. Contrary to n-channel FinFET, the unusual noise behavior can be observed for all the analyzed structures. Additional Lorentzian noise components can be observed, but will be discussed further. From Figure 1, it is clear that the different strain techniques employed have no significant impact on the noise level.

Good agreement between the measured noise spectra and the empirical model proposed in [5] has been verified for all channel gate lengths for all structures studied. Figure 2 illustrates this agreement for the case of a reference device with  $L_{\text{mask}} = 0.16\mu\text{m}$ , with different applied gate biases. We can notice that the unusual noise can be clearly observed only in the weak inversion regime. In strong inversion operation, additional noise components can "hide" the K<sub>1</sub> 1/f noise component, as shown in the Figure 2.



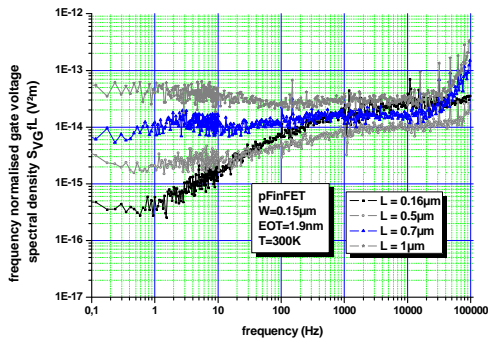
**FIGURE 1.** Frequency normalized gate voltage spectral density for  $L_{\text{mask}} = 0.25\mu\text{m}$



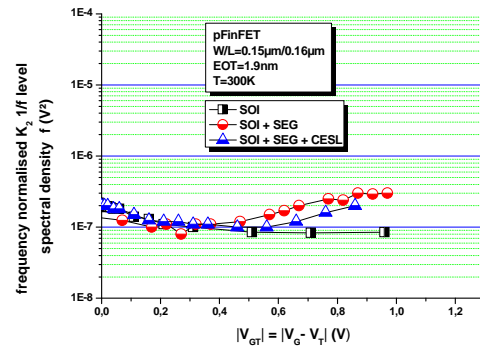
**FIGURE 2.** Frequency normalized gate voltage spectral density for  $L_{\text{mask}} = 0.16\mu\text{m}$ , for different applied gate biases

A study of the low-frequency noise was performed for different channel lengths at fixed drain current (i.e.  $I_D = 3\mu\text{A}$ ). In Figure 3 the gate voltage spectral density normalized by frequency and the mask gate length for the reference device is shown. We can notice that at the same drain current conditions (i.e.  $I_D = 3\mu\text{A}$ ), the unusual noise can be observed only for gate mask lengths smaller than  $0.7\mu\text{m}$ . This result could suggest a possible access resistance contribution on the low noise spectra.

Figure 4 shows the variation of the frequency normalized  $K_2$   $1/f$  level noise spectral density (@  $V_D = -20\text{mV}$ ) versus the absolute value of the applied gate voltage. We consider the hypothesis that the  $K_2$   $1/f$  noise component could be attributed to the carrier fluctuations in the channel (i.e. as in [5]). One can notice that there is no significant difference in the noise magnitude in the weak inversion for all the FinFET structures investigated. These results show that the different strain techniques employed do not affect the noise level.



**FIGURE 3.** The gate voltage spectral density normalized by frequency and the mask gate length for the reference FinFET structures at  $I_D = 3\mu\text{A}$



**FIGURE 4.** The variation of the frequency normalized  $K_2$   $1/f$  level noise spectral density versus the applied gate voltage

It can also be observed that in weak inversion the gate voltage spectral density related to the  $K_2$   $1/f$  level is quasi-independent on the applied gate voltage. This suggests that the carrier number fluctuations due to hole trapping in the oxide

dominate for all devices in weak inversion. This result may be striking since the  $1/f$  noise in pMOS transistors can usually be explained using the Hooge model. Therefore, the carrier number fluctuations model can be used to explain the origin of the noise and extract an average value of the oxide trap density  $N_{it}$  ( $\text{eV}^{-1}\text{cm}^{-3}$ ) [7]. Using the effective gate length and width, this oxide trap density was found to be about  $4 \cdot 10^{18} \text{eV}^{-1}\text{cm}^{-3}$  for all tested devices.

## CONCLUSION

An unusual noise behavior is observed for the all p-channel FinFET structures tested in the present. This striking noise behavior clearly appears only in weak and weak to strong inversion transition. In the same  $I_D$  biases, it was observed for gate mask lengths smaller than  $0.7\mu\text{m}$ . These results imply a possible contribution of the access resistances on the low-frequency noise spectra. The empirical model proposed in [5] can perfectly model the unusual noise behavior. We have found that the carrier number fluctuations dominated the flicker noise for all studied FinFET structures. Further investigations are still necessary in order to validate the origin of the two  $1/f$  noise sources.

## ACKNOWLEDGMENTS

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