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# A 39.7 dBm and 18.5% PAE compact X to Ku band GaN Travelling Wave Amplifier

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Abstract—This article presents an 8GHz to 18GHz Travelling Wave Amplifier (TWA) averaging 39.7dBm of output power and 18.5% Power Added Efficiency (PAE). At 11 GHz, the TWA reaches a peak output power 40.4dBm and a peak PAE of 22%. The proposed architecture consists in the combination of two TWAs in parallel to increase output power. An innovative low loss compact power combiner is proposed to reduce the overall die size and keep high PAE. The amplifier presented here has the advantage to be very compact compared to similar MMICs High Power Amplifiers (HPA). An innovative design methodology based on a strong correlation between the amplifier and the combiner design is introduced.

Keywords—MMIC; GaN; TWA; Power combining;

#### I. INTRODUCTION

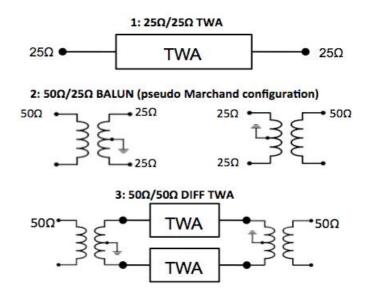
GaN MMICs are of great interest due to their wideband and high power abilities. Moreover, high efficiencies components can be realized with GaN technologies. Higher efficiency makes thermal management easier to deal with because less power is dissipated through heat. Then MMICs can be put closer to each other, which is an important step towards higher integration, and thus size reduction of systems. Moreover, thanks to their physical properties, GaN devices are very reliable in harsh conditions. For example, a GaN MMIC can handle a very high input power before destruction because of the high breakdown voltages of transistors (close to 100V).

Power Amplifier is the key component of any transmitting chain. In fact, frequency range of operation, output power and efficiencies of the complete chain mainly depend on the power amplifier performances. Frequency bands of interest for these applications are C to Ku bands. Designing an efficient HPA over such a wide frequency band is quite a challenge mainly because of impedances management. Indeed, the optimal impedances have important variations with frequency. Moreover, to achieve the powers levels required there is a need to combine multiple power cells. A first approach for doing so is through current combining; power cells are combined together through a network made of metal lines, stubs and parallel capacitors. Interesting results can be achieved in terms of output power and PAE such as in [1] and [2]. However this approach has the disadvantage to occupy an important die size and to present an important ripple when targeting large bandwidths.

Another approach is the Travelling Wave Amplifier (TWA) principle; its inventors detail the theory in [3]. It consists into coupling two lines with active devices. With proper design, this architecture can achieve very important bandwidth with a low ripple such as in [4]. The TWA architecture has been chosen for the circuit presented in this article. Two TWAs are combined in parallel with an innovative combiner to increase output power while keeping the die size as small as possible.

In section II, an innovative design methodology for both TWA and power combiner design is presented. Section III focuses on the design and the optimization of a single TWA and section IV depicts the differential TWA with power combiners and splitters.

Fig. 1. TWA design methodology steps



#### II. INNOVATIVE DESIGN METHODOLOGY

In this section, an innovative design methodology for a differential TWA is introduced.

The methodology is applied here to TWAs design but could work with any amplifier. The objective is to end up with a single-to-single  $50\Omega$  system. However, to increase output power, a solution is to parallelize two unit amplifiers, this introduces the power combination issue. A good candidate to perform the power combination is a balanced to unbalanced transformer (balun). This methodology is based on two assumptions; one is that both input and output optimal impedances for any HPA are typically much lower than  $50\Omega$  and the second one is that a balun can achieve a wider frequency range with low losses if its transformation ratio is equal to 1.

Fig. 1 illustrates the 3 steps design methodology. The first thing is to design and optimize a standalone  $25\Omega/25\Omega$  HPA or TWA in this case. Performances of this amplifier should be better than those of a conventional  $50\Omega/50\Omega$  amplifier because the optimal impedances are closer to  $25\Omega$  than  $50\Omega$  so less losses are expected in the matching network.

Then, the goal of step 2 is to design a power combiner performing the  $50\Omega$  single to  $50\Omega$  differential conversion. So the transformation ratio is equal to one, which helps achieving the largest bandwidth possible. A  $50\Omega$  differential output actually means two  $25\Omega$  outputs in opposition of phase. This is performed both for the input splitter and the output combiner.

Finally, step 3 consists in combining two identical TWAs developed in step 1 through the splitter and the combiner developed in step 2. The two TWAs are then working out of phase and see from both their input and output an impedance of  $25\Omega$ , impedance that they have been designed to work with, so performances should be maximal.

Simulations have been performed with the UMS GH25 process, a European GaN integrated process offering  $0.25\mu m$ gate length HEMTs that can be biased with a DC drain current around 100mA/mm under 25V. The process includes resistor, capacitors, inductors, microstrip-lines and via-holes through substrate.

In section III the design of the single  $25\Omega/25\Omega$  TWA is going to be detailed while section IV focuses on the design of power combiners/splitters and the assembly of the two TWAs in parallel.

#### III. SINGLE TWA DESIGN

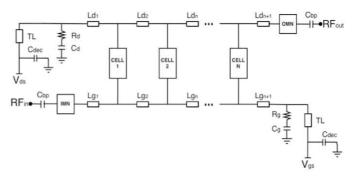
In this section, the design and the optimization of a single  $25\Omega/25\Omega$  are depicted. Optimization is made in terms of output power and efficiency rather than in small signal gain and flatness.

#### A. Architecture and parameters optimization

In a conventional TWA (or uniform TWA), all cells are the same, all input transmission lines in between cells  $(L_{g1}..L_{gn})$  have same width and length, same thing applies for output lines  $(L_{d1}..L_{dn})$  and both input and output lines should be terminated by a resistor with a value of  $25\Omega$  in our case (would be  $50\Omega$  for a conventional TWA). If these conditions are met then the amplifier is optimized in terms of small-signal gain and gain flatness as in [5]. However, as described in [6] when trying to optimize the TWA in terms of output power and PAE, non-uniform topologies should be concerned. This approach consists in increasing transistor sizes in cells close to the output

and changing size of transmission lines in order for each cell to see its optimal impedance in terms of output power and PAE.

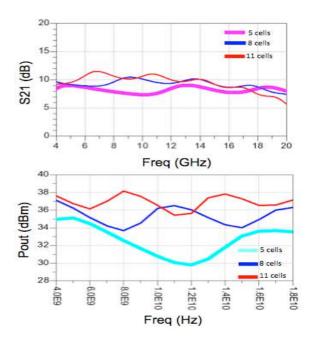
Fig. 2. Single TWA architecture



The architecture of choice for the single TWA is presented in Fig. 2. The active cells (1 to n) are common source HEMTs with a RC network located on the gate of each device to prevent low frequencies oscillations. IMN and OMN blocks are matching networks for both the input and the input to present impedances as close as possible to  $25\Omega$  all over the frequency range; practically they are just open stubs.  $R_{\rm g}$  is the input resistor described earlier and  $R_{\rm d}$  should be the output one. However, with the objective to get a maximal output power, it was chosen to remove  $R_{\rm d}$  in order to transmit as much power as possible to the load and not dissipate it into a resistor. This would introduce a small-signal gain ripple but that is the cost to pay towards high output power and thus high PAE.

Next, it matters to determine the optimal number of cells to match both bandwidth and output power specifications. More cells would increase gain and output power at the cost of bandwidth and vice versa.

Fig. 3. Number of cells effect on gain (top) and output power (bottom)

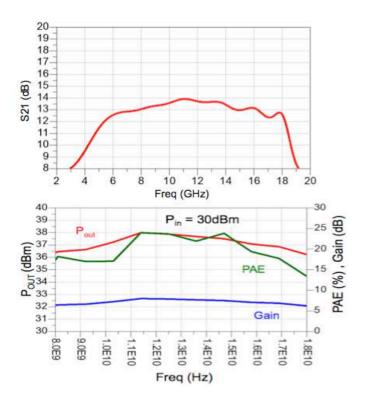


Linear simulations have been performed to determine the optimal numbers of cells versus bandwidth and non-linear ones to optimize output power; results for both are plotted in Fig. 3. 5 cells structure clearly allows achieving a large bandwidth (up to 20GHz) but the output power is in average all over the band 3dBm lower than architecture with 11 cells. Even though 11cells structure introduce a strong gain-cut off after 17GHz, it is still delivering high output power up to 18GHz. This is explained by the fact that optimal impedances differ quite a lot from small to large signal behavior so this frequency cut-off shifting is noticed in every MMIC HPAs and not just for TWAs.

#### B. Simulation results

Based on previous considerations and optimizations the architecture chosen is the non-uniform 11 cells TWA. Cells 1 to 9 have are  $4*75\mu m$  HEMTs (with R=700 $\Omega$  and C=0.72pF for the stabilization network) and cells 10 and 11 are  $4*100\mu m$  devices (R=200 $\Omega$  and C=0.93pF).  $R_g$  is equal to  $30\Omega$  and  $R_d$  has been removed,  $C_g$  is equal to 5pF and does not contribute to matching but prevents DC to be shorted to the ground. Each cell is biased with a DC drain current of 120mA/mm under a drain voltage of 20V.

Fig. 4. Small signal (top) and non linear (bottom) simulation results



Small signal gain is plotted in Fig. 4; from 8GHz to 18GHz it averages a value of 13.2dB and reaches 13.9dB at 11GHz. S<sub>11</sub> remains under -5.2dB and S<sub>22</sub> under 9.5dB all over the frequency range. Large signal simulation results are plotted in Fig. 4 too for an input power of 30dBm. In average the output power and the PAE are respectively equal to 37.3dBm and 18.8% with maximal values of 38dBm and 24% respectively at 11GHz and 14.8GHz.

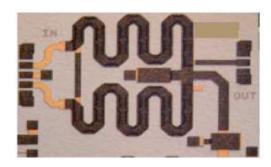
#### IV. DIFFERENTIAL TWA

To increase output power from the single TWA, two of them are going to combined in parallel to double output power. Firstly, implementation of power splitters and couplers are detailed and then simulations results for the overall TWA are presented.

#### A. Power combiner design

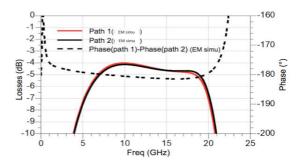
As explained in Section II, a balun topology has been picked to implement the power combiner and the power splitter. This topology has the advantages of having low losses over a wide frequency range. Moreover, this structure can be very compact when implemented as a stacked balun instead of planar balun. It means having the windings on top of each other instead of side by side, electromagnetic coupling is then vertical instead of planar. Two layers are required to implement such a balun (one for each winding), however MMICs classical back ends just have one. On a previous work, we proposed an innovative solution to implement a stacked balun with the helps of air bridges. Details on the design and measurements results can be found in [7]. Based on the same topology a new balun has been designed to match frequency range. A photography of a realized stacked balun is presented in Fig. 5.

Fig. 5. Photography of a realized stacked balun



The same balun can be used in the input and the output because in both case a  $50\Omega$  to a differential  $50\Omega$  conversion is required. The balun is fully EM simulated (with Agilent Momentum software) for better accuracy, results are plotted in Fig. 6. From 8 to 18GHz, insertion loss average 1.4dB with an amplitude imbalance of 0.15dB, minimal insertion loss of 1dB is achieved at 10GHz. Phase imbalance goes from 0.1° to 1.2° all over the band and the size of this balun is only 0.61mm².

Fig. 6. Standalone balun simulation

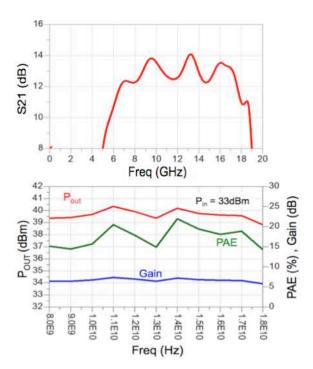


This balun is very good candidate to act as a power combiner/splitter due to its very small size and its low loss wideband behavior.

#### B. Differential TWA

the building blocks (single TWA, power combiner/splitter) now designed optimized, and implementation of the full amplifier can be done. As shown in Fig. 1, it consists in parallelizing two single TWAs through baluns to end up with a compact single  $50\Omega$  to single  $50\Omega$  ultra wideband and high power amplifier. EM simulations of combiners and all transmission lines have been performed for better accuracy.

Fig. 7. Small signal (top) and non linear (bottom) simulation results



Simulation results are plotted in Fig. 7. For both small signal and large signal behavior. Small signal gain is over 12.2 dB from 8GHz to 18GHz and reaches a peak value of 14.1dB at 13GHz. Gain ripple is close to 2dB, as explained before circuit has been optimized in terms of power and not gain flatness. For an input power of 33dBm, the output power averages 39.7dBm all over the band and reaches a maximum of 40.4dBm at 11GHz. The PAE is 18.5% in average and reaches a peak value of 22%. In Table. I, performances of the developed amplifier are compared to the state of art.

#### CONCLUSION

Through an innovative design methodology, a compact wideband TWA was developed. It delivers an average of 39.7dBm from 8 to 18GHz with an efficiency of 18.5% making it a very suitable candidate to be implemented in an high power wideband transmitter. This circuit has not been realized yet, but layout estimations allow us to claim that the overall HPA could fit inside 15mm<sup>2</sup>.

TABLE I. GAN TWA STATE OF ART

Ref	Technology	Frequency (GHz)	Pout (dBm)	PAE (%)	Size (mm²)
This work	GaN 0.25μm	8-18	39.7	18.5	15
[4]	GaN 0.2μm	2-20	42	26	38
[8]	GaN 0.25μm	2-20	40	28	NA
[9]	Gan 0.25µm	1.5-17	39	20	15.3

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