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A 2.4GHz to 6GHz Active Balun in GaN Technology

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Abstract— This article presents a S-C band active balun in a GaN integrated technology. Based on a differential pair this circuit realizes the single to differential conversion. Moreover this circuit can be used as preamplifier to drive a power stage. It delivers more than 25dBm in each differential path in the [2,4GHz-6GHz] band with a maximum of 29dBm at 3.8GHz. The chip has been realized in the UMS GH25 process, a GaN HEMT technology with a 0.25μm gate length.

I. INTRODUCTION

One of the main advantages of GaN based integrated technologies is the ability to deliver a high output power over a wide frequency range. Various applications can take advantage of this property such as electronic warfare communications and radar systems. For example we can mention radar in S, C, X and Ku bands for military applications or meteorological radars in C-band and base stations for cellular phones too. To increase even more the delivered power from the emitter side, a solution is to parallelize unit power cells in the power amplifier [1]. In this article, a differential structure allowing combining two elementary power cells is presented. This approach implies the single to differential conversion problem. To ensure this conversion, a balun is used most of the time. Classical baluns are realized with two passive inductors either stacked or interleaved. Such elements have important losses, especially when they are designed to work over a wide frequency range. The proposed solution in this article is to realize an active balun based on a differential pair. This structure has the advantage to deliver gain instead of losses thanks to the transistors used in the differential pair. Moreover such a circuit can perform at the same time the single to differential conversion and act as driver amplifier too. This results in a very interesting decrease in terms of die area because instead of having a passive balun and a differential amplifier, there is only the active balun left.

An important amount of differentials pairs used to realize the differential to single conversion could be found in the literature such as [2]. On the contrary, very few circuits realizing the single to differential conversion thanks to a differential pair are reported. A demonstration of such a circuit is made in a CMOS technology [3] and another one [4] with a

MMIC. Both these work achieve good performances in terms of gain and phase mismatch but none of them propose a solution delivering high output power as it is done in this work.

This circuit has been implemented in the GH25 integrated GaN process from UMS foundry. This technology is still under development and has not been qualified for public release yet. Power devices are normally on HEMT transistors with a minimal gate length of 0.25μm. This technology is dedicated for power applications up to 20GHz.

In section 2, the topology used will be presented and discussed. Section 3.A will focus on small-signal simulation results while in section 3.B non-linear simulation results will be discussed.

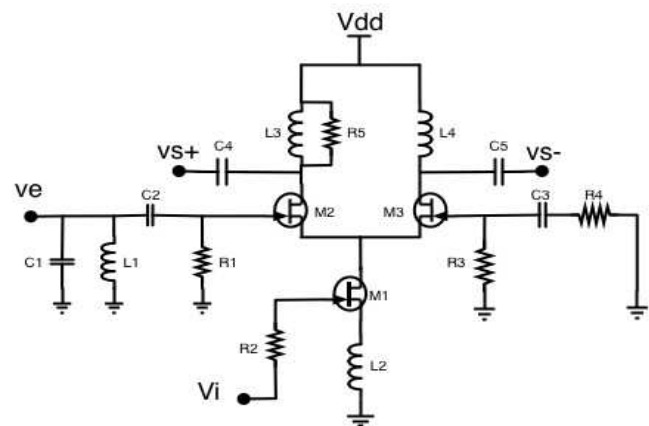


Figure 1. Active balun schematic.

II. ACTIVE BALUN ARCHITECTURE

To perform the single to differential conversion with gain instead of losses, a differential pair in referenced mode will be used. Indeed one input will receive the RF signal and the second input will be grounded from the RF point of view, both sides will have the same DC bias point. Outputs will be in

opposition of phase and thus generate the differential signal. The circuit topology is presented in Fig. 1.

By inputting the signal to on only one input, dissymmetry in terms of both gain and phases will appear in the outputs. The conception challenge is thus to decrease them as much as possible with compensation techniques.

The circuit is based on transistors $M2$ and $M3$, which form the differential pair core. These transistors are HEMT GaN with a size of $8 \times 125 \mu\text{m}$ each, they are biased with a DC current of 145 mA each. $M1$ is a device of $8 \times 150 \mu\text{m}$ which biases the differential pair. The wideband input matching network is formed by the parallel elements $C1$ and $L1$ and by the serial capacitor $C2$ that acts as bypass capacitor too. Inductors $L3$ and $L4$ are chock inductors for each differential output but although contribute to the output matching networks. In the same way, capacitors $C4$ and $C5$ are used both for output matching and for bypass purpose.

V_e is the single input on the gate of $M2$, while V_{s+} and V_{s-} are the two differential outputs respectively taken on $M2$ and $M3$ drains. As mentioned earlier, the fact to input the signal on one side of the differential pair only is going to generate dissymmetries in terms of gain and phase in between the two outputs. To compensate these dissymmetries resistors $R4$ and $R5$ are introduced respectively in series on $M3$ gate and in parallel with choke inductor $L3$. These resistors aim at modifying the quality factor of $C3$ and $L3$, in order to decrease dissymmetries in between the outputs.

As far as biasing is concerned, an effort was made to decrease the numbers of different voltage values. The fact that GaN HEMT transistors require negative V_{gs} values to function properly must be taken into consideration. V_i is the voltage applied to $M1$ gate; it controls the DC current level. V_i is chosen to bias $M2$ and $M3$ at the desired current value (145mA for each transistor) and to be able to impose a null voltage to $M2$ and $M3$ gates, that is to say to ground them from a DC point of view. A value of -1.8V for V_i allows to achieve these requirements, it leads in a static drain voltage of 2.7V for the transistor $M1$. This means that both sources of $M2$ and $M3$ have their DC voltage set to this same value of 2.7V . Then when we connect $M2$ and $M3$ gates to the ground, it results in a V_{gs} DC voltage of -2.7V for both $M2$ and $M3$. Setting V_{DD} to 25V , currents I_{ds2} and I_{ds3} are equal and are set with the help of the single voltage reference V_i . The value of 145mA for I_{ds2} and I_{ds3} was determined to be the best compromise between gain and power delivered to the output.

III. SIMULATION RESULTS

Both linear and non-linear simulations are performed to optimize this circuit performances' both as driver amplifier and as a balun. For the amplifier side, input and output matchings' alongside power delivered have to be plotted, while for the balun gain imbalance and phase difference between the outputs are two highly important criteria.

Linear and non-linear simulation results are presented in two different parts in this section.

A. Linear Simulations

S-parameters simulation is performed with the ADS software from Agilent to ensure proper input and output matching along with linear stability. The convention that S_{11} correspond to the input V_e and that S_{22} and S_{33} respectively correspond to the outputs V_{s+} and V_{s-} is taken in the following. S_{11} remains under -10dB in the $[2.5\text{GHz} - 6\text{GHz}]$ band (Fig. 2). This demonstrates that matching network formed by $C1$, $L1$ and $C2$ has wideband capabilities. In the output side, a difference between S_{22} and S_{33} is observed. Even if both curves have the same shape, S_{22} remains at a much lower value than S_{33} for every frequency over 3GHz .

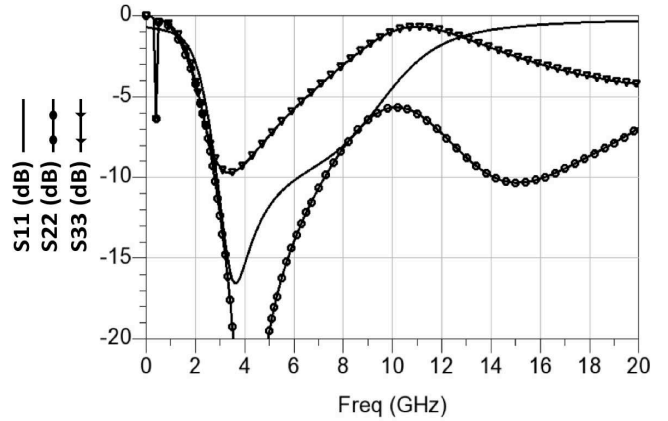


Figure 2. Input matching (S_{11}) and output matchings (S_{22} , S_{33}).

This difference can be explained by the fact that an effort has been made to equalize the two outputs in terms of power behavior more than in terms of linear mode of operation. In other words, the matching performed is a power matching and not one to the conjugate as it is normally done to improve small signal gain.

Fig. 3 is a plot of the phase difference between the outputs V_{s+} and V_{s-} . In the frequency band of interest, the phase difference goes from 189° at 2.5GHz to 175° at 6GHz . This leads to a maximal error of 5.5% compared to 180° .

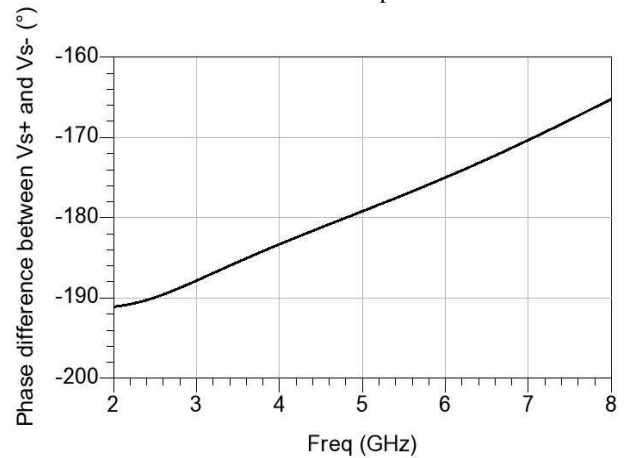


Figure 3. Phase difference between the differential outputs V_{s+} and V_{s-} .

B. Non-Linear Simulations

To evaluate power performances and non-linear behavior, harmonic balance simulations are performed. Both wideband and high power aspects have to be considered here. That is why, firstly a frequency sweep with a fixed input power level has to be performed and then a power sweep at a fixed frequency in the middle of the frequency band is simulated.

Fig. 4 represents the output power delivered to each of the differential output for frequencies from 2GHz to 8GHz with an input power level constant at 20dBm. In the [2.4GHz-6GHz] frequency band, each output delivers more than 25dBm with a peak of 27.4dBm@3.8GHz. The power imbalance in between the two outputs varies from 0dB to 0.4dB in the [2.4GHz-6GHz] frequency band.

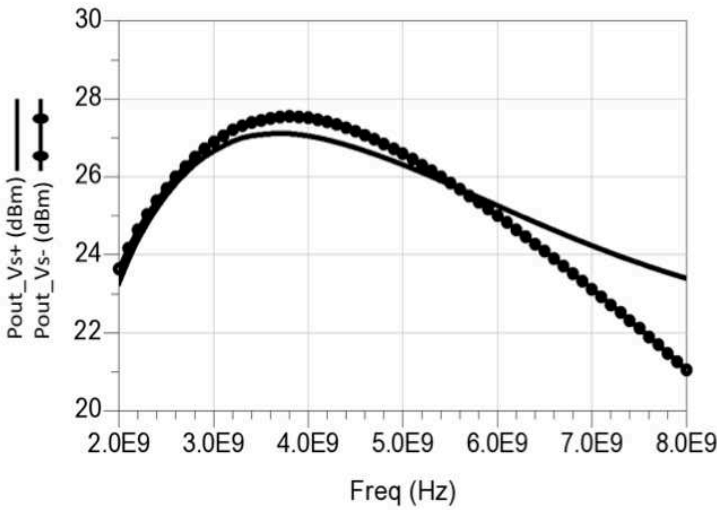


Figure 4. Output power in each output for $P_{in} = 20\text{dBm}$.

Both output voltage waveforms are plotted in Fig. 5, two periods are represented, which gives access to both amplitude and phase information. First thing to notice is that differential outputs are out of phase. To be accurate the maximal time difference experienced between when one output reaches its maximal value and the other one is minimal value is of 3.2ps. Considering the fact that a frequency of 3.8GHz corresponds to a period of 263ps, this time difference represents a phase mismatch of 4.4° , a value in agreement with the results obtained with linear simulations in section 3.A. In terms of amplitude, one output has an excursion of 15V when the second one reaches 16.1V. This corresponds to 6.8% of relative error in between the outputs.

Fig. 6 is a power sweep performed at 3.8GHz, a frequency where best performances are achieved. Both outputs (V_{s+} and V_{s-}) are represented versus input power. An output power of respectively 29.1dBm and 29.6dBm for both outputs is observed for an input of 25dBm, this results in a differential output power (sum of the output power delivered to each path) of 32.4dBm and thus in a differential gain of 7.4dB. These values confirm the great interest of this circuit topology that realizes the single to differential conversion and has power gain at the same time making it a very reliable to act as a driver amplifier for a differential power stage.

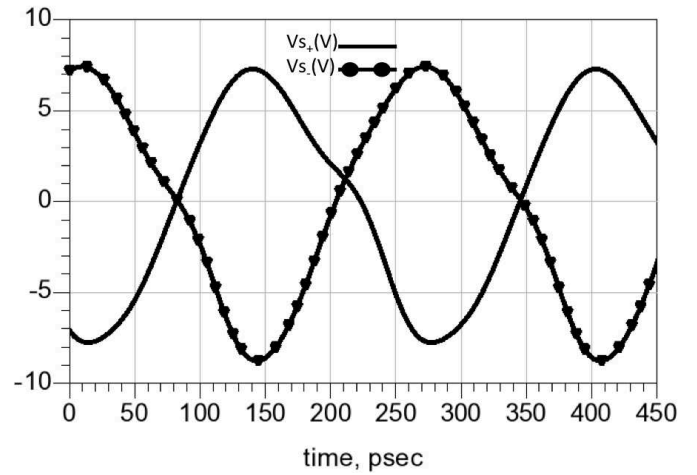


Figure 5. Outputs voltage waveforms @3.8GHz.

Taking a look at mismatch between the two power paths in Fig. 6, a very good correlation is obtained for an input power between 18dBm and 25dBm with a power imbalance lower than 0.2dB. From 0dBm to 17dBm of input power, an almost constant imbalance of 0.9dB is observed while power paths diverge for an input power of 25dBm. Due to the strong changes in the transistor behavior, which goes from linear to highly non-linear through the power sweep, the compensation technique presented earlier has been designed to be the most efficient for an input power around 20dBm, which is proven by values enounced earlier.

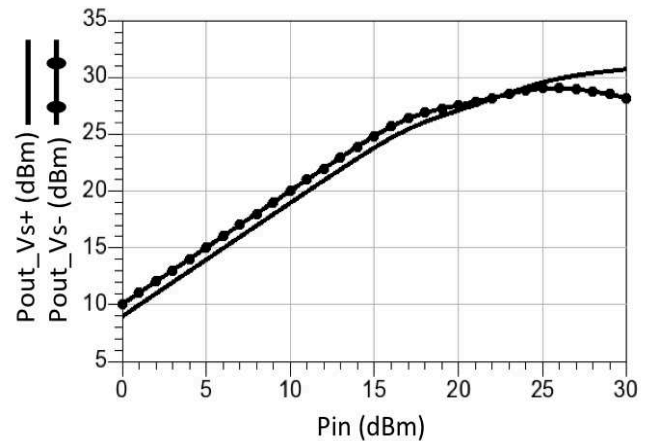


Figure 6. Output power vs P_{in} @3.8GHz

The power added efficiency as it usually defined does not correspond very well to the differential structure proposed here. Then it is decided to introduce the differential power added efficiency (DPAE) defined, by (1). P_{out_Vsp} and P_{out_Vsm} correspond to the power delivered by each output expressed in watt while P_{in} and P_{dc} correspond respectively to the input power and to DC power both expressed in watt too. According to this formula (1), the DPAE is expressed in percentage. In this circuit for an input power of 20 dBm the DPAE averages 10.8% in the [2.4GHz-6GHz] frequency band. The maximal efficiency is reached at 3.8GHz with a value of 13.8%. The lack of differential driver amplifiers in a GaN integrated process published make it is hard to give a numbered comparison with the state of the art.

$$DPAE = \frac{100 * (P_{out_vsp} + P_{out_vsm}) - P_{in}}{P_{dc}} \quad (1)$$

IV. CONCLUSION

This study has proven the feasibility of an active balun in a GaN integrated technology. Simulation results show that gain and phase imbalances have been well compensated in the frequency band of interest from 2.4GHz to 6GHz. Moreover, non-linear simulations show that the maximal output power reaches 27.4dBm@3.8GHz and remains over 25dBm overall the frequency band considered for an input power of 20dBm. By increasing the input power to 25dBm, both outputs deliver more than 29dBm@3.8GHz with an associated gain of 4.3dB. Power level values are given for each of the differential output, which means that the total output power delivered is 3dB higher than these values. This active balun can then be used as a driver amplifier for a differential power stage. The combination of both the balun and driver function results in a drastic reduction of the die area compared to a classical approach consisting in passive balun followed by a preamplifier, this circuit occupies an area of only 3.5mm². This circuit can be used in many applications whenever high power levels are at stake such as radars for military applications in S to C bands or communicating systems based on multipurpose antennas.

This circuit has been implemented in the GH25 process from UMS foundry. The version presented here has the only

difference to have its outputs matched to 50 Ohms while the one sent into foundry actually acts as a driver amplifier so was match directly to the power stage it drives.

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