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Direct writing of graphene patterns on insulating substrates under ambient conditions

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To unleash the full potential of graphene in electronics and optoelectronics, high-quality graphene patterns on insulating substrates are required. However, existing methods generally follow a “synthesis + patterning” strategy, which are time consuming and costly for fabricating high-quality graphene patterns on desired substrates. We developed a nanofabrication process to deposit high-quality graphene patterns directly on insulating substrates via a solid-phase laser direct writing (LDW) process. Open-air and room-temperature fabrication of graphene patterns on insulating substrates has been achieved via a femtosecond LDW process without graphene transfer and patterning. Various graphene patterns, including texts, spirals, line arrays, and integrated circuit patterns, with a feature line width of 800 nm and a low sheet resistance of 205 ohm/sq, were fabricated. The LDW method provides a facile and cost-effective way to fabricate complex and high-quality graphene patterns directly on target substrates, which opens a door for fabricating various advanced functional devices.

Graphene, a single-atom layer of graphite, has drawn tremendous attention from both the academic and industrial communities, starting soon after its discovery, due to its unique and outstanding electrical^{1–3}, mechanical⁴, thermal⁵, and optical properties^{6,7}. Due to its high electrical conductivity and wide-range optical transparency, graphene has been envisioned as one of the most promising candidates for future flexible, transparent electronics and optoelectronics⁸, including touch screen displays⁹, solar cells^{10,11}, sensors^{12–15}, and transparent electrodes^{16–19}.

The nanofabrication of high-quality graphene patterns on desired substrates remains one of the key challenges for future graphene applications and has recently become a focused research area. Up to now, the fabrication of graphene patterns has been achieved through various methods following a “synthesis + patterning” strategy²⁰. For example, graphene is synthesized by chemical vapor deposition (CVD) on Cu or Ni foils and then transferred to an insulating substrate followed by a patterning (e.g. plasma etching) process with a shadow mask^{21,22}. Although high-quality graphene patterns can be reliably fabricated using the “synthesis + patterning” approaches, a typical fabrication process generally requires multiple steps which are time consuming and lack economic viability. Therefore, there is a strong demand for cost-effective nanofabrication of graphene patterns with low energy consumption and a short fabrication time.

The laser direct writing (LDW) technique has been proposed and appears to be one of the promising approaches²³. Compared with the conventional “synthesis + patterning” approaches, the LDW approach provides high flexibility for arbitrary graphene patterning via non-contact and maskless fabrication processes which reduces the fabrication cost. More importantly, LDW can achieve a single-step fabrication of the graphene patterns by combining the graphene growth and patterning steps, resulting in a significantly enhanced efficiency²⁴. Recently, two main LDW methods were reported for the fabrication of graphene patterns. One is the laser-induced localized thermal reduction of graphene oxide (GO) films^{23,25}. The other is the LDW of graphene patterns on Ni foils via a localized laser-assisted CVD process^{24,26}. In both methods, simultaneous graphene growth and patterning have been achieved via a single-step writing process.

Despite the progress made so far, there are still several serious issues remaining in the existing methods, which need to be addressed to achieve low-cost, large-scale nanofabrication of graphene patterns. For the thermal reduction of GO films, the as-reduced graphene still contains a substantial amount of defects; and the carbon-

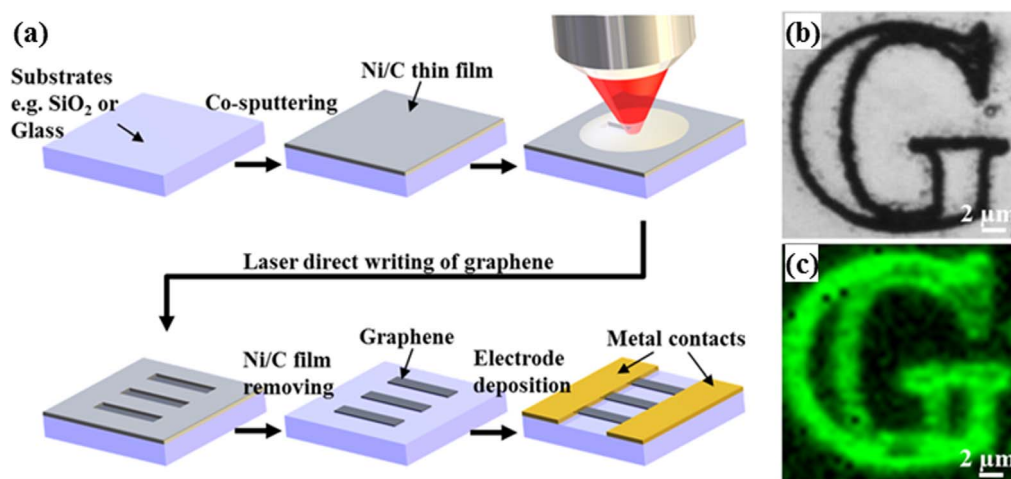


Figure 1 | (a) Schematic of the LDW process to fabricate graphene patterns under ambient conditions; (b) Optical micrograph and (c) Raman 2D band mapping image of the as-fabricated graphene patterns on a glass substrate.

oxygen bonds (e.g., C=O and C-O) cannot be completely eliminated, which limits the conductivity of the graphene patterns. The reduced GO films also demonstrate a relatively large sheet resistance in the $K\Omega/\text{sq}$ range²³, and a comparatively low carrier mobility ranging from $0.1 \sim 10 \text{ cm}^2/\text{V sec}$ ^{27–29}. For the laser-assisted CVD of graphene patterns on Ni foils, the graphene quality was significantly improved. The sheet resistance of the as-fabricated bi-layer graphene can reach about $400 \Omega/\text{sq}$ by the laser-assisted CVD process²⁶. However, in the established laser-assisted CVD methods, the graphene growth generally requires a closed-chamber environment filled with explosive hydrocarbon precursors (CH_4/H_2) and a post-growth graphene transfer process^{24,26}. Therefore, a cost-effective method for fabricating large-scale graphene patterns on insulating substrates under ambient conditions is still absent.

In this study, we find that bi-layer graphene can be synthesized through rapid heating of co-sputtered Ni/C thin films on various insulating substrates. By applying a femtosecond laser direct writing (Fs-LDW) technique, open-air and room-temperature nanofabrication of arbitrary graphene patterns on insulating substrates (e.g., glasses and SiO_2/Si) has been established. The nanofabrication method enables the cost-effective fabrication of graphene patterns directly on insulating substrates without a subsequent graphene transfer process. Scanning electron microscopy (SEM) and atomic force microscopy (AFM) characterization of laser scan paths show that the Ni thin film was evaporated after the laser irradiation, leaving the graphene patterns with certain doping of Ni nanoparticles on the insulating substrates (Supplementary Information, Fig. S1). Various graphene patterns, including texts, spirals, parallel lines, and layouts of integrated circuits (ICs), were demonstrated. Compared with previously established laser-based graphene fabrication methods, our method has unique advantages, including: (a) The quality of graphene obtained by our method is comparable to that of laser-assisted CVD (the sheet resistance is about two times lower than the bi-layer graphene fabricated by the laser-assisted CVD) and is much better than the reduced GOs (the sheet resistance is one order of magnitude lower than the reduced GOs); (b) This method does not need vacuum chambers and high substrate temperatures for the graphene synthesis as required by the laser-assisted CVD method. In contrast, graphene patterns can be fabricated under ambient conditions by this method; (c) This method can be used to deposit graphene patterns directly on the dielectric substrates without the need of graphene transfer steps which are required in CVD-based methods. Therefore, the LDW method developed in this study is more convenient than the laser-assisted CVD methods for various graphene-based applications.

Results

Figure 1b shows a “G” character graphene pattern under an optical microscope. The formation of graphene is evidenced by the 2D band Raman mapping (Fig. 1c) which clearly shows a G-shaped pattern precisely replicating the image in Fig. 1b. Besides, the uniform color contrast of the Raman mapping image indicates the homogeneous growth of graphene via the LDW process. In this study, it is interesting to see that by heating the co-sputtered Ni/C thin film using the fs laser irradiation, graphene synthesis with a much faster growth rate and a much lower substrate temperature can be achieved as compared with the conventional thermal heating in a vacuum. Control experiments of graphene growth via the fs-LDW process and the rapid thermal annealing process¹⁹ were conducted (Supplementary Information, Fig. S2). Results show that bi-layer graphene can be rapidly grown by the laser scanning of Ni/C thin film at a speed of $500 \mu\text{m/s}$, indicating the graphene formation occurs in $< 2 \text{ ms}$ under the laser irradiation (given the laser spot size of $\sim 800 \text{ nm}$). However, for the thermal annealing process, no obvious bi-layer graphene growth was observed even after 2 min heating at 600°C in a vacuum. Bi-layer graphene can be only grown at a much higher substrate temperature of about 1100°C in the thermal annealing process.

Various graphene patterns are further demonstrated in Figs. 2a to 2d, including a “Graphene” text pattern (Fig. 2a), a spiral pattern (Fig. 2b), arrays of lines (Fig. 2c), and an interconnection layout of a NAND logic circuit (Fig. 2d). The feature line-width of the as-fabricated graphene patterns, which is defined by the focal spot size of the fs-LDW system, is confirmed to be around 800 nm as shown in Fig. 2e. Clear G and 2D bands are observed in a typical Raman spectrum (Fig. 2f) which confirms the formation of graphene on the insulating substrates. The 2D/G band ratio is close to 1, indicating the formation of bi-layer graphene³⁰. A weak D band is also observed in the Raman spectrum due to the existence of graphene edge defects, which is a characteristic of the submicron graphene lines³¹. Transmission electron microscopy (TEM) of the as-fabricated graphene patterns transferred onto Cu grids has also been conducted. By characterizing the edges of the graphene, the bi-layer structure was clearly observed as shown in Fig. 2(g), which confirms the formation of bi-layer graphene in the LDW method. The optical transmittance of the graphene fabricated via large-area laser scanning on glass substrates were also obtained as shown in Fig. 2(h). The as-fabricated graphene has a high optical transparency ($> 88\%$) in the wavelength range from $300 \sim 800 \text{ nm}$. The as-measured optical transmittance of the graphene fabricated by the LDW method is 94.3% at 550 nm which is consistent with the property of bi-layer graphene³².

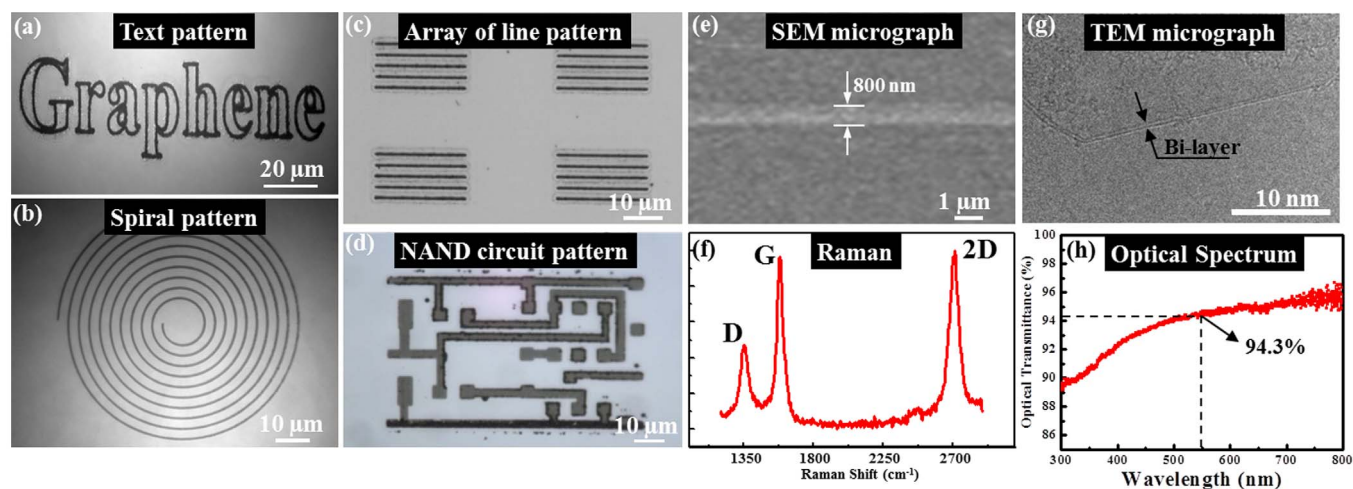


Figure 2 | Characterization of the as-fabricated graphene patterns. Optical micrographs of (a) “Graphene” text pattern on a glass substrate, (b) a graphene spiral pattern on a glass substrate, (c) arrays of graphene lines on a glass substrate, (d) a NAND circuit pattern on a SiO₂/Si substrate. (e) An SEM micrograph of a graphene line. (f) A typical Raman spectrum of the graphene patterns. (g) A TEM micrograph of the graphene transferred on a Cu grid. (h) An optical transmittance spectrum of the graphene film on a glass substrate fabricated by the LDW method.

Discussion

It is clear that the fs-LDW process has unique advantages over the conventional thermal annealing process on graphene growth. First, the highly efficient energy delivery by the laser beams enables the rapid heating of the Ni/C thin film and hence leads to a significantly enhanced growth rate of graphene. Second, the rapid laser heating process can leave the substrates at a much lower temperature than that in a thermal annealing process with global substrate heating. Therefore, the fs-LDW process enables the low temperature graphene growth on various desired substrates which cannot survive in the typical graphene synthesis processes by conventional thermal annealing techniques.

It is known that the graphene quality, such as the layer number and crystallinity of graphene, directly determines the properties of the graphene patterns (electrical, optical, mechanical, and thermal properties). In this study, the dependence of graphene quality on laser average power (focal spot size: ~800 nm) was systematically studied using Raman spectroscopy. The Raman spectra of the graphene patterns show that the variation in fs laser average power indeed affects the graphene quality (Figs. 3a and 3b). When a low laser average power of 12 mW was used, the as-fabricated graphene line shows a relatively large D band and a small 2D band, indicating that the as-fabricated graphene line contains multiple graphene layers (number of layers ≥ 3) and possesses a relatively large amount of defects. As the laser average power increases to 24 mW, the intensity of the D band of graphene decreases with respect to the G band; and the 2D band increases to about the same intensity of the G band. The changes in the Raman spectra indicate that the crystallinity of the graphene lines improves with the formation of bi-layer graphene as the fs laser average power increases from 12 to 24 mW. However, as the fs laser average power further increases from 24 to 48 mW, the D band of the graphene increases again, indicating the formation of additional defects with the excessive laser average power above 24 mW. The Raman peak ratios of D/G and 2D/G as the functions of laser average power are shown in Fig. 3b. It indicates that the as-grown graphene lines have the lowest D/G ratio and the highest 2D/G ratio at a laser average power of 24 mW, which is an optimal condition for fabricating high-quality graphene patterns. Laser average powers above or below 24 mW will result in an increased D/G ratio and a decreased 2D/G ratio, indicating the quality degradation of the graphene patterns. On one hand, the graphene lines are not efficiently synthesized with laser average power below 24 mW due to the insufficient heating during the laser irradiation. On the other

hand, high laser average power (>24 mW) will also induce damages in the graphene lattice³³. Based on the control experiments, the optimal laser average power of 24 mW is obtained for the graphene growth. It is noted that the fs laser fluence used in our LDW process is less than 0.1 J/cm², much lower than fs laser ablation thresholds of borosilicate glass (1.7 J/cm²) and SiO₂/Si (1.2 J/cm²), respectively^{34,35}. Therefore, no substrate damages would occur during the LDW process.

Under the optimized condition for high-quality graphene growth, the fabrication of large-scale graphene patterns has been realized. We have developed a semiautomatic fabrication process with software capable of converting a normal Geometric Data Stream (GDSII) file of an integrated circuit (IC) layout (Fig. 3c) into a General Writing Language (GWL) file which is readable by the LDW system (Fig. 3d). Therefore, the LDW system can automatically write the graphene patterns on insulating substrates according to the “GWL” file as shown in a recorded video (Supplementary Information, video of the LDW process). Large-scale graphene-based IC patterns have been easily fabricated as shown in Fig. 3e (also see Supplementary Information, Fig. S3). The successful fabrication of the complex graphene-based IC patterns clearly demonstrates the capability and reliability of the LDW method.

To investigate the electrical properties of the graphene patterns produced under the optimal LDW condition (laser average power: 24 mW, writing speed: 500 μ m/s), various graphene patterns with Au contacts were fabricated and tested. Fig. 4a shows an electrical device structure with four Au electrodes intersected with an array of parallel graphene lines for sheet resistance measurements. The inter-line spacings of the graphene channels and the Au electrode patterns are 40 and 50 μ m, respectively. The *I*-*V* curve of the electrical devices shows a linear dependence between the channel current and the voltage drop, indicating the metallic characteristics of the graphene lines (Fig. 4b). The sheet resistance of the as-fabricated graphene patterns was measured to be 205 ± 19 ohm/sq via the four-probe measurement method, showing a high electrical conductance of the graphene patterns. Comparing with the bi-layer graphene grown via the laser-assisted CVD method (~400 ohm/sq)²⁶, our work further reduces the sheet resistance of the graphene patterns by a factor of 2. The high electrical conductance of the as-fabricated graphene patterns is believed to be ascribed to the following two factors: a) relatively high-quality graphene preserved by the transfer-free growth process; and b) the existence of Ni doping (Supplementary Information, Fig. S4 and Table S1) which are expected to enhance the electrical conductance of the graphene sheets^{36,37}. Due to the high

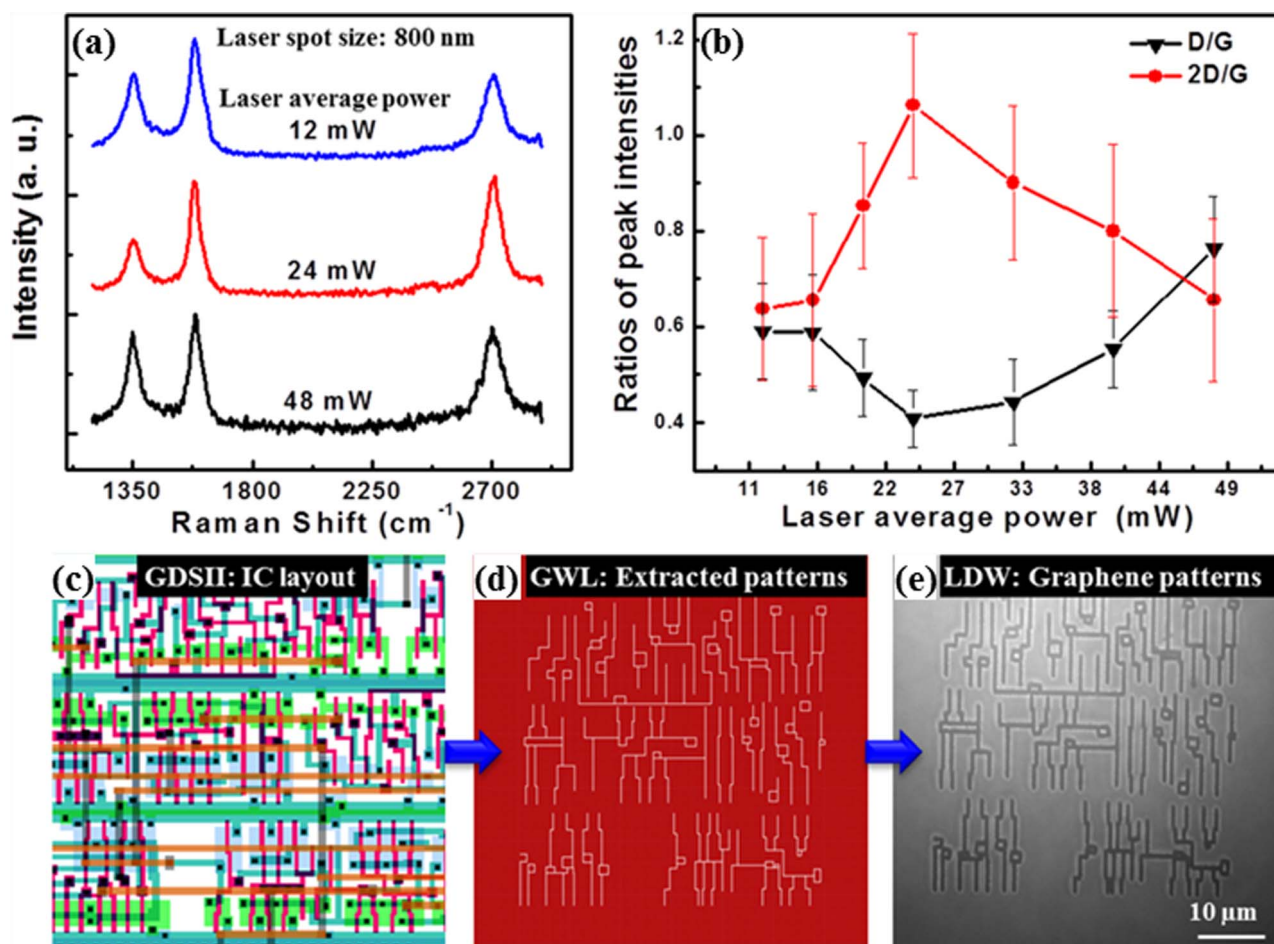


Figure 3 | Dependence of the graphene quality on laser average powers. (a) typical Raman spectra of the graphene lines fabricated with three different laser average powers, including 12, 24, and 48 mW, and (b) Raman D/G and 2D/G ratios of graphene lines as functions of laser average power. Fabrication of large-scale graphene patterns for integrated circuit (IC) application: (c) an IC layout in the GDSII format, (d) an extracted metal layer layout in the GWL format, and (e) the fabricated graphene patterns on a glass substrate.

electrical conductance, the as-fabricated graphene patterns are promising for various applications such as transparent electrodes, solar cells and smart windows.

To further characterize the carrier density and mobility of the as-fabricated graphene patterns, Hall effect measurements were

conducted. As shown in Fig. 4c, a Greek-cross graphene pattern was adopted in the Hall effect measurements due to two reasons: a) the low measurement error of the Greek-cross pattern as a van der Pauw test structure³⁸ and b) the simple pattern geometry which can be easily fabricated by the LDW method. Four Au electrodes were

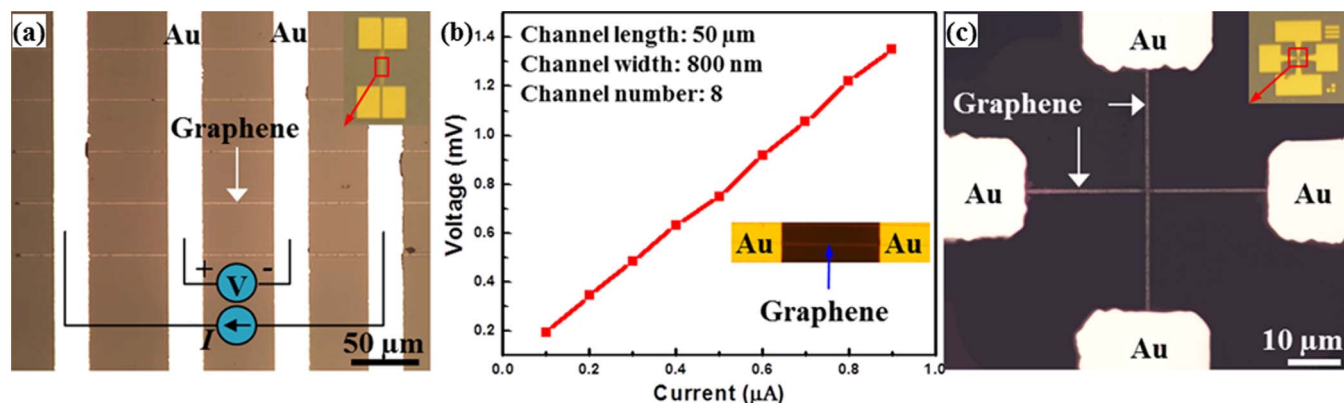


Figure 4 | Electrical characterization of graphene devices fabricated by the LDW method. (a) An optical micrograph of a four-terminal device for sheet resistance measurements. (b) *I-V* curve of the four-terminal electrical device with eight graphene straight line channels as shown in a, the inset show an optical micrograph of one graphene channel between two Au contacts. (c) An optical micrograph of an electrical device with (a) Greek-cross graphene pattern for Hall measurements. The insets in (a) and (c) show the zoomed-out optical micrographs of the parallel line and cross-bar graphene devices, respectively.



precisely deposited at the ends of the Greek-cross graphene pattern via conventional photolithography and lift-off techniques. By following the standard Hall measurement procedure (provided by the National Institute of Standards and Technology), the electrical properties of the as-fabricated graphene patterns were obtained. The majority carrier in the graphene patterns is found to be the hole, indicating the p-type doping of the graphene patterns. The average sheet carrier density and mobility of the as-fabricated graphene at room temperature were measured to be $(11.9 \pm 2.7) \times 10^{12} \text{ cm}^{-2}$ and $95.7 \pm 6 \text{ cm}^2/\text{V sec}$, respectively, which are comparable to the published results³⁹. It is noted that the graphene synthesized by the thermal CVD method usually has a high carrier mobility of several thousand $\text{cm}^2/\text{V sec}$ at room temperature⁴⁰. Therefore, the carrier mobility of the as-fabricated graphene by the LDW method at ambient conditions is lower than that of the high-quality graphene fabricated by the CVD methods, which is believed to be ascribed to the existence of carrier scattering sites by the Ni doping. However, as compared with the reduced GO patterns, the graphene patterns fabricated by our LDW method show a much higher carrier mobility and electrical conductance (for reduced GOs, carrier mobility: $0.1 \sim 10 \text{ cm}^2/\text{V sec}$; sheet resistance in $\text{k}\Omega/\text{sq scale}$)^{23,27–29}, suggesting a significant improvement of the graphene performance achieved by the LDW method. Moreover, comparing with the conventional CVD based methods which generally requires a temperature of $\sim 900^\circ\text{C}$ and Cu substrates for the graphene growth, this LDW method has several apparent advantages: 1) capability to achieve graphene growth at ambient conditions which allows the direct integration of graphene with many external material systems of low heat resistance such as ordinary glasses; 2) direct growth of graphene on target substrates without tedious transfer process; and 3) high flexibility and simplicity for fabricating complex graphene patterns on target substrates, which opens a door for fabricating various advanced graphene-based devices.

In conclusion, a cost-effective LDW method for fabricating graphene patterns under ambient conditions has been developed. Rapid graphene growth via laser heating of co-sputtered Ni/C thin films has been achieved at room temperature. Complex graphene patterns have been directly grown on glass and SiO_2/Si substrates by a fs laser beam combined with a high resolution X-Y piezo stage. The developed fabrication method successfully eliminates the use of a vacuum chamber as required in the thermal CVD process and enables the transfer-free growth of complex graphene patterns on insulating substrates with low thermal resistances. The sheet resistance and carrier mobility of the as-fabricated graphene patterns have been characterized to be $205 \pm 19 \text{ ohm/sq}$ and $95.7 \pm 6 \text{ cm}^2/\text{V sec}$, respectively, indicating a significant performance enhancement over the reduced GO patterns fabricated by LDW methods. Considering the high simplicity, flexibility, and reliability in producing graphene patterns, the LDW method developed could open a door for fabricating a wide range of advanced graphene-based devices.

Methods

Laser direct writing of graphene. The schematic of the fabrication process for the LDW of graphene patterns is shown in Fig. 1a. First, the cleaned insulating substrates (e.g., glasses or SiO_2/Si) were deposited with amorphous C and Ni films via direct current (DC) magnetron co-sputtering technique (ATC Orion 5 UHV, AJA International, Inc.; Sputtering power: 90 W for C and 15 W for Ni, co-sputtering time: 15 min, Ni/C film thickness: 45 nm, Ni/C atomic ratio: 10:1) using graphite (Kurt J. Lesker, 99.999% purity) and nickel (Kurt J. Lesker, 99.995% purity) targets at room temperature. Then, a controlled femtosecond (fs) LDW process under ambient conditions using a Photonic Professional LDW System (Nanoscribe GmbH) was conducted for directly writing graphene patterns on the substrates. A 780 nm fs laser (pulse width: 120 fs, pulse repetition rate: 100 MHz) was focused on the Ni/C thin film to induce localized heating to facilitate the graphene growth. The graphene formation in the LDW process follows a similar solid-state transformation mechanism as reported in our previous study¹⁹. Prior to the LDW process, a layer of immersion oil (Immersion oil Immersol 518 F fluorescence free) was applied on the surface of the Ni/C film to prevent the potential Ni oxidation. No vacuum and additional substrate heating are required in the LDW process. By moving the sample with respect to the focused laser beam using a high-resolution piezo stage (spatial

resolution: 5 nm, scanning speed: 500 $\mu\text{m/s}$), arbitrary patterns of graphene lines were formed directly on the insulating substrates without any graphene transfer process. The whole LDW process was monitored by a charged coupled device (CCD) camera installed on the Photonic Professional LDW system (Nanoscribe GmbH). After the LDW of graphene patterns, the immersion oil atop the graphene patterns was removed by acetone and methanol cleaning. The remaining Ni/C thin film was then removed simply by a wet chemical etching process (Type I Ni etchant, Transene Inc.), leaving only the graphene patterns on the substrates. Graphene devices were fabricated by depositing Au contacts on the desired regions of the graphene patterns via standard photolithography, lift-off and sputtering deposition (Kurt J. Lesker, 99.99% purity Au target) processes.

Characterization of graphene patterns. The surface morphologies of the graphene samples were characterized using a field-emission SEM (FESEM) (Hitachi S4700 FESEM system, 5 kV), a scanning probe microscope (SPM) (Digital Instruments Nanoscope IIIa Dimension 3100 SPM system) and an optical microscope (Nikon Eclipse LV150). A field-emission transmission electron microscope (FEI Tecnai G2 E30) was used to observe the layer structures of the graphene. The Raman characterization of the graphene samples was conducted with a Renishaw InVia Raman microscope with an excitation wavelength of 514.5 nm and a spatial resolution of $\sim 1 \mu\text{m}$. The Raman mapping was carried out with a grid spacing of 0.25 μm and an accumulation time of 3 seconds at each spot. The *I-V* characterization of the graphene samples were conducted using a semiconductor parameter analyzer (Agilent HP4145C). The sheet resistance measurements were conducted with a home-built four-probe measurement system consisting of a Keithley 2601B sourcemeter and a Keithley 2182A nanovoltmeter. The Hall effect measurements of the graphene devices were conducted at room temperature with a magnetic field of 14600 Gauss produced by a GMW Magnet system (model 5403 electromagnet). The transmittance was measured using a UV-visible spectrophotometer (Thermo Scientific Evolution 201).

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Author contributions

W.X. conceived the idea. W.X. and W.J.H. performed the sample preparation and graphene characterization. W.X., L.J.J. and L.S.F. performed the LDW fabrication. Y.G. and L.J.J. helped with TEM and software programming. W.X. and Y.S.Z. co-wrote the paper. Y.S.Z. and Y.F.L. performed the paper revision. Y.F.L., L.J. and J.F.S. contributed significant discussion and final paper polishing. The manuscript was written through contributions of all authors.

Additional information

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