



**HAL**  
open science

# An Adaptive Output Impedance Gate Drive for Safer and More Efficient Control of Wide Bandgap Devices

Romain Grézaud, François Ayel, Nicolas Clément, Jean-Paul Rouger,  
Jean-Christophe Crébier

► **To cite this version:**

Romain Grézaud, François Ayel, Nicolas Clément, Jean-Paul Rouger, Jean-Christophe Crébier. An Adaptive Output Impedance Gate Drive for Safer and More Efficient Control of Wide Bandgap Devices. IEEE WipDa 2013, 2013, Columbus, United States. 10.1109/WiPDA.2013.6695564 . hal-00988293

**HAL Id: hal-00988293**

**<https://hal.science/hal-00988293>**

Submitted on 25 Feb 2021

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



Distributed under a Creative Commons Attribution 4.0 International License

# An Adaptive Output Impedance Gate Drive for Safer and More Efficient Control of Wide Bandgap Devices

Romain GREZAUD<sup>1,2</sup>, François AYL<sup>1</sup>  
<sup>1</sup>MINATEC – CEA/LETI  
17 rue des Martyrs  
38054 Grenoble Cedex 9 – FRANCE  
romain.grezaud@cea.fr

Nicolas ROUGER<sup>2</sup>, Jean-Christophe CREBIER<sup>2</sup>  
<sup>2</sup>Univ Grenoble Alpes, G2Elab, CNRS  
38400 Grenoble, FRANCE  
nicolas.rouger@g2elab.grenoble-inp.fr

**Abstract**—This paper presents an adaptive gate drive circuit to provide a safer and more efficient control of Wide Bandgap Devices (WBD). The gate drive circuit fabricated in AMS0.35 $\mu$ m HV CMOS technology has an adaptive output impedance for optimal turn-on/off driving conditions and a gate side power transistor switching transition detection. Its impedance can be precisely adjusted from 0.7 $\Omega$  to 12.5 $\Omega$  during transition time accordingly to the switched current to reduce overvoltage due to parasitic inductances. It can also be set to maintain the same transition times of WBD over operating point and temperature variations. Therefore, in an 800 kHz switching frequency synchronous buck converter based on WBD, the proposed gate drive circuit demonstrates secure but drastic dead-time reduction with a peak performance gain of 20% compared to a fixed dead-time of 50ns.

## I. INTRODUCTION

Wide Bandgap Devices (WBD) as GaN HEMTs and SiC JFETs offer outstanding performances for high switching frequency, high power density and high temperature applications. They are expected to be used in many power converters where silicon devices are less efficient [1], [2] or cannot even operate properly, especially at high frequency [3] and high temperature [4].

But for their implementation at an industrial scale, the reliability of WBD into power converters must reach a very high level. That will only be possible with technological process improvements but also with a development of a specific gate drive circuit. Indeed, these new devices require more attention on the gate side compared to their counterpart in silicon because of the small turn-on energy and very fast transition time [5]. Moreover most of GaN HEMTs and some SiC JFETs do not have built-in body diode [1-2]. As a result, operation of H bridges in the third quadrant is different or even prohibited without the addition of discrete antiparallel diodes.

An adaptive output impedance drive technique has been already presented in [6] in order to minimize the difference in the turn-on/off delay times between parallel connected IGBTs.

Based on WBD characteristics, we introduce a specific adaptive gate drive circuit to adjust its output impedance with

respect to the operating point and temperature variations to provide optimal turn-on/off driving conditions. Thus the presented driving technique can reduce overvoltage due to parasitic inductances and can also maintain the same transition time to perform secure dead-time reduction.

The present paper is organized as follow. Section II introduces the characteristics of WBD without body diode and their impacts on operations of H bridges. The detailed design of the gate drive is described in section III and section IV gives the experimental results of the drive circuit into a synchronous buck converter based on WBD.

## II. IMPACT OF WIDE BANDGAP DEVICES ON CONVERTER OPERATIONS AND GATE DRIVE DESIGN

### A. Switching characteristics

The attractive switching characteristics of a GaN device have been demonstrated at 350V/20A in a boost converter in [5]. The chosen WBD is a SiC-JFET [7] with a drain voltage and current slew rate of 60V/ns and 1.7A/ns. The turn-on energy being only 160 $\mu$ J, the risk of undesired switching is very important during fast transitions. Indeed, the gate driver is connected to the power transistor gate and source through parasitic inductances as  $l_{OUTH}$  and  $l_{OUTL}$  on half-bridge H of Fig. 1. Moreover, when the LX node is switched, a current  $I_{gd}$  given by (1) is circulating into the gate/drain capacitance  $C_{gd}$  and is evacuated by the driver.

$$|I_{gd}| = C_{gd} \cdot \frac{|\Delta LX|}{\Delta t} = C_{gd} \cdot \frac{|\Delta V_{ds}|}{\Delta t} \quad (1)$$

Thus when the voltage slew rate is too important  $I_{gd}$  becomes significant and the driver cannot evacuate it. If  $I_{gd}$  is positive it will charge the gate/source capacitance  $C_{gs}$  beyond the threshold voltage  $V_{th}$  putting back the power transistor into conduction. There are two possibilities to attenuate this phenomenon: to adapt the driver and to bring it very close to WBD in order to reduce parasitic inductances, or/and to adapt the driver to slow down switches and reduce  $I_{gd}$ , while increasing switching losses.

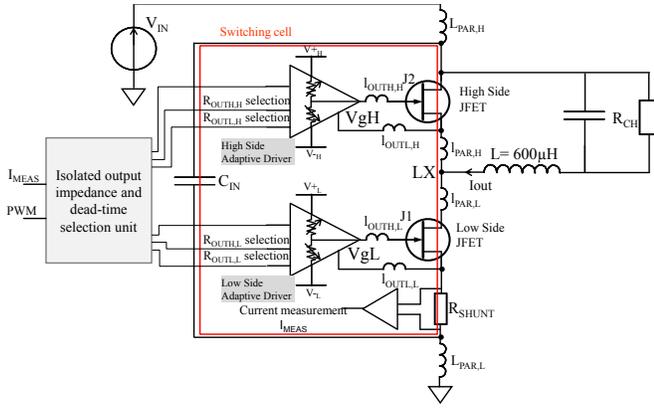


Figure 1. Schematic of synchronous buck converter based on two WBD driven by the adaptive gate drive circuit

The other impact of the WBD high switching speed into the converter is the overvoltage between the drain and source terminals due to parasitic inductances ( $I_{par,L}$  and  $I_{par,H}$ ) into the switching cell of Fig. 1. When the current slew rate is too important the drain/source voltage  $V_{ds}$  exceed the maximum breakdown voltage  $BV_{ds}$ . Another possibility is to reduce the parasitic inductance values while working on novel packaging and integration schemes.

### B. Reverse conduction characteristics

The chosen SiC-JFET [7] is a pure vertical channel device in opposition to SiCED JFET which have a combined lateral-vertical channel design [8]. Compared to the SiCED JFETs, pure vertical SiC-JFET do not have a parasitic body diode which can be used as a freewheeling diode. This parasitic body diode between drain and source is also not present into the HEMT structure of GaN and GaAs transistors [1-3].

Although WBD HEMTs and some JFETs do not have a body diode, they do present the ability to conduct a reverse current and offer freewheeling states. A DC measurement of the reverse conduction characteristics has been performed for the SiC-JFETs. Fig. 2 shows that reverse conduction characteristics depend on the gate voltage  $V_{gs}$  when this latter is below  $V_{th}$  (in this case  $V_{th}$  is equal to  $-4.5V$ ). In these conditions, the lower the gate voltage is, the higher the reverse drain source voltage  $V_{ds}$  is, as it is shown by (2).

$$V_{ds}|_{I < 0 \text{ \& } V_{gs} < V_{th}} = V_{gs} - V_{th} \quad (2)$$

WBD without body diode conduct the reverse current directly through their channels. Consequently, the reverse-recovery charges are negligible compared to conduction through body diode. On the other side during dead-times into synchronous converter based on WBD every power transistors are switch off ( $V_{gs} < V_{th}$ ) to prevent power supply from short circuits. The whole output current  $I_{out}$  circulates anyway through one or more transistors (J2 on Fig. 1) which are then into conditions of (2) where  $V_{ds}$  are not negligible. The reverse conduction losses due to dead-time  $t_{dt}$  are given by (3).

$$P_{dead\ time} = (V_{gs} - V_{th}) \cdot I_{out} \cdot f_{sw} \cdot 2t_{dt} \quad (3)$$

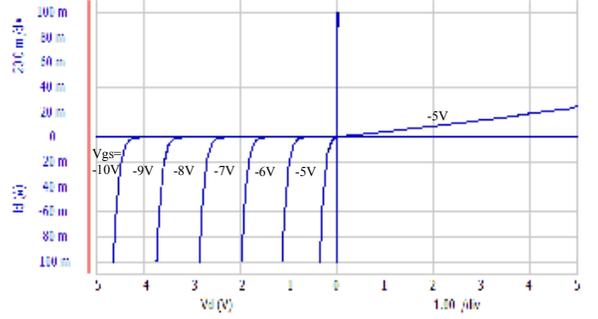


Figure 2. Forward and reverse conduction characteristics of SJD120R085 SiC-JFET without internal body diode for different gate voltages

In a synchronous buck converter losses generated by dead time  $P_{dead\ time}$  have an impact on the reliability of WBD but also on the converter efficiency. Especially for high switching frequency  $f_{sw}$  and low output voltage  $V_{out}$  [9]. In the view of securing and improving operations of synchronous converters without diodes, a very short dead-time is definitely desired.

### III. DESIGN OF A SPECIFIC GATE DRIVE CIRCUIT FOR A CONVERTER BASED ON WIDE BANDGAP DEVICES

The proposed gate drive circuit has been specifically designed for WBD to drive them in a safe and effective way into a synchronous converter.

#### A. A secure and efficient synchronous buck converter

The switching cell of the synchronous buck converter visible on Fig. 1 is made of two SiC-JFETs, a high-frequency capacitance and a low parasitic shunt for high-frequency current measurement. Each JFET is driven by one floating adaptive gate drive which receives switching orders and output impedances selections from an isolated and external control unit.

This unit can set the output impedance of the gate driver according to the PWM signal and the desired output current to secure WBD operations. Indeed, slowing down switches can be an option when current transitions are too fast. The overvoltage between drain/source of power transistors can then be reduced and undesired switching due to fast voltage transitions can be avoided. The switching losses are however increased when the switching speed is reduced.

The control unit can also control the output impedances of drivers to balance the impacts of the operating point and the temperature on switching characteristics [10] and so maintain the same WBD transition times. In that case, every switching time is precisely known and so the dead time can be virtually deleted while remaining effectively protected against cross conduction and short circuit. Since the chosen SiC-JFETs don't have an integrated current sense, a discrete high-frequency current measurement is included into the switching cell to detect shoot-through and to adapt dead-time in consequence.

For the moment, the output impedances is set by the control circuit working as an open-loop system. The suitability of this selection depends on the chosen WBD switching characteristics and the converter design. A selection of the impedances based on a closed-loop system would permit to get an auto-adaptive output impedance gate drive capable of drive WBD in any

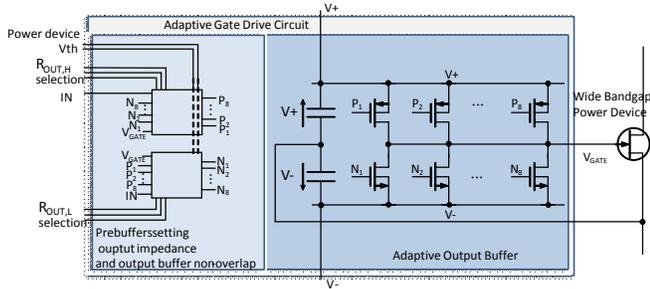


Figure 3. Block diagram of the adaptive gate drive circuit

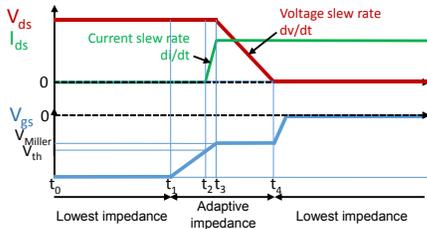


Figure 4. Switch on with the adaptive output impedance gate drive

converter without any calibrations. It is however difficult to implement such a solution because it requires high-voltage and high-frequency sensors, and overall, a very fast closed loop.

#### B. The adaptive output impedances gate drive circuit

The proposed gate drive circuit adapt its fall and rise output impedance between two switching periods and steady states by respectively adjusting the number of parallel NMOSs and PMOSs constituting the output buffer shown on Fig. 3.

The gate drive is made of the adaptive output buffer and prebuffers. These latters deal with the selection of the appropriate number of parallels transistors but also with the non-overlap protection of output buffer. In order to prevent the inherent CMOS cross conduction, the prebuffer of NMOSs (/PMOSs) can turn on their respective controlled switches only if it has received a turn off signal from PMOSs (/NMOSs).

Moreover, a detection of the power device switching state on the gate side is implemented in order to ensure the safest operations. Indeed, when the gate voltage  $V_{GATE}$  exceeds the miller plateau voltage  $V_{Miller}$ , the driver sets automatically the lowest impedance. In that way the output impedance selection is effective only during turn ON or turn OFF and parasitic switching can be avoided during steady states as shown on Fig. 4. The only requirement is that the miller plateau voltage of the wide bandgap power device must be externally set.

## IV. RESULTS

A photograph of the converter and the layout of the adaptive gate drive are shown on Fig. 5. The driver has been fabricated in AMS  $0,35\mu\text{m}$  HV. The die area is almost  $3,8\text{ mm}^2$ .

The output buffer can precisely control WBD thanks to different sizes PMOSs and NMOSs in parallel which can be independently selected. Its rise and fall output impedances have been measured and they are almost equal. As a consequence, it is then possible to drive WBD with an output impedance from  $0,7\Omega$  to  $12,5\Omega$  during turn on and turn off.

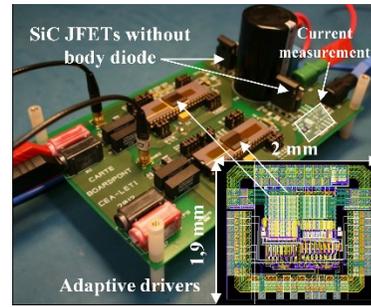


Figure 5. Synchronous converter made of SiC-JFETs without body diodes driven by the adaptive gate drive circuit

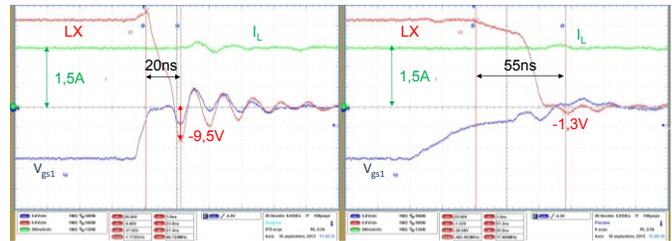


Figure 6. Fast and slow turn on of the SiC-JFET driven by the adaptive gate drive circuit into the lowest and the highest output impedance mode

#### A. The adaptive gate drive secure operations of fast switching wide bandgap devices into the converter

As one can see on Fig. 5 the two  $1200\text{V}/17\text{A}$  SiC-JFETs are not very close to each other. So the connections between the JFET and its driver are definitely not optimized for low parasites. The design of the converter is not specifically adapted to high frequency switching characteristics of WBD. And so parasitic inductances into the switching cell ( $I_{PAR}$ ) and between the driver and the power transistor ( $I_{OUTH}$  and  $I_{OUTL}$ ) shown on Fig. 1 are not negligible.

Consequently, slowing down JFET the adaptive gate drive does secure the operations of WBD into a non-optimized converter design. Fig. 6 presents waveforms of converter when a voltage and current of only  $12\text{V}/1,5\text{A}$  are switched at two different speeds. When the rise output impedance of the low side driver is set to its minimum of  $0,7\Omega$  the middle LX node is switched on less than  $20\text{ns}$  at the turn on transition to reach a negative potential of  $-9,5\text{V}$ . The high side power transistor see an overvoltage of 38% which is critical at higher voltage where the overvoltage between drain and source can exceed the breakdown voltage. When the output impedance of the low side driver is set to its maximum of  $12,5\Omega$  the LX node of the buck converter is switched on almost  $55\text{ns}$  to reach a negative potential of only  $-1,3\text{V}$ . The high side transistor sees in this case an overvoltage of only 5%.

By extending switching times SiC-JFETs are well protected against overvoltage and parasitic switching. A compromise must however be performed between protection and switching losses. Indeed, switching loss is proportional to the turn on and turn off switching times, the average inductor current and the frequency. For a given WBD and a switched current, an optimal compromise exists for the switching time and the overvoltage and it must be known to the control circuit to set the safest and the most efficient output impedance.

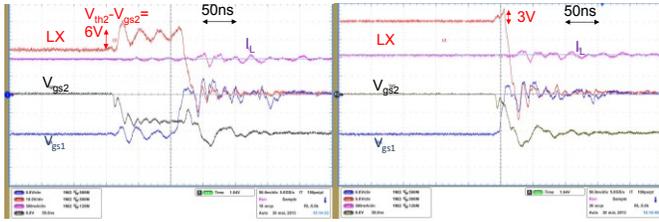


Figure 7. Synchronous buck converter waveforms with 100ns dead-time and with secure drastic dead-time reduction

### B. Safer and more efficient operations of wide bandgap devices without body diode

Accordingly to (3) we propose to virtually delete the dead time losses while reducing its value. Indeed, as one can see on Fig. 7, the operation of WBD without body diode into their reverse conduction mode is avoided when the transistor is below the threshold voltage.

The dead time is set to a fixed value for the first time and it will be reduced until the current measurement highlights a shoot-through. Then the dead time is incremented of one step by the control circuit [9]. Once the minimal dead-time is fixed the adaptive gate drive will secure operations by maintaining same transition times over operating point and temperature variations [10].

Measurements of the converter without diodes efficiency have been achieved on a wide output current range limited by the maximum current rate of the SiC-JFET [7] at 12V input voltage, 1,2V output voltage and a high switching frequency ( $f_{sw}=800\text{kHz}$ ). In that case reverse conduction losses are particularly important. In order to have the same transition times on the output current range, the output gate drive impedance is for now adapted manually function of the temperature and operating point dependence of the JFET switching characteristics. The converter efficiency with drastic dead time reduction is compared to the one with 50ns and 100ns dead time reduction. The results are shown on Fig. 8. A peak gain in performance of 20% compared to a 50ns dead time is reached for an output current of 16A.

The adaptation of the output gate drive impedance to maintain the same switching characteristics has demonstrated the possibility to virtually delete the dead time and so the antiparallel diodes while remaining secure. We found however that for the moment, this technique is difficult to implement. On one hand we can use an open-loop output impedance selection system but we must have a precise characterization of the operating point and temperature dependencies of the WBD performances. On the other hand to use a closed-loop system for the output impedance selection high voltage and high-frequency sensors are required.

## V. CONCLUSION

Impacts of these new wide bandgap power devices on a synchronous converter have been studied in this paper. It points out that for secure operations of high speed WBD the converter and the driver must be specifically designed to reduce overvoltage and parasitic switching due to parasitic inductances

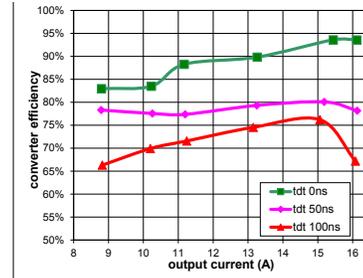


Figure 8. Experimental results of the synchronous buck converter without antiparallel diodes with and without dead-time function of the output current ( $V_{in}=12\text{V}$ ,  $f_{sw}=800\text{kHz}$  and  $V_{out}\approx 1,2\text{V}$ )

Moreover operation of WBD without body diode into an H bridge has been also studied. A lossy reverse conduction mode when the transistor is below the threshold voltage is responsible for important losses during dead time. An adaptive output impedance gate drive circuit has been fabricated in AMS  $0,35\mu\text{m}$  HV. The proposed gate driver can precisely control WBD with an adaptive output impedance from  $0,7\Omega$  to  $12,5\Omega$  between two switching periods by adjusting the number of parallel PMOSs and NMOSs. A control circuit adapt its output impedance according to the switched current to reduce overvoltage due to parasitic inductances until 80%. It can also be set to maintain the same WBD switching characteristics over operating point and temperature variations. Therefore, in an 800 kHz switching frequency synchronous buck converter based on WBD, the proposed gate drive circuit demonstrates secure but drastic dead-time reduction with a peak performance gain of 20% compared to a fixed dead-time of 50ns.

## REFERENCES

- [1] T. Morita, et al., « 99.3% Efficiency of three-phase inverter for motor drive using GaN-based Gate Injection Transistors », in APEC 2011, p. 481-484.
- [2] S. Ji, D. Reusch, and F. C. Lee, « High frequency high power density 3D integrated Gallium Nitride based point of load module », in ECCE 2012, p. 4267-4273.
- [3] V. Pala, H. Peng, P. Wright, M. M. Hella, and T. P. Chow, « Integrated High-Frequency Power Converters Based on GaAs pHEMT: Technology Characterization and Design Examples », IEEE Transactions on Power Electronics, vol. 27, n° 5, p. 2644-2656, May 2012.
- [4] T. Funaki, M. Sasagawa, and T. Nakamura, « Multi-chip SiC DMOSFET half-bridge power module for high temperature operation », in APEC 2012, p. 2525-2529.
- [5] B. Hughes, J. Lazar, S. Hulsey, D. Zehnder, D. Matic, and K. Boutros, « GaN HFET switching characteristics at 350V/20A and synchronous boost converter performance at 1MHz », in APEC 2012, p. 2506-2508.
- [6] M. Sasaki, H. Nishio, A. Shorten, and W. T. Ng, « Current Balancing Control for Parallel Connected IGBTs Using Programmable Gate Driver Output Resistance », in ISPSD 2013, in press.
- [7] « SemiSouth Normally-ON SiC-JFET 1200V/17A SJDP120R085 »
- [8] C. Cai, W. Zhou, and K. Sheng, « Characteristics and Application of Normally-Off SiC-JFETs in Converters Without Antiparallel Diodes », IEEE Trans. on Power Electronics, vol. 28, n° 10, p. 4850-4860, 2013.
- [9] S. Mappus, « Predictive Gate Drive Boosts Synchronous DC/DC Power Converter Efficiency », Texas Instrument Application Report SLUA281, April 2003.
- [10] R. Grezaud, F. Ayel, N. Rouger, and J.-C. Crebier, « A Specific Characterization Method for Evaluation of Operating Point and Temperature Impacts on Wide Bandgap Devices », in WiPDA 2013, in press.