Low Noise CMOS Analog Front-End Circuit With an 8-bit 1-MS/s ADC for Silicon Sensors for Space Applications

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Abstract

A low power analog front-end circuit for silicon (Si) detectors has been fabricated in 0.35 μm CMOS technology. It has been designed to read out signals from large-capacitance Si detectors for incident electron energy ranging from 50 keV to 725 keV. In order to quantify electron energy, the front-end integrates a charge preamplifier, a pulse shaper, a peak detector and an event-driven analog-to-digital converter (ADC). The complete front end including the ADC dissipates 2.5 mW for a maximum electron detecting rate of 650 kHz. The charge-to-voltage gain is approximately 60 mV/fC for a charge range of 0.6 fF to 32 fF. The measured equivalent noise charge (ENC) is 3119 e^- for a 40 pF detector parasitic capacitance.

Index Terms

Si Detector, Charge preamplifier, electron energy measurement.

I. Introduction

PARTICLE instruments incorporate sensors that are used to convert particle energy into quantifiable electrical charges. These sensors with their corresponding analog electronics circuits, also called Analog-Front-End (AFE), form detection channels called "sensor heads" [1]–[3]. The necessity to improve both spatial and spectral resolutions requires the design of multichannel integrated electronics. Thus, space-borne detectors with Application Specific Integrated Circuits (ASICs) should be developed. These integrated circuits allow not only to perfectly adapt the readout circuits to each sensor in order to optimize performances but also to benefit from the various advantages inherent to the use of CMOS technologies: reduced power consumption, smaller size, shorter transit time signals [4] and higher integration [5]. In this paper, the designed front-end circuits are more particularly optimized for a Si detector used to obtain the energy spectrum of incident electrons ranging from 50 keV to 725 keV with an energy resolution of 10 keV. More precisely, this ASIC has been developed to be associated with a detector of radiation belt electrons, outside the South Atlantic Anomaly, on a low altitude polar orbiting spacecraft. Radiation belt electron fluxes at 600 km altitude are weak and their measurement implies a large transmission factor. The size of the detector allows reaching a transmission factor of 4 cm^2.sr., which also allows to measure Lightning induced Electron Precipitation (LEP). Further, the spectrometer includes a collimator, which provides the possibility to obtain a rough pitch-angle distribution of the electrons (three directions).

A specific design methodology should be employed in order to withstand constraints due to space applications. The radiation environment can especially damage electronic systems on spacecraft and orbital satellite [6]. Two major radiation effects should be mentioned: the total cumulative dose called Total Ionizing Dose (TID) which is related to interactions between the semiconductor and the trapped particles, and transient events called Single Event Effects (SEE) resulting from high energy particles and random occurrences [7], [8]. Nowadays, instead of using technologies dedicated to space (such as specific BiCMOS or SOI) in order to improve the radiation hardness of integrated circuits, it seems appropriate to use specific design techniques (radiation hardening by design (RHBD)) [7], [9] applied on standard CMOS technologies which are less expensive [10], provide higher performances and for which parasitic effects are studied and well known [11], [12]. The choice of the technology depends first on the duration of the mission as well as on the radiative environments which is related to the space probe orbit trajectory. To fulfill this condition, we rely on studies of CMOS technologies radiation hardness already made by the scientific community [9]. Here, the sensor should be placed in a low Earth orbit satellite. It implies that the systems should withstand a 20 krad TID for a space mission duration of 2 years. A 0.35 μm CMOS technology has thus been chosen since it can naturally withstand more than 50 krad [9]. In particular, it was shown that for CMOS technologies with a thin oxide thickness, TID effects are greatly reduced by tunneling mechanism. Further, in one of our previous 0.35 μm CMOS design, it was shown that TID up to 360 krad can be tolerated [13]. Further, the High-Voltage process option (HV) has also been chosen so that guard rings could be extensively used to prevent as much as possible latchup event. In addition, digital noise

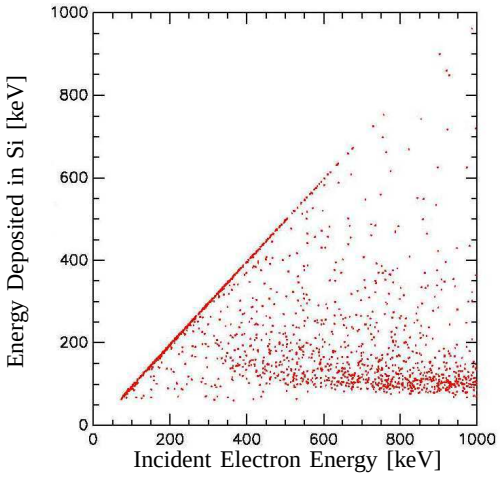

Fig. 1. GEANT4 Simulation of the energy deposited in a Si detector of 300μm thickness shielded by an aluminium foil of 6 μm thickness versus the incident electron energy. N=200000 incident electrons with a random incident angle $\theta \in [0;10^o]$ and a random azimuth angle from 0^o to 360^o.

that can affect the analog front-end in a mixed-signal circuit with both digital and analog circuits on a common substrate can be reduced by using triple well isolation available in HV technologies.

Here, in order to design and optimize the AFE circuits in terms of power consumption, linearity and noise, the main characteristics of the detector should be first extracted and modelled. Then, based on [14], some details about the front-end circuit design and its noise optimization are presented. Contrary to usual approches such as in [15], a differential input stage architecture has been preferred in order to be less prone to crosstalk issues between channels. Finally, simulation and measurement results are presented. A figure of merit (FoM) is also proposed to compare CMOS front-end circuits designed for various semiconductor detectors.

II. Si CMOS Front End Architecture

Firstly, determining the model of the Si detector is necessary to design the Si detector circuits. As it will be explained in the following sections, the main parameters of such a model are the following ones: (1) the charge collection time T_c, (2) the input parasitic capacitance C_{det} and (3) the leakage current I_0. After a short description of the Si detector model, these three parameters will thus be extracted.

A. The detector model

Here, the CMOS front-end is intented to be used with an electron energy spectrometer based on Si sensors. This instrument is intended to analyze the atmosphere-ionosphere-magnetosphere interactions during Transient Luminous Events (TLE) that can occur during atmospheric storms, in order to understand the physical mechanisms responsible for vertical impulsive coupling between the atmosphere and the ionosphere. The final aim is to assess the impact of these phenomena on the earth environment [16].

The Si detector is divided into four cells (10 mm x 10 mm) of 0.3 mm thickness and an aluminium foil of 6 μm thickness is used to shield it from incoming visible and ultra-violet light. Based on Geant4 (see [17]) simulation results, electrons with energy higher than 50 keV (due to aluminium foil) and lower than 500 keV can be detected with a relatively good linearity (see Fig.1). Within such an energy range, the average number of electron-hole pairs $n_{pair_{Si}}$ generated in the Si detector can be calculated as:

$$n_{pair_{Si}} = \frac{E_{in}}{\varepsilon_{Si}} \tag{1}$$

where E_{in} is the energy of the incident electron in eV and ε_{Si} the silicon ionization energy (ε_{Si}=3.62 eV).

For energy higher than 500 keV, electrons can go through the Si semiconductor without losing significant amount of energy and therefore another kind of semiconductor (such as CdTe) would be required to detect them. However, as shown in Fig. 1, electrons with energy higher than 500 keV, can still be detected but with a much reduced detection probability. Consequently, the electron energy detection range has been extended up to 725 keV.

Knowing the maximum charge collection time T_c^{max} is important as it defines the maximum operating frequency of the instruments. It can be expressed as:

$$T_c^{max} = \frac{d^2}{\mu_h \times V_0} \tag{2}$$

TABLE I
CHARACTERISTICS OF THE SI DETECTOR FOR V_0=40 V

Characteristics	Symbol	Si
size (mm)	$L \times l \times d$	$10 \times 10 \times 0.3$
generated pairs	-	13.9×10^3-2.01×10^5
Equivalent charge (fC)	Q_{in}	2.2 - 32
Collection time (ns)	T_c^{max}	≈ 50
Parasitic capacitance (pF)	C_{det}	34.8
Leakage current (nA)	I_0	2

where d represents the distance between the electrodes (which is approximately the Si thickness), μ_h the mobility of holes (450 $cm^2 \cdot V^{-1} \cdot s^{-1}$) and V_0 the voltage applied across the electrodes.

Furthermore, the parasitic capacitance of the semiconductors (SCs) detector should also be taken into account in its electrical model since both the AFE bandwidth and noise depend on its value as it will be shown later. The equivalent capacitance of the SC can then be expressed as:

$$C_{det} = \varepsilon_0 \varepsilon_r \frac{A}{d} \tag{3}$$

where A is the area of the electrodes, d the distance between them, ε_r=11.8 the relative permittivity of the Si material and ε_0=8.854$\times 10^{-12}$ F·m^{-1} the vacuum permittivity.

Finally, the leakage current I_0 should also be taken into account since it increases the AFE output noise, affects the AFE dynamic range and may also compromise the AFE normal operation. This current I_0 is dominated by thermally generated electron-hole pairs that are separated by the applied electrical field. The typical measured value of the Si-detector leakage current is 2 nA at 280 K which will be the maximal operating sensor temperature. Therefore, to design the circuit, a 10 nA current leakage has been chosen as a worst case.

Table I summarizes the main characteristics of the Si detectors. Based on this analysis, Si cells can be electrically modeled by a pulse current source I_{det} to simulate a charge injection in parallel with the equivalent capacitor C_{det} of the cell and the leakage current source I_0.

Knowing such parameters, the analog front end (AFE) consisting of the charge preamplifier (CPA) and pulse shaper (PS) can be designed.

B. The Analog front End Design

The designed AFE should be able to quantify the detected charge in order to reconstruct the electron energy spectrum. Consequently, the AFE should have a linear output response to ease the mapping of the electron energy. The first step is to convert charge into a voltage using a charge preamplifier (CPA) [1], [15]. The CPA consists of a transconductance amplifier (OTA) with a feedback capacitor C_f ($\approx$ 200 fF) to perform the charge integration and a resistor feedback R_f ($\approx$ 1.2 MΩ) to discharge C_f and to provide a DC path for the detector leakage current. Then, in order to improve the Signal-to-Noise Ratio (SNR), the CPA output voltage is filtered by a circuit called pulse shaper (PS). As in [14], a first order semi-Gaussian PS (RC-CR bandpass filter) is used as PS for its high-speed response and its active bandpass filtering characteristics. These two blocks are widely used for such detectors [1]–[3], [14], [18]. The CPA and PS are presented together with the Si detector model in Fig.3 where C_p represents the parasitic capacitance from the chip-sensor connection, the chip input pads and the CPA input capacitance.

The PS dynamic output range is set to $\Delta V_S^{PS_{max}}$=1.65 V in order to fit the input dynamic range of the ADC. Therefore, as stated in Table I, in order to be able to collect a charge up to 32 fC, the Si chain gain can be calculated as follows:

$$G_{CPA-PS} = \frac{\Delta V_S^{PS_{max}}}{Q_{max}} \approx 51.6 \ mV/fC \tag{4}$$

As previously mentioned, the maximum operating frequency f_{op-max} corresponds to the minimal shaping time of the PS $t_{s_{min}}$, which must be equal to the maximal collection time $T_{c_{max}}$ (see eq.2) of the charges generated by an incident electron going through the Si detector. $T_{c_{max}}$ is equal to 50 ns for our Si detector. Finally, to calculate the relaxation time of the chain, the conversion time of the SAR ADC must be taken into account. This ADC architecture has been chosen for reasons of low power consumption, small size and simplicity [19]. An 8-bits SAR ADC is used in adequacy in our application accuracy requirements and operates at a sampling frequency (f_{adc}) of 1 MHz. So, the conversion time t_{conv} set by the channel to discriminate is given by:

$$t_{conv} = \frac{1}{f_{op-max}} + \frac{1}{f_{adc}} + T_{reset} \tag{5}$$

with T_{reset} the time required ($\approx$ 200 ns) to reset the digital functions after the SAR ADC conversion. Note that t_{conv} does not take into account the delays through the other Si chain blocks as they are negligible compared to the shaping and conversion times.

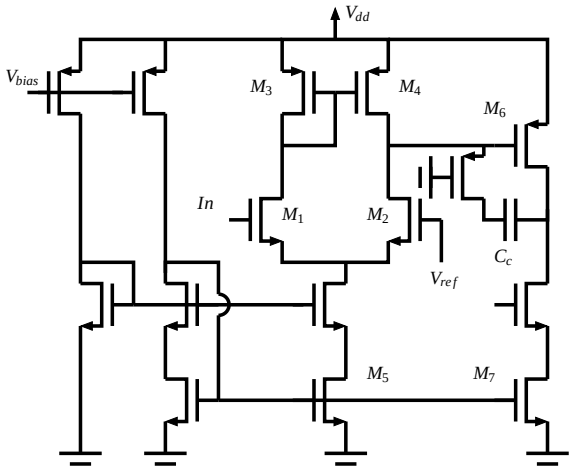

Fig. 2. Schematic of the operational transconductance amplifier (OTA) used as the charge preamplifier circuit

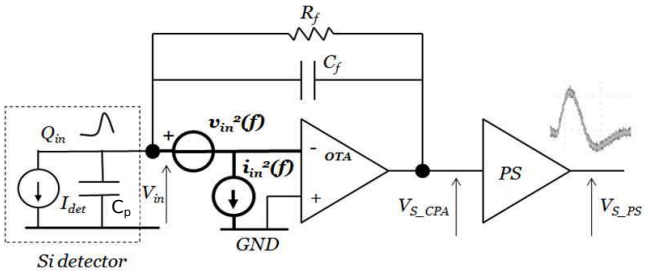

Fig. 3. Simplified AFE circuit diagram with Si detector model for noise analysis.

Furthermore, the maximum integration time is defined as the discharge time of the CPA+PS which corresponds to approximately 5 times the shaping time of the CPA+PS . This time must be inferior to the ADC conversion rate according to:

$$t_{s_{max}} = \frac{1}{5 \times f_{adc}} = 200\ ns \tag{6}$$

So, t_s can be increased from 50 ns up to 200 ns, which can be interesting to further reduce the circuit bandwidth and thereby the noise. However, t_s is set to be equal to 100 ns in order to add a safety margin because the reset time of the chain (ADC reset and discharge time of the peak detector capacitance) must be taken into account.

As far as noise is concerned, the AFE has been designed to reduce both the intrinsic and extrinsic noise. With the aim to use up to 4 channels on the same die, crosstalk between channels must be drastically reduced. This issue is of up most importance here as each channel includes a peak-detector and a SAR ADC. Therefore, to address this extrinsic noise, a differential input stage (Fig.2) is used instead of the usual single-ended architecture [14], [15]. Nevertheless, the equivalent input noise power spectrum is doubled compared to a single transistor amplification stage (if each transistor is biased by the same current), which corresponds to a noise increase by a factor of $\sqrt{2}$.

For the intrinsic noise, studies show that most of the noise is generated by the CPA input transistor [18]. This implies that it should be designed properly. Fig.3 shows the circuit diagram that can be used to determine the output noise voltage of the AFE. The Equivalent Noise Charge (ENC) defined as the ratio of the total output rms noise of the PS to the peak amplitude response to one electron input charge, can be optimized either to the detriment of the power consumption by increasing the drain current I_D or to the detriment of the bandwidth by increasing t_s [18]. Here, the PS is limited to a first order band pass filter, in order to reduce the power consumption and circuit complexity. Based on [14], the ENC of the system including the Si sensor, the CPA and the PS ENC_{tot} can be expressed as:

$$ENC_{tot} = \frac{e}{q}\sqrt{R^2\left(\frac{2}{3}\frac{kT}{gm_1 t_s} + \frac{K_f}{C_{ox}^2 (WL)_1}\right) + \frac{qI_t t_s}{16}} \tag{7}$$

$$\text{with } R = C_{det} + C_p + C_{gs_1} + C_{gd_1} + C_f$$

where k is the Boltzmann constant, q the elementary charge, T the temperature, K_f the 1/f flicker noise coefficient, I_t the sum of the detector leakage current and the equivalent input noise current of the input connection, gm_1 the M_1 transconductance,

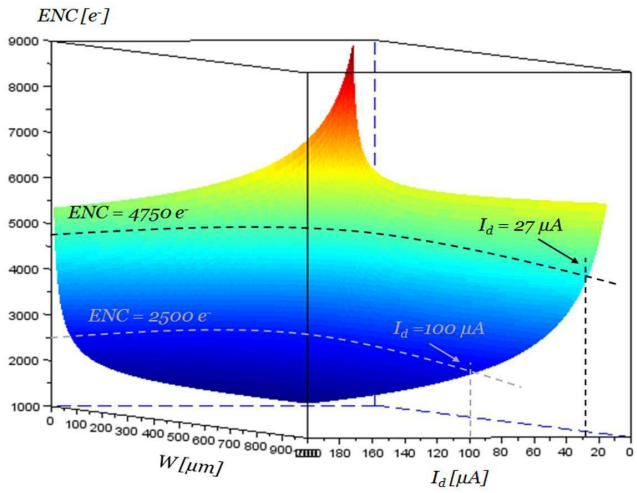

Fig. 4. 3D simulation of the CPA+PS circuit ENC_{tot} as a function of the width (W) and the drain current I_D of the CPA input transistor with a first order band-pass filter, C_{det}=40 pF, C_f=200 fF, t_s=100 ns, I_0=10 nA and L=0.7 μm.

C_{gs_1} and C_{gd_1} M_1 related capacitance and C_{ox} the gate oxide capacitance per unit area.

A two-stage OTA is used for the CPA with an NMOS input transistor (Fig. 2). The design methodology is based on the separate study of the gain of each stage depending on the requested gain-bandwidth product which is affected by the detector capacitor, the feedback capacitor and the load capacitor. In addition, the transistors are biased in the weak or moderate inversion regions as such a biasing provides relevant advantages for high-gain/low-frequency applications compared to the strong inversion region [20]. However, one of the main drawback is that the slew rate decreases slightly in these regions [21]. Considering the design of the CPA, the drain current I_D of the input transistor affects both the CPA noise and GBW. Therefore, out of these two CPA parameters, one should determine which one requires the higher current value. In Fig.4 and according to [2], the 3D simulation of the of the CPA+PS circuit in weak inversion as a function of the width (W) and the drain current I_D of the input transistor is calculated with a first order bandpass filter and t_s=100 ns. Note that in Fig.4, the capacitor C_d is equal to the sum of the detector C_{det} (included a variation of 10%) and the parasitic input capacitor of about 1.5 pF (pad and wire connections capacitors). A 27.5 μA I_D is necessary to fulfill the minimum GBW requirement. However, as shown in Fig. 4, for such a current I_D, an ENC_{tot} of 4750 e^- can only be reached. It is located in a steeply increasing ENC_{tot} zone due to the thermal noise which is inversely proportional to the input transistor transconductance gm_1. It is thus preferable to increase the current up to 100 μA to leave this zone and also to reduce the channel noise down to 2500 e^- ENC, even if it is to the detriment of power consumption. From these data, an electrical simulation with Cadence Spectre is performed to determine the required input transistor size to minimize the ENC_{tot}: W_1=556 μm.

C. The Back End

To save power as well as reduce the influence of any external parasitic signals, the analog to digital conversion of the CPA+PS output should be performed within the same chip. Thus, the following conversion channel architecture is opted: a CPA+PS, a comparator with an adjustable threshold voltage level, a peak detector (PD) and a 1 MS/s Successive Approximations Register (SAR) ADC (Fig.5). Such an SAR architecture has been chosen since it is a low power architecture that can easily achieve the required accuracy. Further, it only requires one active analog component: the comparator. To summarize, the CPA+PS converts the incident charge into a proportional voltage and the comparator detects if the incoming charge is higher or lower than the desired threshold level. Note that the minimum detection threshold level can be obtained by setting the threshold voltage of the comparator just above the noise floor. The PD is used to store the peak value of the PS output voltage, which is proportional to the electron energy. This track-and-hold voltage is then digitized by the SAR ADC. A control logic block of the system (referred as the “command block”) is also designed to manage the communications between the blocks.

As it can be observed in Fig.6, six steps are necessary to convert the output signal of the PS:

1) Track the output voltage of the PS by the PD.
2) Detect the presence of an event: at the same time and independently of the PD actions, the comparator informs the Command block (`EVENT` = ’1’) that an incoming charge has been detected. It is important to note that this signal is only sent when the comparator switches back to ‘0’, which means when the amplitude of the peak falls below (after the PS peak) to be sure that the PD has finished the track-and-hold process.
3) Hold the charge value: The Command block sends (`CMD_EN` = ’1’) to the PD blocks which is blocked in order to store the value. Then, (`CMD_READ` = ’1’) is sent to the ADC to start the conversion (`END_CONV` = ’0’).

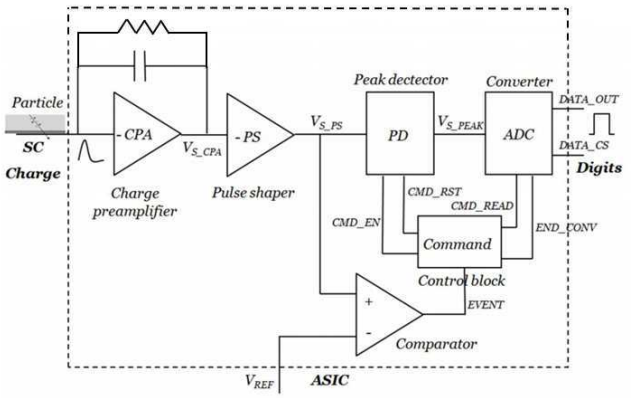

Fig. 5. AFE conversion system to measure the energy deposited by an incident electron in a Si detector.

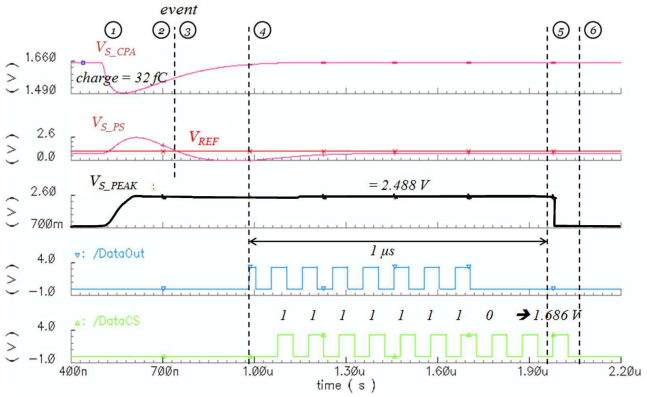

Fig. 6. From top to bottom: Transient output of the CPA, the PS, the PD and the ADC for a 50ns input charge of 32 fC and C_{det}=40 pF. The six steps necessary for the detection and the conversion can be observed.

4) Analog to digital conversion: The ADC converts the value while the others blocks of the back end are in sleep mode. When the conversion is complete, the ADC sends a signal (`END_CONV` = '1 ') at the Command block and is set in standby mode.
5) The reset: the command unit resets the PD (`CMD_RST` = '1') in order to discharge the memory capacitor. Then `CMD_READ` is set to '0', which allows the ADC to recover its baseline.
6) Finally, the command system resets itself and sets (`CMD_EN` = '0') and (`CMD_RST` = '0'). The system is then ready to perform a new conversion.

III. Results

A. Simulation

Transient simulations are performed to observe the amplitude and the settling time corresponding to the charge conversion. The CPA and PS response times for charges from 1.6 to 32 fC for a 50 ns injection duration ($T_{C_{max}}$), are respectively represented on the left and on the right of Fig.7. A rise time of 23 ns and a fall time of 464 ns are obtained for the CPA. For the PS, a rise time of 67 ns and a fall time of 881 ns (including over-shoot) are obtained. The shaping time is found to be t_s=110 ns. The conversion range (from 1.6 to 32 fC) of the AFE is linear and shows a CPA resolution of 5 mV/fC and a CPA+PS resolution of 55 mV/fC. The Si AFE circuits consume 1152 μW. The measured ENC is equal to 3277 e^-, which corresponds to a precision of 0.53 fC. These results are in agreement with the theoretical design methodology.

B. Measurements

The Si front end circuit has been implemented in a CMOS HV 0.35 μm technology. Fig.8 shows the layout view of the complete front-end: CPA+PS, peak detector and ADC. The die size is about 0.21 mm^2. To reduce crosstalk, analog and digital circuit wells are separated from each other and the corresponding circuits have their own power supplies VDD and GND.

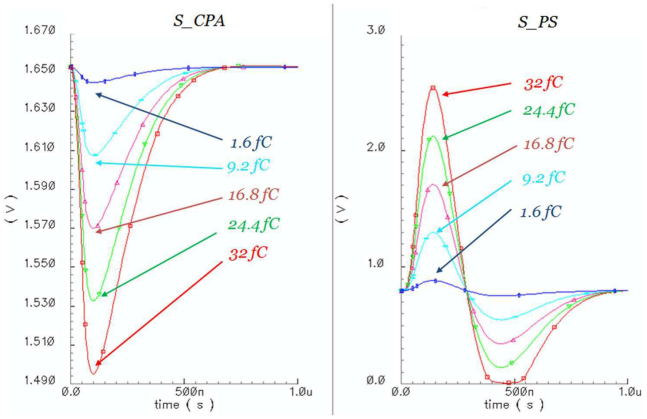

Fig. 7. Transient responses of the CPA output (left) and the CPA+PS output (right) for different injected charges ranging from 1.6 fC to 32 fC, an injection duration of 50 ns and Cdet = 40 pF.

TABLE II
PERFORMANCES COMPARISON

Year	This work 2013	[1] 2010	[22] 2011	[15] 2012
Detector type	Si	Si-W	Si	CdZnTe
Input charge range (C)	0.6 f - 32 f	0 - 2.4 p or 52 p	-	-
Technology	AMS HV CMOS 0.35 μm	AMS CMOS 0.35 μm	UMC CMOS 0.18 μm	Globalfoundries CMOS 0.35 μm
Detector capacitance (pF)	40	0-350	30	6
Shaping time (ns)	105	400	60	1000
Gain (mV/fC)	51.5	55.5	-	100
ADC	yes	yes	yes	no
Consumption (mW)	<3	2.8	1.75	7.8
ENC (e^-)	3119	2278+7.5/pF	880	70
FoM	15×10^3 3.4×10^4 (CPA+PS)	8.8×10^3 (C_{det}=40pF) 4.0×10^4 (C_{det}=350pF)	7.95×10^4	5.1×10^3

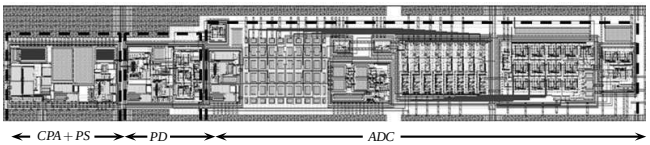

Fig. 8. Die layout of one Si CMOS front end channel implemented in a CMOS HV 0.35μm technology.

The linearity of the system can be evaluated by analyzing the ADC output. Its dynamic range is 44 dB with a linearity error of less than 0.32%. After having characterized the behavior of the ADC, the output of the Si front end ($DATA_{OUT}$ and $DATA_{CS}$) are observed for a 50 ns ($T_{C_{max}}$) input charge of 22.35 fC (see Fig.9). For a charge of 22.35 fC, the digital output is '10101001'. The detection time corresponds to the time between the arrival of the charge and the start of its conversion at the output of the ADC ($DATA_{CS}$ = '1'). This detection time is equal to 320 ns. The conversion time of the ADC is 1 μs and the reset time of the digital blocks is 200 ns. So, the effective operating frequency of the chains is approximately equal to 650 kHz.

The linearity of the Si front end is plotted in Fig.9 for 50 acquisitions for each charge step and averaged over three different ASICs. The conversion gain is 57.7 mV/fC with an ENC of 3119 e^- (or 0.5 fC) in the linear region and the saturation value is approximately 32 fC for linearity errors less than 0.81%. The minimum detectable value is approximately 0.6 fC which is higher than the expected detection threshold and is different from the measured ENC values. That can be explained by the fact that the detection thresholds are affected by the PCB ground noise.

Crosstalk measurements similar to those made in [13] have shown that crosstalk is negligible. So using an isolated-well technology (HV) and a differential pair in the CPA brings a real benefit in the integration of multiple channels on the same chip. In Table III, the specifications, the simulated and measured data are summarized. Measurements are very close to simulation results which validate our design methodology.

Certainly it is very difficult to compare the performance of a dedicated ASIC instrumentation to another because the detection and specifications are very different. For instance, the ASIC described in [1] was designed to be adapted to a wide range of detectors ($0< C_{det} <350$ pF) and to a wide range of charge detection ($0< Q_{in} <52$ pC). That adaptability was made to the

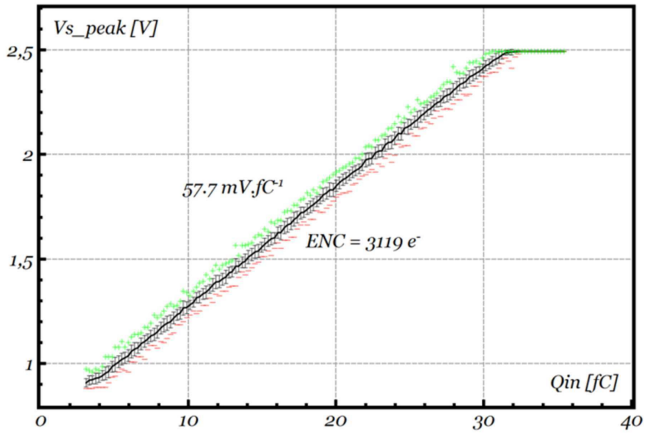

Fig. 9. Output Linearity of the Si CMOS front-end deduced from the output of the 8-bit ADC for injected charges ranging from 0.6 fC to 35 fC (50 acquisitions for each injected charge value) measured on 3 different ASICs with a 39 pF input parasitic capacitance. Averages (line), standard deviations (error bars), maximum (green +) and minimum (red -) values of 50 measures per step

TABLE III
SI CMOS FRONT-END PERFORMANCE SUMMARY

	Specification	Simulated	Measured
Input charge range (fC)	2.2 - 32	0.53 - 32	0.6 - 32
Detector capacitance (pF)	40	40	$\approx$ 40
Shaping time (ns)	100	110	$\approx$105
Gain (mV/fC)	51.5	55.5	57.7
Operating frequency (kHz)	1000	658	650
Power supply voltage (V)	3.3	3.3	3.3
Size (μm)			180$\times$1750
Consumption (mW)	$<$3	2.5	-
CPA+PS consumption (mW)		1.15	
PD consumption (mW)		1.1	
ADC consumption (mW)		0.25	
ENC (e^-)	2500	3277	3119

detriment of the speed, the gain and especially the noise (>2278 e^-). A cyclic ADC is also integrated and allows to achieve a 12 bit resolution. Conversely, the work presented in [3] was designed to be adapted to a specific application and a specific detector by minimizing the noise (198 e^-) but to the detriment of the speed and the power consumption. In the present work, noise and power consumption are optimized for each channel for an electron-hole pair generation rate closely determined by the Si detector.

In order to evaluate different detector front-end performances more quantitatively, based on eq.7, we propose to use the following Figure of Merit (FoM):

$$FoM = \frac{C_{det}}{Power \cdot ENC_{tot} \cdot \sqrt{t_s}} \tag{8}$$

As previously explained, both the shaping time t_s and C_{det} are closely related to the detector performances (Table I) and as shown in eq.7, they affect directly the ENC. They can thus hinder the performances of the CMOS front-end from being correctly assessed. Further, t_s also reflects the maximum operation frequency that can be achieved. However, the power consumption of such circuits is usually determined by the noise performances to be achieved and not by the bandwidth. Therefore, $\sqrt{t_s}$ was chosen instead of t_s. Comparison results with other recent similar works [1], [15], [22] are given in Table II.

IV. CONCLUSION

In this paper, a low noise low power CMOS front-end for particles energy measurement in space environment has been implemented in CMOS 0.35 μm HV technology. A methodology for the electronic dimensioning perfectly adapted to the detector and the targeted application has been developed. The circuit occupies a surface area of about 0.21 mm^2. The proposed circuit conversion gain is 57.7 mV/fC for an input dynamic range of 0.6 fC to 32 fC and the ENC is 3119 e^-. The power consumption is 2.5 mW at a rate of 650 kHz.

In order to extend the linear range of detection up to 4 MeV, in the future, another detector based on CdTe will be used in combination with Si detectors to fit the energetic electron detector instrument (IDEE) requirements for the TARANIS space mission [23]. Using the approach employed for the Si detectors, a CMOS front-end circuit dedicated to CdTe detectors caracterized by high parasitic capacitance and a lower electron/hole mobility than in Si, will be designed.

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