Tackling the challenges of System level ESD: from efficient ICs ESD protection to system level predictive modeling

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***Abstract*– This paper provides a review of the main tools that will allow developing a system efficient ESD design (SEED) approach. It starts with copying with the challenges of the narrowing of the ESD design window with temperature and high-voltage I/Os. We then present our behavioral modeling approach using VHDL-AMS and characterization tools such as TLP testing. Finally, the efficiency of the modeling methodology is illustrated with three case studies.**

Keywords – system level ESD, Human Metal Model, behavioral modeling, VHDL-AMS, ESD protection.

1. INTRODUCTION

Protection against ESD at system level is a main challenge for embedded electronic systems. It is particularly true in automotive applications where the electronic equipment in vehicles is continuously increasing over the years. More and more complex electronic modules have to work together without disturbing or being disturbed by electromagnetic interferences and fast transient events. To address these requirements, several electromagnetic standards such as IEC61000-4-2 [1] or ISO10605 [2] have been defined to assess the immunity of systems to both direct and indirect ESD stress during operation.

The IEC standard is designed for completed systems. However original equipment manufacturers (OEMs) are requesting integrated circuits manufacturers to also test individual components to this standard. The Human Metal Model (HMM) standard test method [3] is intended to define a test method for evaluating components using the IEC-61000-4-2 waveform [1].

It has to be underlined that the ESD robustness at system level does not depend only on the ESD robustness of the standalone components but also on the complex interactions between the various elements (passive, active, PCB traces) implemented on the printed circuit board (PCB).

In addition, automotive electronics is required to operate at higher temperatures than consumer products. This trend will be accelerated with the advent of electric vehicles and the introduction of wide band gap semiconductors such as GaN and SiC that require silicon drivers operating at high temperature (T≥200°C). It has to be reminded that system level ESD standards require tests for both unpowered and powered systems. As a result, it is important to take into account the ambient temperature for the design of ESD protections.

Given these various requirements and constraints, to perform System Efficient ESD Design (SEED) [4], it is essential to develop high-robustness ESD protections but also to be able to simulate/predict the real behavior of the system under such stress. The main challenge for OEMs to perform predictive modeling is the lack of information regarding the internal ESD strategy of the ICs. A very similar problem arose a few years ago for IC signal integrity issues and gave birth to the IBIS standard [5].

In this paper, we review the main challenges that need to be tackled to answer requirements for system-level-ESD robustness. In section 2, we first present ESD design protection approaches to cope with narrowed ESD design window in high voltage technologies as well as high temperature issues. In section 3, we present our behavioral ESD predictive modeling based on using ESD-upgraded IBIS models. In section 4, we will detail the characterization methodology we developed as an alternative to using an ESD gun. After presenting the SEED approach in section 5, we will describe in section 6 three case studies involving on the one hand two digital circuits and on the other an analog one. Finally we will give some perspectives of this work.

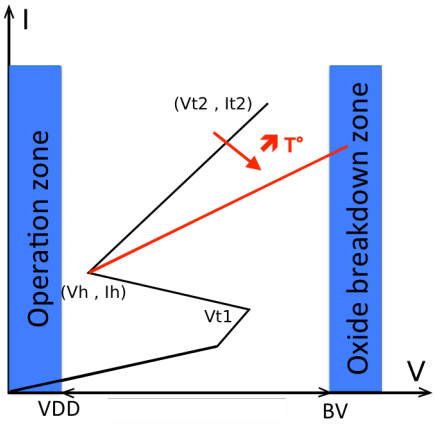


Fig. 1 ESD design window showing the detrimental effect of temperature.

2. HIGH-ROBUSTNESS ESD PROTECTION

In automotive applications, providing ESD protection for all the different I/Os from low to high voltages is a real challenge, some particular pins of the ICs being required to withstand very high HBM and IEC robustness (≥ 8kV).

The ESD design window is defined on the one hand by the operation voltage of the I/O to be protected (VDD) and on the other hand by its breakdown voltage (BV) (Fig. 1). In smart power technologies, this window is narrowed by two constraints:

- the increase of VDD whereas the oxide breakdown voltage remains the same for high voltage I/Os,
- and the detrimental effect of temperature that tends to increase the on-resistance of protection devices.

To cope with the first issue, one solution consists in using ESD protection devices with no snapback. In general, NPN transistors are preferentially used as ESD protections for their very low on-resistance (R_{ON}). However, their high gain results in a strong snapback that is a major drawback to meet high-voltage specifications.

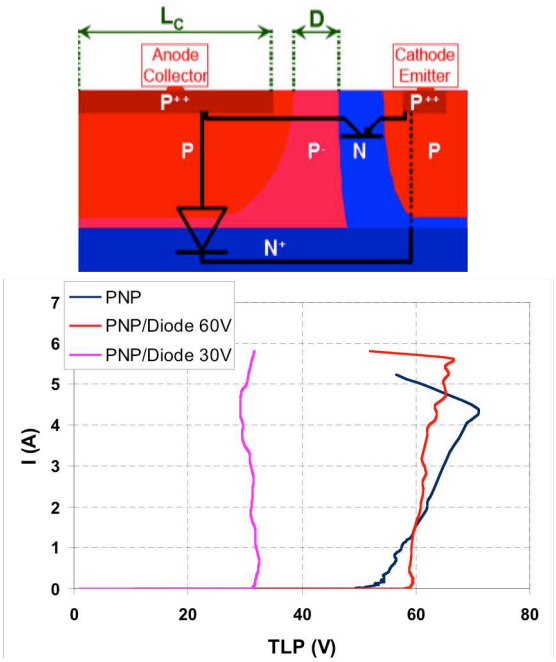


Fig. 2 View of the improved PNP ESD protection (top) and TLP characteristics of two optimized PNP-diode structures (30V and 60V clamping voltages) and of a standalone optimized PNP (bottom).

One way, to solve this problem, is to replace the NPN by a PNP. Indeed, PNP transistors exhibit a weak or no snapback. However, they have a serious handicap lying in their very much higher R_{ON} related to the low mobility of holes carriers. Using careful design guidelines (minimum emitter length, low base doping, abrupt collector doping, base contact suppression, matrix design to maximize emitter perimeter), it is possible to achieve area-efficient PNP-based ESD protections [6]. An additional improvement consists in taking advantage of the vertical parasitic PNP of the technology that operates much like a diode (Fig.2). The assisting diode can be used to set the clamping voltage of the structure.

As shown in Fig. 2, using such an implementation, a reduction of R_{ON} by a factor of seven is achieved: 0.1 $m\Omega.cm^2$ compared to the initial PNP device. Thanks to this low on-resistance, the measured HBM robustness is 8kV for a $100x100\mu m^2$ silicon area.

Regarding high temperature operation, SOI smart power technologies qualified up to 200°C or even more are now proposed [7]. A classical ESD protection solution is to use a central MOS power clamp. It has the advantage to use devices of the technology library that can be simulated by the designers but it generally requires a large silicon area. In addition, its on-resistance is very sensitive to temperature, thus degrading the ESD robustness (It_2) at high temperature that can drop from 1.74A at 25°C to 1.34A at 200°C.

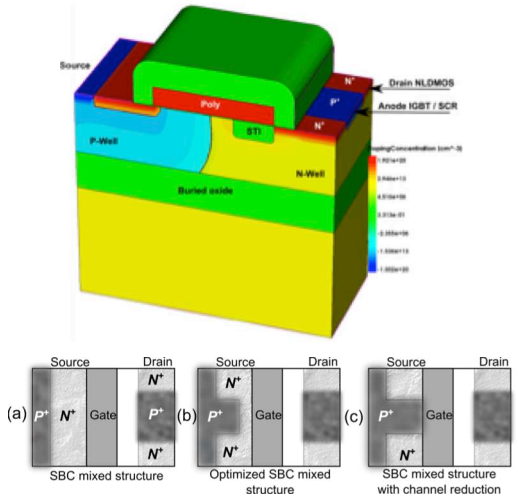


Fig. 3 IGBT-MOS-SCR structure exhibiting 50% IGBT/MOS ratio (top) and proposed source engineering solutions to increase SCR holding current (bottom).

To counterbalance this detrimental effect, an interesting solution consists in combining MOS and bipolar effects in the same structure and also taking advantage of the parasitic SCR triggering to improve the ESD robustness [8], as shown in Fig. 3.

Such IGBT-MOS-SCR structures provide a high ESD robustness (It_2> 5.5 A) with a ten times smaller silicon area compared to the initial LDMOS-based power

clamp. The best-measured IGBT-MOS-SCR structure robustness (It_2) is equal to 10 A or $1.7x10^5$ A/cm². As shown in Fig. 4 (top), this implementation confers to the protection a limited sensitivity to temperature. Given the strong snapback related to the SCR triggering, original design solutions to improve the immunity to latch-up of these structures consist in engineering the source side (Fig. 3), such as locally reducing the channel, and applying a gate voltage to increase the holding current, I_H. The best results are obtained with a reduction of 20% of the channel and a voltage bias on the gate allowing increasing I_H from 7 mA with the initial design to 40 mA with the optimized design. To even more increase I_H, several cells can be arranged in parallel to reach the required 100 mA (Fig. 4, bottom)..

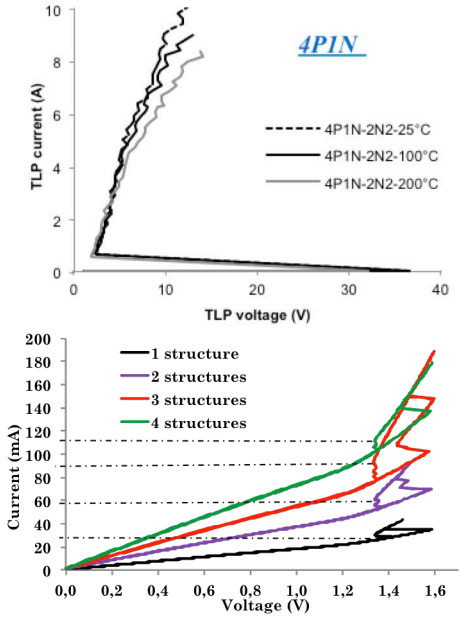


Fig. 4 TLP characteristics of an IGBT-MOS-SCR structure with 80% IGBT/MOS ratio for different temperatures (top) and holding current results for 1P1N structures (50% IGBT) in parallel (bottom).

3. SYSTEM EFFICIENT ESD DESIGN (SEED)

As previously mentioned, IEC61000-4-2 standard requires testing the system both under powered and unpowered conditions. The ESD protection scheme of an IC is generally designed for withstanding HBM stress under unpowered conditions. This is one of the main reasons why there is no possible direct correlation between the ESD IC robustness and the ESD system robustness as shown by Fig. 5 [9].

A possible misunderstanding may also have its origin in the fact that device (HBM) and system (IEC) standards look like being similar tests although they are very different. The model in both cases is made up by a capacitor and a resistor but their values are very different: device HBM: R=1500 Ω, C=100 pF; IEC 61000-4-2: R=330 Ω, C=150 pF. As a result, 8kV HBM corresponds to 5.2A current whereas 8kV IEC to 24A. This would mean that, if a pin of an IC is required to withstand 8kV IEC, the surface of the ESD protection would have to be almost five times the one required for the same HBM robustness. Increasing the size of the protections is not acceptable and the only way to fulfill such harsh requirements is to adopt co-design approaches. This is the purpose of the SEED approach proposed by the Industry Council [4].

One important point highlighted by the SEED approach is to better understand ESD events within systems. It is possible to predict the behavior of the ESD protection scheme of an unpowered IC under an HBM stress but this is much more complex when the IC is submitted to an ESD stress while operating. To validate that the implemented protection strategy will provide the targeted robustness under system level ESD stress, behavioral modeling and simulation is then essential.

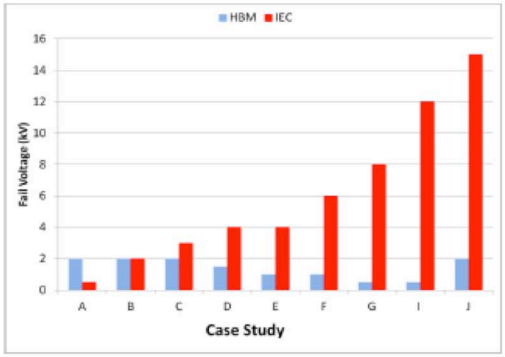


Fig. 5 Comparison of IC level and system level ESD failure threshold of various systems (A-J) showing that HBM protection is not related to System level ESD robustness [9].

4. PREDICTIVE BEHAVIORAL MODELING

For system designers, predicting the impact of ESD stress requires having access to information about the ICs including their internal ESD protection strategy. This latter information is proprietary and generally not available. The same problem occurred years ago in the field of Signal Integrity (SI) and was solved via the proposal by Intel of the IBIS standard that was first standardized in 1995 (ANSI/EIA-656) [5]. The main advantage of IBIS models is to provide exchangeable information useful for the system designer while preserving proprietary information.

Keeping the concept of IBIS description, we proposed to build IC models based on IBIS information and including ESD protections models that can be extracted without knowing the proprietary details of

the protection strategy. Such model could be used into any simulator tool.

The simulation is set with the assembly of building

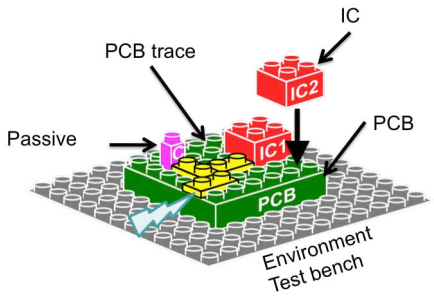


Fig. 6 ESD system level modeling methodology.

blocks following the hierarchy of the system composed of multiple elements: ICs, PCB traces, passive components and the test bench environment, as illustrated in Fig. 6 [10, 11].

As previously mentioned, IBIS files provide a lot of information that can be useful to build the IC model. IBIS files include ESD protection models, but they are not sufficient to predict faults [12]. IBIS simply describes the ESD protection scheme only with diodes between Input/Output, VDD and VSS. These diodes are static ones and their model are only valid from -VDD to 2*VDD, which is a range that is too small for ESD events simulation. Moreover, IBIS suffers from a lack of information concerning the central Power Clamp (PC) protection between VDD and VSS, which is crucial for the ESD strategy, as it drives the current from VDD to the IC ground.

For accurate ESD predictive modeling, IBIS models information need then to be upgraded with a full ESD protection strategy description of the IC. To keep the IBIS concept, no prior knowledge of IC internal structures should be needed, which is often the case for system designers at OEM level.

Measurement data are needed to extract information about on-chip ESD protections. TLP tester and curve tracer are used to extract pulsed (quasi-static) and static characteristics between each pair of IC pins. From this measurement, we proposed a behavioral description of the ESD protection scheme that has the advantage to protect proprietary information.

Diodes are good examples to present the philosophy. Only two parameters are needed: the triggering voltage, Vt_1, and the on-state resistance, R_{ON}. This defines a very simple two-state machine diagram. When the voltage across the diode is below Vt_1, the diode is off (State 0), no current flows into the protection. Otherwise we are in state 1 with the equation $V= R_{ON}.I$.

In CMOS technologies, ESD power clamp based on a big MOS transistor driven by a more or less complex triggering circuit provides a central protection between VDD and VSS. The proposed behavioral model is a two-state machine like a diode. As the actual RC-triggering delay is not known, the triggering condition is set on a dV/dt.

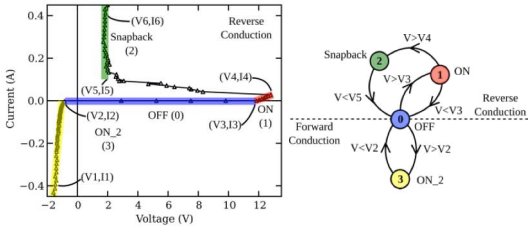


Fig. 7 Behavioral description of a SCR using a state machine.

For protection structures exhibiting a snapback behavior, four states need to be defined as shown in Fig. 7 for an SCR. Six voltage and current couples (Vx, Ix) define the inflection points of the SCR and the equivalent equations for states 0, 1, 2 and 3. To avoid convergence issues, the equivalent parasitic capacitance (often given in IBIS) is added in parallel to the SCR.

It is necessary to validate the models on the different discharge paths that involve more than one protection element. Fig. 8 illustrates a comparison between TLP measurement and simulation for a power clamp. Globally, the discrepancy is lower than 20%. The largest one observed for the path Out-to-Vss may be due to serial resistances that are not properly extracted when characterizing individual protection devices.

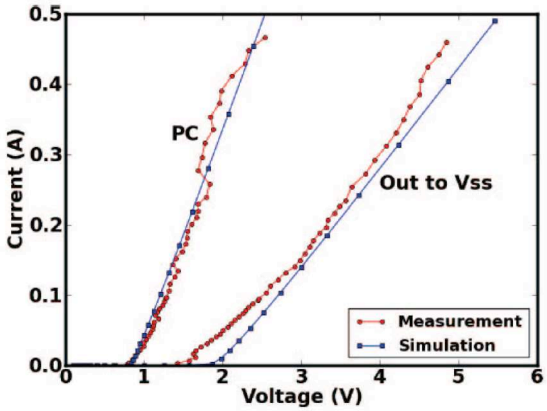


Fig. 8 TLP measurement vs simulation using VHDL-AMS model of a Power clamp for two stress modes: Vdd to Vss (left) and Out to Vss (right).

5. ESD SYSTEM LEVEL CHARACTERIZATION

The ESDA Human Metal Model standard practice provides IC manufacturers and customers with a

testing method applicable to devices that utilize the current waveform of IEC 61000-4-2. It establishes the procedure for testing, and characterizing the ESD sensitivity of component pins that will be directly connected to external connectors or ports on a completed system both under un-powered and powered states. The ESD pulse source is generally an ESD gun. However, for characterization purpose and modeling calibration, this source is too noisy and it is preferable to use a 50Ω coaxial source such as a TLP (Transmission Line Pulse) tester.

The TLP tester as previously mentioned is used to characterize the protection devices at each pin of the IC. It can also be used to inject the ESD stress on specific pins. A "one-ohm measurement" setup as defined by the EMC standard IEC61967 [13], allows measuring the current flowing into the circuit.

For susceptibility studies, the ESD TLP stress is injected into the VDD pin using the DPI (Direct Power Injection) technique [14] through a DC block composed of a 6.8nF capacitor.

Another interesting injection method is based on using a Very Fast TLP tester coupled to a near-field injection probe. The injection probe is moved above the surface of the circuit to produce cartography of the sensitive zones of the circuit [15].

Reversely, the scan probe can be used to monitor the propagation of an ESD stress within a system. The magnetic probe allows extracting the current waveforms using integral and fast Fourier Transform methods [16].

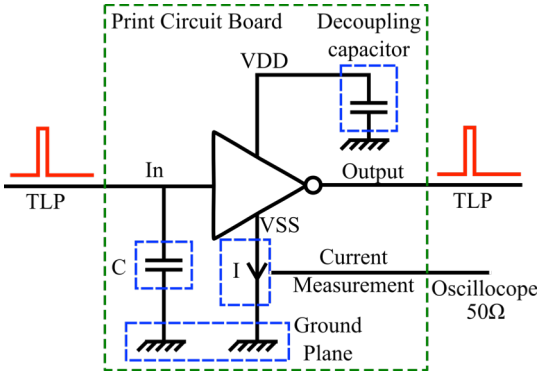


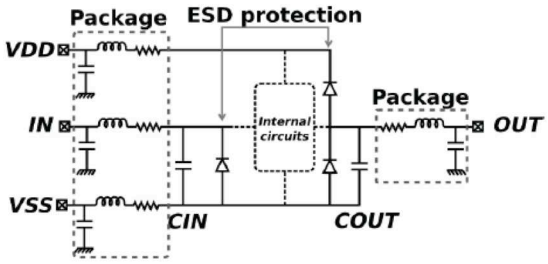
Fig. 9 Simplified schematic of the inverter circuit implemented to study the ESD stress propagation.

6. CASE STUDIES

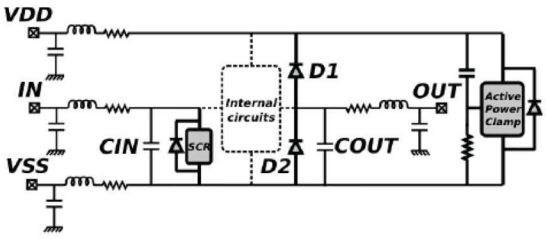
In the following, we present several examples where behavioral simulation allows getting a better understanding of the observed behavior of the system under an IEC stress. Three cases are discussed: two digital circuits - a simple one based on a CMOS inverter [10] and a more complex one based on a 16-bit microcontroller [17] - and finally the case of an analog circuit, namely an audio amplifier IC [18].

6.1 CMOS commercial inverter

The studied system is built around a simple inverter in 0.25um CMOS technology. As Fig. 9 shows, an external decoupling capacitor is placed as close as possible to the IC, between the VDD pin and the ground plane. Another capacitance is placed close to the input as an Electromagnetic Interference (EMI) filter or external ESD protection. TLP tester is used to inject a 100ns rectangular pulse with 1 ns rise and fall times. Two injection cases are investigated: into the input to ground and into the output to ground.
The equivalent model of the IC extracted from the available IBIS file is reported in Fig. 10 (a). To ESD upgrade this model for ESD simulations, we performed TLP measurement on the pins of the circuits and identified a power clamp between VDD and VSS and an ESD protection exhibiting a strong snapback (SCR) at the input. According to this measurement, we upgraded the IBIS model according to Fig. 10 (b).



(a)



(b)

Fig. 10 Equivalent IC model of the inverter circuit provided by IBIS (a) and ESD upgraded model (b).

Fig. 11 illustrates the case of the injection of an ESD stress into the input pin IN, with and without an external decoupling capacitance. Without capacitance, the TLP current flows as expected through the ESD structure. However, when added, the decoupling capacitor diverts all the current until its voltage reaches the triggering voltage of the SCR. After snapback, the ESD structure conducts the current from the decoupling capacitor to the ESD discharge current creating a strong current peak. Its amplitude is determined by the package inductance and the

parasitics of the external capacitor. The simulations show that both physical and behavioral models of the protections give the same results. This is mainly due to the fact that the parasitic elements play a more determinant role than the protections that have a very low intrinsic resistance (lower than 1Ω).

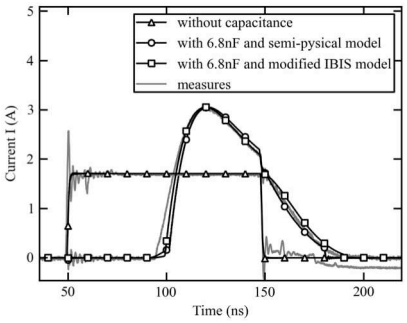


Fig. 11 Measurement vs simulation comparison of a TLP stress injection between IN and VSS of the inverter circuit with and without 6.8nF decoupling capacitor. Behavioral IBIS-based models are compared to semi-physical models.

This behavior was also validated on the output pin of the system under study using an alternative near-field measurement technique. Fig. 12 presents different cartographies acquired at different times of the ESD stress. It clearly shows that current injection is first absorbed by the decoupling capacitor and later on split between the ESD protection scheme of the circuit and the capacitor.

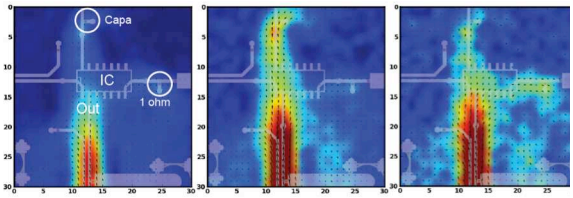


Fig. 12 Near-field measurement for a TLP stress injected between OUT and VSS of the inverter circuit showing (from left to right) how the current splits between the capacitor and the circuit.

6.2 16-bit microcontroller

The near-field probe can also be used to inject the ESD stress by scanning it above the surface of the IC. It was successfully used to study the ESD sensitivity of a commercial 16-bit microcontroller in combination with a Very Fast TLP tester [17].

In this experiment, we have flashed in the circuit a simple program to deliver a square signal period of 40 MHz, which is used as a reference to identify if the circuit runs correctly. This program uses the oscillator and PLL blocks to create the output signal. The near-field probe is moved above the chip to extract the ESD immunity cartography as shown in Fig. 13. The susceptibility criterion in measurement consists in finding, for different ESD pulse shapes, the amplitude required to stop the program or activate the clock monitor failure. Two zones are more susceptible to ESD: RESET and PLL/oscillator. The susceptibility of the RESET block is related to the exceeding of the input threshold voltage. However, more investigation was needed to understand the behavior of the PLL/oscillator block that induces clock losses (Fig. 13).

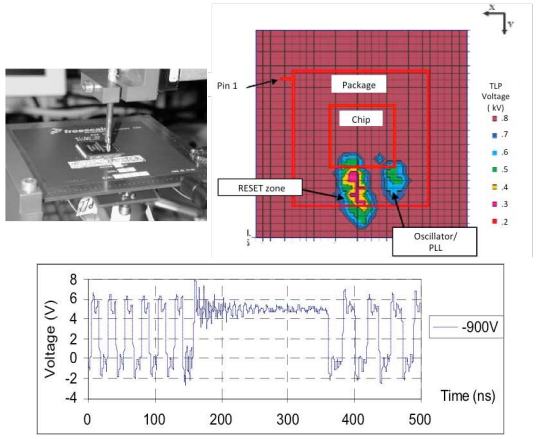


Fig. 13 ESD pulse injection system with a near-field probe (left), ESD immunity cartography (right) and resulting clock losses (bottom).

We performed simulations to validate that the microcontroller clock losses are actually induced by the ESD stress injection. For the simulation, only the following blocks are modeled: reduced model of the microcontroller including the oscillator block with its power supply, package model for the four involved pins, injection probe model and mutual coefficient coupling the loop probe with the package inductances of the pins. The simulation allowed reproducing the same faults with a good correlation with measurement.

6.3 Audio amplifier

We present hereafter a case study illustrating a strong miscorrelation between the HBM robustness and the IEC one and analyze the reasons of this behavior [18]. The circuit is an audio amplifier IC realized in a 0.25µm CMOS technology. The main blocks of the IC are represented in Fig. 14, together with the external devices (decoupling capacitor C_{DEC} and charge pump capacitor C_{OUT}) required on the testing board. The audio amplifier is composed of two symmetrical amplifiers (AOP) that provide the right and left headset sound outputs (OUTR and OUTL). The power supply VBAT can vary from 2.7V to 5.2V and an internal charge pump generates a symmetrical negative power supply –VBAT. The LDO regulators provide ±2.2V to the AOP.

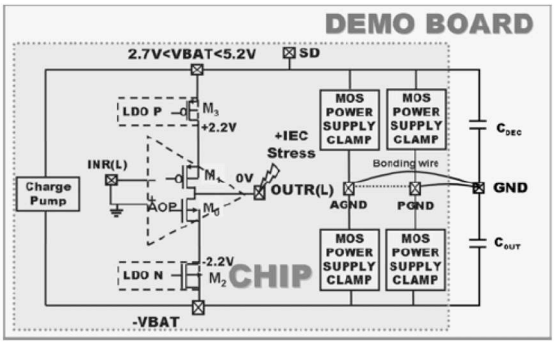


Fig. 14 Overview of the audio amplifier in IEC test conditions. C_{DEC} and C_{OUT} are external capacitors.

This IC was not originally designed to withstand IEC gun testing. A study was then carried out to assess its robustness under such stress both in powered and unpowered conditions. The gun stress is applied to the amplifier outputs (OUTR or OUTL) with its ground (GND) connected to the ground plane of the set-up. Both positive and negative stresses were applied as defined by the specifications. The results are summarized in Table 1.

TABLE I
IEC gun tests results in function of the power supply

VBAT	0V	3.8V	5.2V
IEC failure level	7kV	2kV	1kV

As shown by these results, the IEC robustness decreases from 7kV to as low as 1kV when the IC is powered. The failure analysis revealed that the device that is failing is the n-MOS output transistor M_0, the physical damage being a drain-source melt filament. Such failure signature indicates that the parasitic bipolar transistor was triggered on.

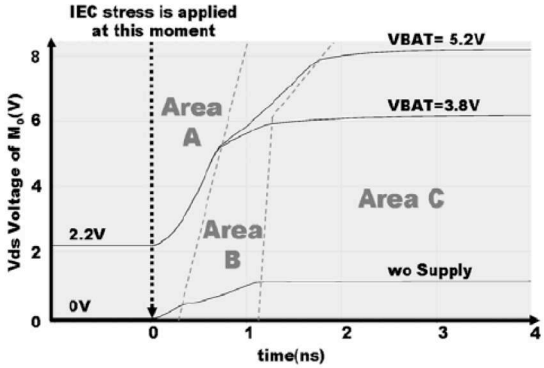


Fig. 16 Simulated drain-to-source voltage of M_0 as a function of power supply for 1kV IEC stress.

To understand why the ESD protection strategy is not efficient when the IC is powered, we performed behavioral simulations. The protection strategy is based on four MOS Power Clamp and the body diodes of the output MOS transistors M_0, M_1, M_2, and M_4.

We carried out simulations for a positive IEC stress applied to OUTR(L) when the IC is not powered and it resulted that the Power clamps are not involved at all and the discharge current is entirely absorbed by the external capacitors C_{DEC} following IEC(1) path on Fig. 15. These capacitors are large enough (1µF) to sink the ESD current without a voltage fluctuation on VBAT large enough to trigger the Power Clamp. When the IC is powered up, there is an additional discharge path, IEC(2) in Fig. 15, involving transistor M_0.

The results of the simulations are summarized in Fig. 16 that plots the drain to source voltage of transistor M_0. When the IC is unpowered, this voltage is below 1V and then no current flows in the transistor since its bipolar trigger voltage is around 10V. However, when powered up, the gate of transistor M_0 is biased thus significantly lowering the bipolar trigger voltage and favoring its activation.

This example shows that under IEC stress, the powered active circuit can interact with the ESD protection strategy and make it inefficient. Only a global protection strategy approach taking into account the final system and its operation would allow achieving system efficient ESD design.

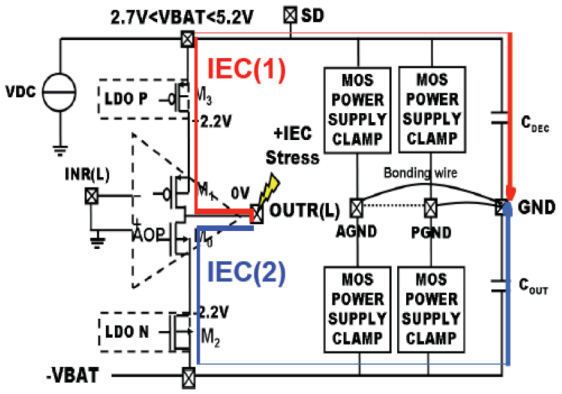


Fig. 15 Current discharge paths for a positive IEC stress applied to the output under powered conditions.

7. CONCLUSION

Designing ESD-robust integrated protections provides HBM safe ICs but does not guarantee they will survive in their application. Field returns clearly showed that there is not a straight correlation between HBM robustness and the system level one. Behavioral modeling associated to appropriate characterization tools allows better understanding the behavior of a system during ESD events such as the IEC stress. The

proposed approach is based on upgrading IBIS models with behavioral ESD relevant models and using VHDL-AMS for their description. This approach is now being discussed within ESDA standard working group WP14, System level ESD, to standardize it in the same way as IBIS.

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