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Combined MOS-IGBT-SCR structure for a compact high-robustness ESD power clamp in smart power SOI technology

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Abstract - Smart power technologies are required to withstand high ESD robustness, both under powered and unpowered conditions, in particular for automotive and aeronautics applications among many others. They are concurrently confronted to the challenges of high-temperature operation in order to reduce heat sink related costs. In this context, very compact high-robustness ESD protections with low sensitivity to temperature are required. To fulfill this need, we studied a new ESD protection structure that combines in the same component MOS, IGBT and thyristor effects. This is achieved by inserting in the same LDMOS device P⁺ diffusions in the drain. We studied the impact of N⁺/P⁺ ratios on R_{ON} and holding current at high temperatures. Structures optimization have been realized with 3D TCAD simulation and experimentally validated. The proposed structures provide a high ESD robustness with small footprint and reduced temperature sensitivity compared to classical solutions. Original design solutions to improve their immunity to latch-up are also presented.

I. INTRODUCTION

Within the context of a sustainable development and to face the challenges of fossil energy shortage, transports are becoming more electrically driven in order to optimize overall energy consumption efficiency. This requires new generations of power devices and electronic circuits. With the advent of wide band gap semiconductors such as GaN and SiC, the driving circuitry that is still realized using silicon technologies, has to be placed as close as possible to the power devices and should be able to operate at high temperature ($\geq 200^\circ\text{C}$).

To overcome isolation issues induced by high temperatures, implementing a full dielectric isolation (Silicon-On-Insulator, SOI) in silicon Smart Power technologies is becoming more and more interesting. It allows managing very high blocking voltages, reducing parasitic bipolar effects and increasing circuits speed.

In addition to high temperature constraint, ESD requirements from the integrated circuit to the system are particularly severe: for example, in automotive applications, 2-8kV in contact according to the IEC 61000-4-2 standard [1] is often required. It has to be reminded that this ESD standard requires tests both for unpowered and powered systems. For the latter testing, the effect of temperature has then to be taken into account in the ESD design window. Protection should provide

a high failure current but also work at high temperature, its performance being as insensitive as possible to this parameter.

In this paper, we propose a study of an ESD protection solution based on combining MOS and IGBT structures in the same device and allowing SCR triggering to reach a high ESD robustness and a low sensitivity to temperature.

In section II the proposed device and its technology are described. A first analysis based on simulation is carried out in section III. Finally, in section IV, the experimental results are thoroughly analyzed including triggering overshoot and latch up risk.

II. SMART POWER SOI TECHNOLOGY AND PROPOSED ESD PROTECTION

The chosen technology is a smart power SOI (TFSMART 1) provided by Telefunken Semiconductors [2]. It is a 0.8 μm Bipolar CMOS DMOS merged technology on SOI. The buried oxide and active silicon thicknesses are 500 nm and 2 μm , respectively. The process offers 0.8 μm five-volts CMOS devices, lateral npn-and pnp-transistors, P-type and N-type lateral DMOS devices with complete deep trench isolation between wells and vertical oxide isolation to handle wafer/substrate for different supply voltages

Regarding the N-LDMOS devices, TFSMART 1 library contains two types of structures. The first one is named Source Body Short (SBC), since the source N⁺ diffusion is shorted to the P-type body diffusion. This short is implemented by inserting within the source N⁺ diffusion a P⁺ body contact. The second one, called Source Body Open (SBO), has a Shallow Trench Isolation (STI) between the source and the P⁺ body contact (Fig. 1). This latter structure allows biasing the body at a different voltage from the source.

The TFSMART 1 library proposes a high-voltage active MOS-based ESD-power-clamp. This is actually a 25V N-LDMOS with increased gate-drain ballasting distance. It is composed of 11 identical cells that are formed of two 150 μm -fingers with a central drain diffusion, the body being connected to the source. The corresponding surface is 302 μm x 183 μm and it provides a 2 kV HBM robustness according to TFSMART1 foundry data [2] that correlates with our measurement. We observed a robustness equal to 1.74 A at

25°C and 1.34 A at 200°C for 100 ns current pulses. This is a dramatic robustness reduction of 25% with temperature. The performance of this MOS-based protection structure, namely its on-resistance, is very sensitive to the temperature [3]. According to our measurements, the on-resistance increases from 4.4 Ω at 25°C to 7.14 Ω at 200°C. If this temperature behavior is not taken into account during a circuit’s ESD-protection-design, it could induce detrimental effects such as a lower failure current and even could fail providing the expected protection due to the lack of compliance with the ESD design window. To compensate this effect, the size of the power clamp protection would have to be increased.

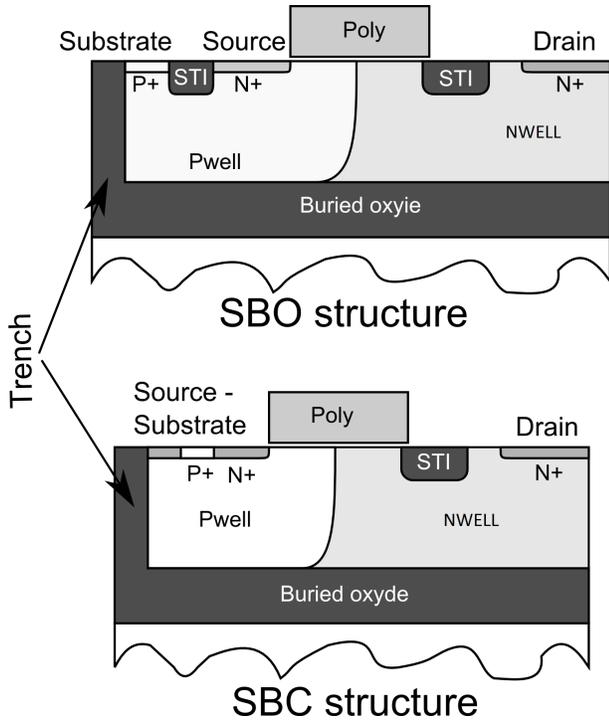


Fig. 1: SBC and SBO types structures.

To cope with these issues, we contemplated developing a new ESD protection. The basic concept presented in this paper consists in combining MOS and bipolar effects in the same structure in order to compensate the detrimental effects of the temperature. To improve the ESD robustness, we also take advantage of the turn-on of the parasitic thyristor of the structure that will provide a very low on-resistance.

We implemented within the structure of the N-LDMOS a lateral IGBT by inserting in the drain region both N⁺ and P⁺ diffusions (Fig. 2).

The equivalent electrical schematic is presented in Fig. 3. The protection is triggered via its gate to allow protecting low voltage circuitry and a nearly triggering of the structure (MOS then IGBT) to compensate the intrinsic SCR slow response.

Such MOS-thyristor combination was already proposed in our laboratory (LAAS) in 1985 by H. Tranduc to improve the performance of power device structures [4]. More recently a pure LIGBT was proposed to implement an efficient ESD power clamp in an SOI smart power technology [5]. The authors demonstrated the improved performance compared to

an NDRIFTMOS device. However, combining the three devices’ action (MOS, IGBT, SCR) in a single device was not yet studied to the best of our knowledge.

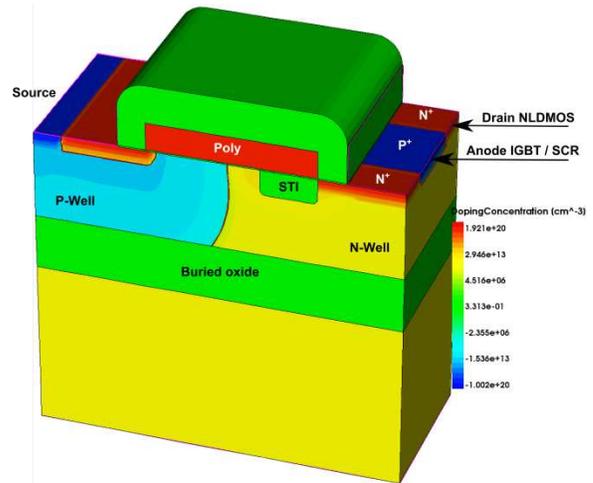


Fig. 2 :Structure of the “elementary cell” of the proposed LDMOS-LIGBT. Here 50%-IGBT, i.e. the P⁺/N⁺ ratio at the drain side is equal to 1.

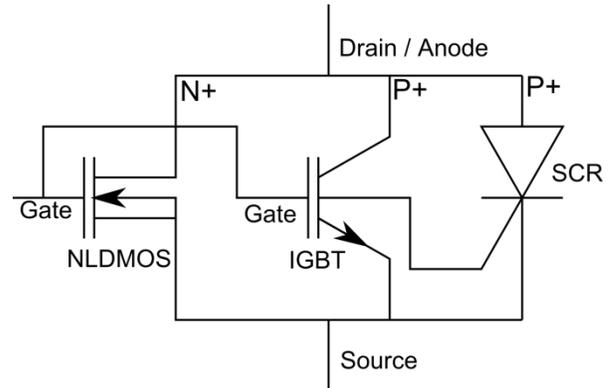


Fig. 3: Equivalent electrical schematic of the mixed structure LDMOS-LIGBT.

Two silicon runs (RUN01 and RUN02) have been made in order to optimize the behavior of these new devices.

We use a naming convention where the N-LDMOS is considered as the reference structure and the IGBT percentage represents the proportion of P⁺ diffusion among the full device drain width. For example, a 20%-IGBT device has 20% of P⁺ and 80% of N⁺ in its drain. Thus, 0%-IGBT is the reference N-LDMOS (no IGBT action) and 100% -IGBT is the full LIGBT (no NMOS action). An illustration of a 50%-IGBT is shown in Fig. 2 where the N⁺/P⁺ diffusions ratio is thus equal to 1.

In a previous work presented in [6], we designed a test chip with various structures going from a N-LDMOS to a LIGBT and mixed structures with an increased IGBT percentage of 33, 50 and 66%. The proposed structures provide a high ESD robustness (> 5.5 A) with a ten times smaller silicon area compared to the LDMOS-based ESD power clamp from the library. Another beneficial effect of this design is that the performance of the ESD protection becomes much less sensitive to temperature.

The main problem we encountered in this initial study was the small value of the SCR holding current. In the next section, we

propose solutions to overcome this issue, firstly optimized using 3D TCAD simulations and then experimentally validated on silicon.

III. INVESTIGATION ON HOLDING CURRENT OPTIMIZATION BASED SOURCE SIDE TCAD ANALYSIS

The holding current of the parasitic SCR is defined by the following parameters and equation [7]:

$$I_H = \frac{\beta_p(\beta_n+1).I_{NW}+\beta_n(\beta_p+1).I_{PW}}{\beta_n\beta_p-1} \quad (1)$$

Where β_n and β_p are the current gains of the parasitic NPN and PNP bipolar transistors and I_{NW} and I_{PW} the currents flowing into the N-well and P-well, respectively.

To increase I_H , as we can hardly modify the current gain of the two bipolar transistors, the classical way is to reduce as much as possible the resistances of the two wells [8]. In the proposed structure, this means on the one hand optimizing the N^+/P^+ ratio in the drain and, on the second hand, introducing P^+ diffusions into the N^+ source diffusion to reduce the P-well resistance;

To find out the best trade-off between high I_H and low on-resistance, we performed 3D simulations. They show that varying the N^+/P^+ ratio in both source and drain regions allows controlling and increasing I_H whereas preserving the ESD performance. However measurements showed that I_H is almost independent of the N^+/P^+ ratio at the drain side, which means that the SCR behavior is mainly controlled by the parasitic NPN bipolar transistor (N^+ source, P-well, N-well). Therefore, the most efficient way to increase I_H consists in engineering the source side of the device that defines this parasitic bipolar transistor.

All the structures used in the first test run were of SBO type (Fig.1) with external short circuit between source and body contact since the original LDMOS was implemented that way.

A first solution to optimize the I_H value is to use an SBC-type structure that allows significantly reducing the P-Well resistance (base of the NPN bipolar transistor). Using Sentaurus TCAD, we simulated a 3D structure to check the impact on the holding current. The structure under study is based on an NLD MOS 25 V. We could not have access to accurate doping profiles for this technology. To perform the 3D simulation on the NLD MOS 25V, we performed an extrapolation from another SOI technology and did some fitting according to TLP measurement. As a consequence, the simulation results can only be considered as qualitative to compare the relative efficiency of different design solutions.

To perform the three-dimensional (3D) simulations, which are known to be time consuming, we used a quasi-stationary simulation and an elementary 3D cell of $3\mu\text{m}$ -width to minimize computation time. In addition, since the simulations are carried out in the low current regime, around the holding current point, self-heating does not have a very large impact on the device behaviour; as a consequence the heat equations were not included in the simulations.

The computed I_H should be scaled according to the real structure width from the results obtained with the $3\mu\text{m}$ -width elementary cell. According to equation (1) I_H is inversely proportional to the well resistances via I_{PW} and I_{NW} currents, and a scaling coefficient can be computed. According to the way we compute it, its value can be in the range of 6 to 10.

Fig. 4 shows that I_H increases from 5 mA for a SBO structure to 8 mA for a SBC one for simulated $3\mu\text{m}$ -wide 50%-IGBT devices at room temperature and $V_{GS}=3\text{V}$.

As the increase of I_H from 5 to 8 mA is not sufficient, another interesting solution consists in locally inserting a P^+ diffusion into the source either as close as possible to the gate (Optimized mixed structure SBC Fig. 5 middle), or even totally replacing the N^+ source diffusion (Fig.5 right). In that latter case, the MOS channel will not be able to form then resulting in a structure with a reduced channel and the local elimination of the parasitic NPN bipolar transistor. We named this latter structure ‘‘SBC structure with channel reduction’’.

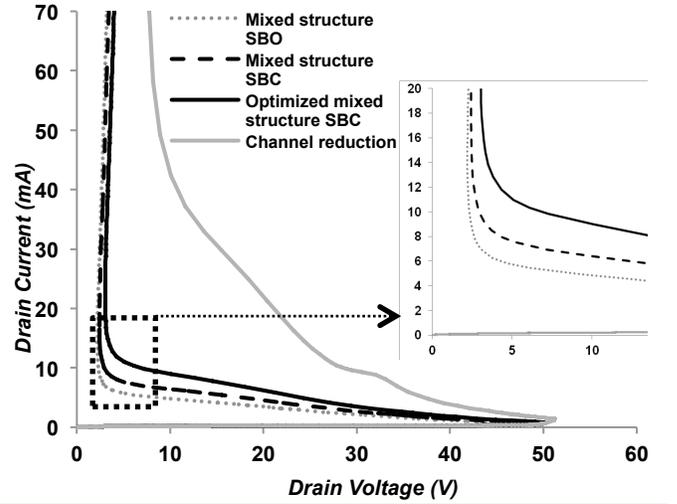


Fig. 4: TLP characteristics difference between SBO mixed structure, SBC mixed structure, optimized mixed structure that illustrated in Fig. 5 and mixed structure with reduced channel by 30% at room temperature and at $V_{GS} = 0\text{V}$. The inset in the right shows the zoom of the three first curves.

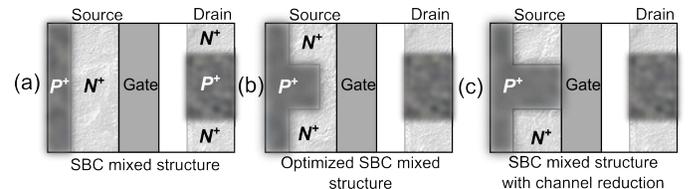


Fig. 5: Source side optimization of an 50%-IGBT: SBC mixed structure (a), Optimized SBC mixed structure (b) and SBC mixed structure with reduced channel (c).

The result of the simulation for the optimized mixed structure (Fig. 5 middle) shows that I_H increases from 8 mA for a SBC structure to 12 mA. For the reduced channel structure I_H raises up to 40 mA. However, in this latter case, the holding voltage increases to 7.5 V to be compared to 4 V for the three first ones. With such holding voltage increase there is a risk to lower the ESD robustness of the structure. Finally, taking into account the simulation-scaling coefficient, the resulting I_H

should be in the range of 100 mA therefore meeting the latch up specification. The experimental result will be detailed and discussed in section VI-b.

IV. OPTIMIZED STRUCTURES ELECTRICAL CHARACTERIZATION RESULTS

Starting from the simulation results we have designed a number of optimized mixed structures. We designed structures with a N^+/P^+ ratio in the drain varying between 0 and 4 (0, 1/4, 1/3, 1/2, 1, 2, 3 and 4) which corresponds respectively to 100, 80, 75, 66.6, 50, 33.3, 25 and 20%-IGBT device according to the naming convention defined in section II.

For each N^+/P^+ ratio, the IGBT P^+ diffusion can be implemented as a single segment or partitioned into several ones. For example, we designed two configurations for the 80%-IGBT structure, and four configurations for the 75%-IGBT. However, this does not lead to significant changes of the devices behavior and thus will not be detailed here.

For the design of the mixed structures, we started from 25V ESD NLD MOS of SBO type from TFSMART1 library. To reduce the PWell resistance, we also designed different configurations for the source side of the device. We introduced P^+ islands of $3.2 \mu\text{m}$ abutting the N^+ source and locally replacing the STI.

Both drain side and source side configuration will be detailed later on in the next sections.

To characterize the optimized structures of the second test chip called RUN02, we used the same techniques as for the first test chip (RUN01): an analogic curve tracer to extract holding current and a 100 ns pulse generator (TLP bench) to characterize the ESD structures robustness, trigger voltage and serial resistance, both at low and high temperatures.

a. Robustness results and temperature effects

Measurements are done until failure defined when the leakage current becomes significant ($>1 \mu\text{A}$) at room temperature. For a given N^+/P^+ ratio, we did not notice any significant impact of drain or source configuration on the robustness (Table 1).

Failure current (A)	Drain config. 1	Drain config. 2	Drain config. 3	Drain config. 4
Source Config 1	9.33	9.73	9.54	9.93
Source Config 2	9.52	9.73	9.14	9.38
Source Config 3	N.A.	N.A.	9.33	N.A.

Table 1: Failure current for the different source and drain configurations of the structure 3P1N (75% IGBT). The third source configuration is implemented with only one drain configuration.

We noted that the robustness of the structures increases with the percentage of P^+ in the drain with one exception, which is the LIGBT. Indeed the presence of P^+ in the drain allows the triggering of the parasitic thyristor associated with the IGBT, and then a current distribution within the volume of silicon. Thus in a mixed structure, most of the current flows through

the thyristor region of the component (lower resistance), so if this region is larger, the structure can hold more power and the opposite is true. Between the 80%-IGBT structure and the LIGBT one, the robustness decreases from 10 A to 7.5 A. A linear extrapolation of the robustness with the percentage of P^+ into the drain would result in 13 A for the LIGBT robustness.

Fig. 6(a) presents the variation of the normalized failure current and resistance as a function of P^+ drain percentage. In this Figure, we see that although its on-state resistance is smaller than all mixed structures, the robustness of the LIGBT is lower. From Fig. 6(b), we can see that the LIGBT power failure is almost equal to that of the 25%-IGBT structure. Note that the power to failure is calculated by multiplying the failure current by the failure voltage.

This exception case (LIGBT) will be analyzed in detail in the next sub-section.

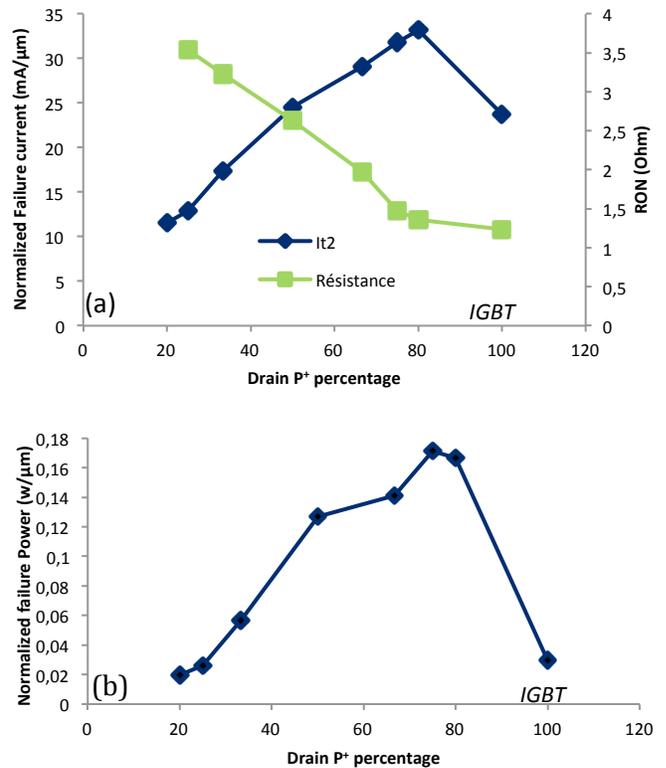


Fig. 6: Failure current and on-resistance variation as a function of percentage of P^+ diffusion in the drain (a) and, failure power variation as a function of the percentage of P^+ in the drain (b) at room temperature and grounded gate

Moreover, measurements up to failure show that the robustness does not change by changing the gate bias. It is the same for the on-state resistance. Indeed, increasing the voltage V_{GS} , only changes the low-current part of the curve (linear and saturated) but right after the triggering of the thyristor, the gate bias has no more impact.

Fig. 7 shows the TLP characteristics as a function of temperature for grounded gate 20%-IGBT (1P4N), 80%-IGBT (4P1N) and LIGBT structures. The results show a decreased robustness when increasing the temperature for all components. This decrease is accompanied by an increase of the on-resistance which in turn results in increased self-

heating and then to early failure.

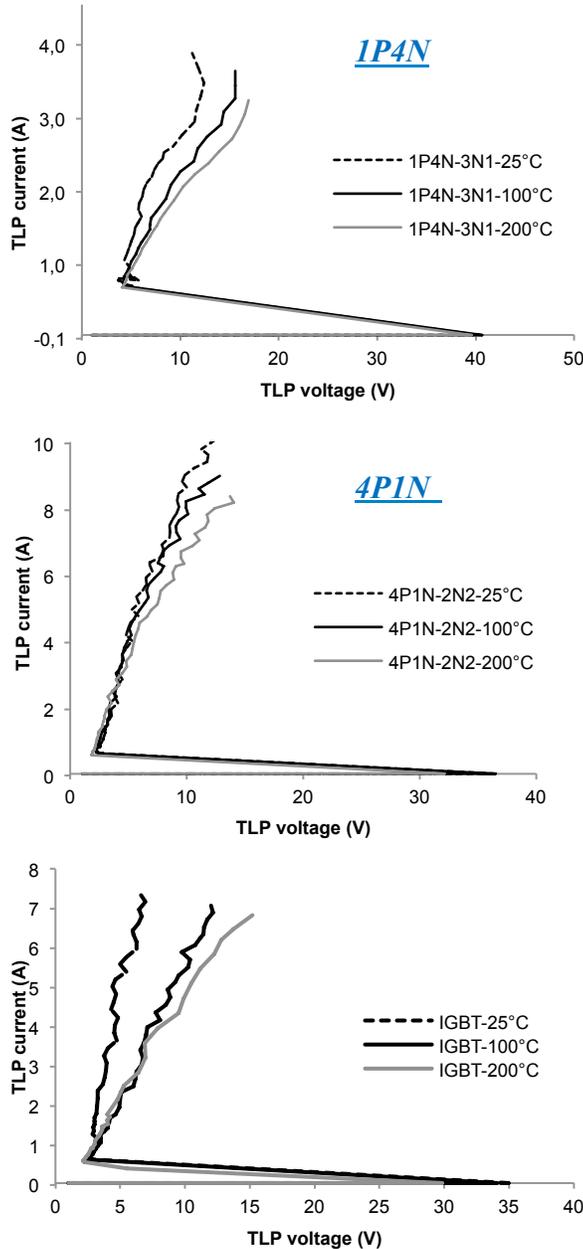


Fig. 7: TLP characteristics of 1P4N structure (20% IGBT) (up) and 4P1N structure (80% IGBT) (center) and IGBT (bottom) with grounded gate and as a function of temperature. We can remark the three part of structures name in the legend: the first is the drain configuration, the second is the segments number of the mentioned diffusion in the drain and the third number in the second part is the source configuration.

b. Investigation on the LIGBT unexpected behavior

Fig. 8 shows a photoemission view of the first configuration of 1P2N (33% IGBT) structure where the IGBT is divided into three segments. This Figure shows a photo-emission captured at a current level of 4 A. It clearly shows that the power is distributed over the different regions of the IGBT structure (3 light-emitting areas) that correspond to the three P^+ zones of this structure. At this current level, we observe a small current crowding phenomenon. It may be noted also that in this structure, which has two fingers, a larger current flows in the

upper finger (light emitting more intense) than in the lower one. The upper finger is the first to be triggered due to a lower source access resistance. This difference between upper and lower fingers make the robustness smaller than can be.

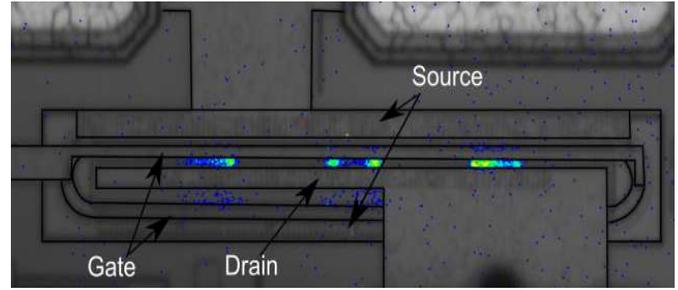


Fig. 8: Photoemission of the 1P2N structure with 4 A of current and at room temperature.

A first explanation for this low experimental I_{T2} value of the LIGBT could be the occurrence of a current focalization in the structure that does not occur in the case of mixed structures. However, an observation in photoemission of the LIGBT at 6A shows that the current is homogeneous, even at the periphery of the drain.

We analyzed the TLP voltage and current waveforms across the LIGBT and mixed structure. It shows that in the LIGBT, the SCR needs more time to propagate throughout the structure and have therefore the lowest snapback voltage. Indeed, Fig. 9 presents the TLP characteristic of a LIGBT for $V_{GS} = 5V$ on the left figure and current waveforms (bottom right) and voltage (upper right) with a value of $I_{TLP} = 5A$. Fig. 10 shows the same curves, for the 80%-IGBT structure with one P^+ segment in the drain. In the first case, the snapback voltage firstly reaches 75 V at $t = 25$ ns, and then continues to decrease linearly until $t = 50$ ns. In the second case, the snapback voltage is steep. So we can conclude that this delay in the LIGBT generates a phenomenon of self-heating that is more important than in a mixed structure.

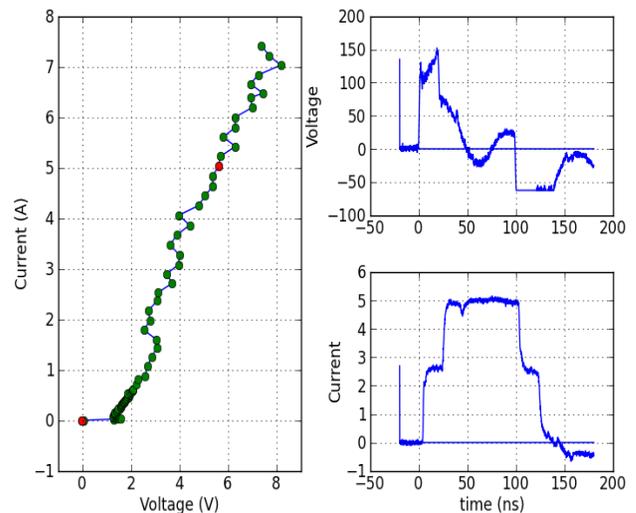


Fig. 9: TLP Characteristics of the LIGBT structure (left) and voltage and current waveforms (right) for $I_{TLP} = 5A$ and $V_{GS} = 5V$

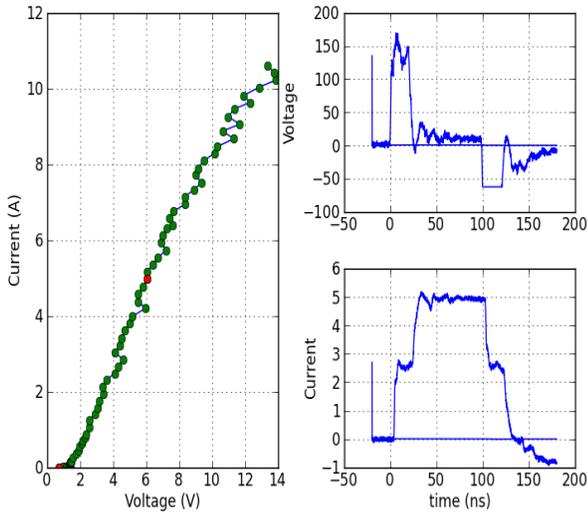


Fig. 10: TLP characteristics of the 4P1N structure (left) and voltage and current waveforms (right) for $I_{TLP} = 5A$ and $V_{GS} = 5V$

c. Triggering overshoot

The results in the previous section showed a high voltage across the DUT. To evaluate the actual overvoltage seen by the DUT before the triggering of the protection structure, we carried out transient TLP measurement using a Very Fast TLP system with a pulse duration of 2.5 ns and a rise time equal to 100 ps.

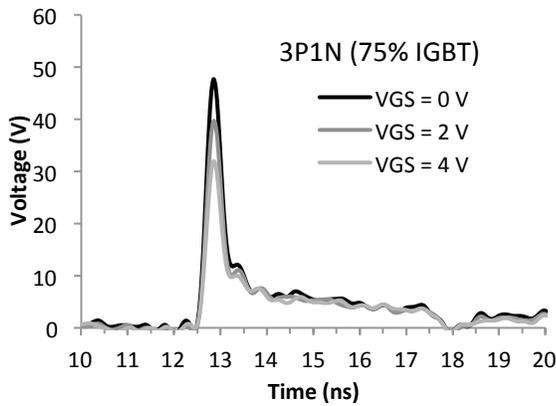


Fig. 11: Waveform of the voltage across the structure 3P1N (75% IGBT) for many gate polarizations at constant temperature and initial signal amplitude 100V.

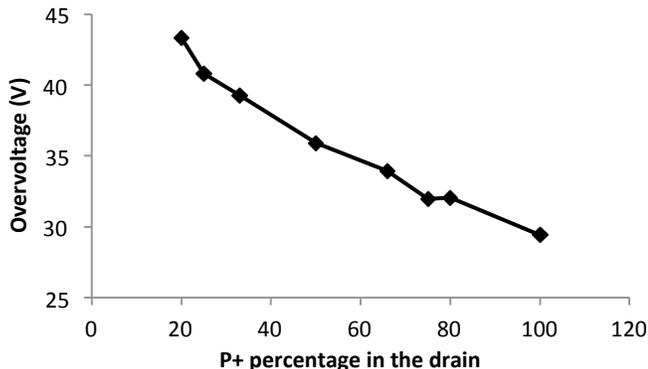


Fig. 12: Over-voltage variation with P+ percentage in the mixed structures result to transient TLP characterization

A dedicated TLP measurement and data processing methodology, developed by A. Delmas et al. [8], allows accurate extraction of the voltage and current waveforms across and through the DUT.

The results show the decrease of the overvoltage with increasing gate bias (Fig. 11). This decrease becomes more significant with a higher percentage of IGBT structure.

The high value of the overvoltage can be a cause of failure of the component or circuit to be protected if greater than the failure voltage of the component. Several methods can be considered to solve this problem and provide a perspective of this work [10].

The variation of overvoltage with P⁺(IGBT) percentage in the drain is presented in Fig. 12 at $V_{GS} = 4V$ and at room temperature. We can remark that the overvoltage decreases with the increase of P⁺ percentage. This overvoltage decrease maybe related to the reduction of the on-resistance of the structure with the P⁺ percentage.

d. SCR holding current and latchup risk

To improve latch up immunity, we focused our efforts on the source engineering by implementing P⁺ islands to reduce the Pwell body resistance (Fig. 13). These islands are implemented using two configurations. In the first one (config 1), their width constitutes 1/8 of the total width of the structures and in the second (Config 2) 1/4. A third configuration consists in removing the STI between the P⁺ body contact and the N⁺ source diffusion that corresponds to a Source Body Shorted (SBC) type structure.

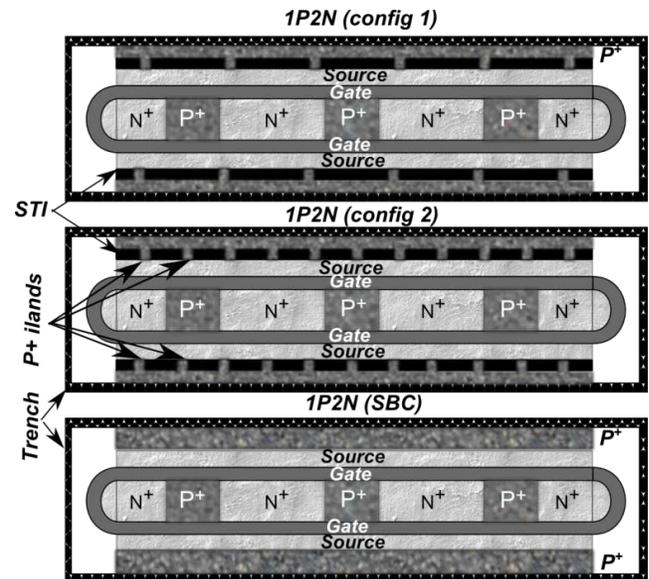


Fig. 13: Various source configurations for a structure with ballast drain resistance.

Table 2 shows the variation of holding current for three different source configurations for a voltage V_{GS} of 3 V. The differences in I_H values between Config 1, Config 2 and SBC are not significant enough to draw a conclusion about the impact of the source configurations.

Then we analyzed the impact of the drain configuration, i.e., the P^+ percentage variation in the drain (Fig. 14). In this figure, there are several points for a single percentage of P^+ , these points correspond to different segmentations of the P^+ for the same percentage of this latter in the drain. Although there is a slight increase of I_H for structures having a P^+ percentage higher than the one in the 2P1N one (66% IGBT), the higher holding current is obtained with the lowest percentage of P^+ in the drain.

Drain configuration	Source configuration		
	Config 1	Config 2	SBC
	Holding current (mA)		
1P4N (20% IGBT)	28	27,5	27,5
1P3N (25% IGBT)	29	28,5	28
1P2N (33% IGBT)	27,5	27	26,5
1P1N (50% IGBT)	24	24	22
2P1N (66% IGBT)	22	23	22
3P1N (75% IGBT)	22,5	23,5	21,5
4P1N (80% IGBT)	23	23	22
LIGBT	26	26	24

Table 2: Holding current variation for the different configurations (source side) of the ESD components with a drain ballast resistor at $V_{GS} = 3$ V

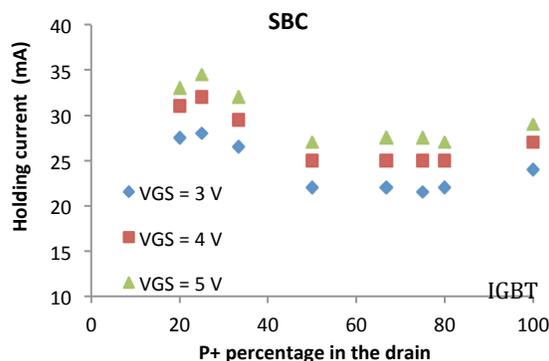
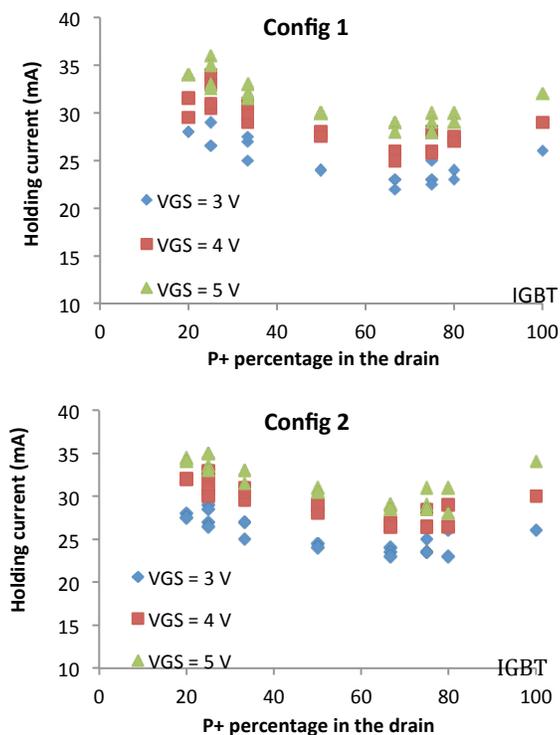


Fig. 14: Holding current variation with P^+ percentage in the drain at room temperature, for several values of V_{GS} and for the three configurations of source.

The holding current exhibits a minimum value for 2P1N (67% IGBT). This can be explained by the fact that the P^+ percentage in the drain has two opposite effects. Increasing the P^+ diffusion ratio into the drain increases the quantity of holes injected in the low-doped region thus decreasing in the Nwell resistance by conductivity modulation. As a consequence a higher current is required in the NWell for the PNP bipolar transistor to turn-on. Concurrently, the increase of P^+ in the drain results in a greater hole current in the Pwell (source side), favoring an easier NPN bipolar transistor turn-on and then the thyristor triggering. According to the realized measurements (Fig. 14), 2P1N structure configuration corresponds to the threshold where there is no predominance of either of these effects (Nwell-resistance modulation or NPN base current increase).

e. Impact of channel reduction

For the study of the structure with reduced channel, we used non-ballasted structures that were originally designed as improved power devices. As a result, the ESD robustness is almost halved by the absence of the ballast resistor: for example, for the 4P1N structure it decreases from 10 A with the ballast resistor down to 6.5A without it.

Fig. 15 shows these specific configurations (source side) for 1P2N structure without ballast drain resistance to study the effect of that area in this technology. They are respectively from top to bottom: 1P2N-20PC, 33%-IGBT structure with 20% channel reduction, 1P2N-10PC, 33%-IGBT structure with 10% reduction channel reduction and 1P1N-1P1N, 50%-IGBT structure with SBC source configuration.

To implement this channel reduction, we replaced 10% (20%) of the N^+ diffusion of the source by P^+ diffusion.

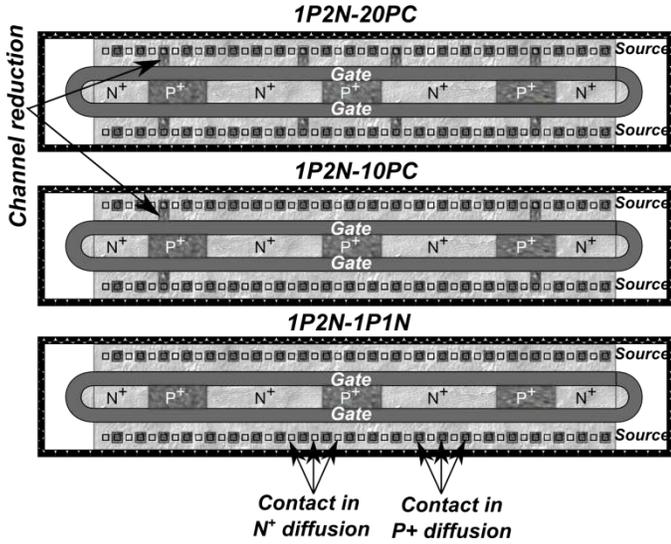


Fig. 15: Diagram of the different configurations (source side) of the 1P2N structure without ballast resistor

To study the channel reduction effect on the holding current value, we made three different measurements for each structure using the curve tracer to get more accurate values.

We studied the effect of the channel reduction on the robustness and the on-resistance of the structures. The TLP measurement showed that there is no change in resistance or robustness.

Indeed, the simulation showed that the holding voltage for reduced channel structures is much larger than the others. Therefore, if we assume that the maximum power failure is constant for these structures, their robustness should be reduced by a percentage proportional to the increase of the holding voltage.

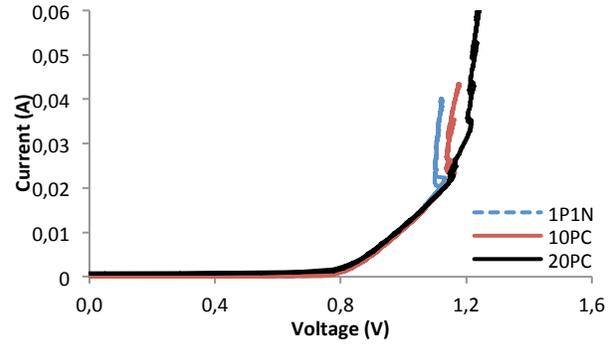
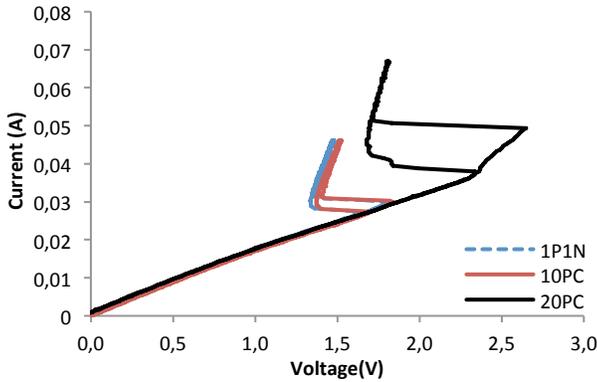


Fig. 16: I-V characteristics for the 1P2N structure (up) and IGBT (bottom) at room temperature, with $V_{GS} = 5V$ and for several source configuration.

Fig. 16 shows the I-V characteristics for 1P2N (percentage of P^+ into the drain = 33.3%) and for LIGBT measured at room temperature and with a voltage V_{GS} of 5 V. It can be noted from this figure that the difference between a normal structure and a structure with a 10% channel reduction is hardly noticeable. However, the 20% channel reduction has a significant effect. This was observed for all the structures. In Fig. 16, for the configuration 20PC, and after thyristor triggering, it can be noticed that the characteristic of the LIGBT snaps back several times. This behavior may be due to the different phases of current distribution in the structure. Each snap back shows that there is a new current filament that opens. In addition to the increase in holding current, reducing the channel also allows increasing the holding voltage.

V. CONCLUSION

We proposed a new mixed ESD component MOS-IGBT improved to operate at high temperature and have a high robustness. The basic concept is to trigger the structure as an IGBT but to also allow its parasitic SCR triggering. To do so, we combined within a same N-LDMOS a lateral IGBT by implementing P^+ diffusions in the N^+ drain region with different N^+/P^+ ratios. The proposed structures provide a high ESD robustness ($> 5.5 A$) with a ten times smaller silicon area compared to the initial LDMOS-based power clamp. The best measured robustness is equal to 10 A or $1,7 \times 10^5 A/cm^2$. Another beneficial effect of this design is that the performance of the ESD protection becomes much less sensitive to temperature. We proposed original design solutions to improve the immunity to latch-up of these structures by engineering the source side, on the one hand, and providing an additional control via the gate, on the other hand. These solutions were validated through comparative 3D simulations and on a silicon test vehicle. The most efficient solution to control the SCR holding current is the channel reduction with IGBT percentage equal to 33%. The highest measured robustness is equal to 10 A or $1.7 \times 10^5 A/cm^2$ with IGBT percentage equal to 80%. The proposed optimized elementary cell can already be used either in series or in parallel to provide the required latch-up immunity.

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