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On-chip measurement to analyze failure mechanisms of ICs under System Level ESD stress

F. Caignet[1,2], N. Nolhier[1,2], M. Bafleur[1,3], A. Wang[1,3], N. Mauran[1,3]

[1]*CNRS, LAAS, 7 avenue du colonel Roche, F-31400 Toulouse, France*

[2]*Univ de Toulouse, UPS, LAAS, F-31400 Toulouse, France*

[3]*Univ de Toulouse, LAAS, F-31400 Toulouse, France*

Abstract - Electro Static Discharge (ESD) is one of the major causes of electronic system failures. Reliability of ICs within the applications is strongly related to the on-chip propagated waveform of the ESD stress on the power supplies, the substrate and through the protections. This paper presents an on-chip oscilloscope developed for in-situ measurement of real ESD event in 65 nm CMOS technology. Dynamic measurements of overshoots, substrate fluctuation and onchip radiated fields presented in this paper are performed with 20 GHz bandwidth.

1. Introduction

System level ElectroStatic Discharge (ESD) has become a major concern in embedded electronic products. Fast electrical signals like the ESD ones can cause severe system reliability issues like destruction of the ICs (due to over-voltages or thermal effects) or functional failures like RESET, clock period losses, or erroneous data. It is extremely difficult to predict these failures because interactions between the Printed Circuit Board (PCB) and the protections inside the chip can be very complex. In previous papers, we demonstrated that the passive components, the parasitic elements of the package can influence the ESD current path that is not predictable by conventional ESD approach [1,2,3]. Even the power supply value can dramatically lower the Integrated Circuit (IC) robustness from 7kV to 1kV as it has been depicted in papers [4,5].

Moreover, inside the chip, even if the ESD stress is well controlled by the ESD protection strategy, it induces over-voltages, substrate voltage fluctuation and local electromagnetic radiations that can cause electronic circuit to fail. In order to avoid these troubles, a complete methodology to anticipate system ESD failures is needed. Regarding ICs reliability during products life, the main question is: "what would be the ESD waveform inside the chip?" To answer this question, we decided to develop a time domain on-chip measurement method that allows capturing the in-situ shape of the ESD stress. In this paper, we perform measurements of the noise induced on the power supplies, of the substrate voltage fluctuation during ESD and of the radiated field from the power rail to the inside core chip. The method used is based on a sample and hold technique. This method has been successfully used years ago for the on-chip measurement on signal integrity on interconnects [6,7,8]. Since, other labs decided to use this technique to analyze on-chip signal integrity [9,10,11,12] . The goal here is to improve this sampling technique to be able to make direct on-chip measurement of over-voltages generated by an ESD stress on the power supply network that can be more than twice the voltage supported by the technology. We expect from these measurements a good understanding of the current propagation within the I/O ring, and so to have a better knowledge about failure mechanisms.

The system is implemented in a 65nm CMOS technology The chip has been designed in collaboration with the French Space Agency – CNES (Centre National d'Etudes Spatiales) and the laboratory of Integration from Material to System (IMS) to study the impact of ESD stress and aging on deep sub-micron technologies. The idea is to extract from on-chip measurement, information about the ESD perturbation inside the chip. In section II, we will describe the on-chip measurement system providing more than 100GHz measurement bandwidth (BW). Some dedicated on-chip probes to perform high voltage measurements have been developed to reach

the 20GHz bandwidth without destructing the measurement system itself. Detail of the voltage probes will be given with its limitations. In section III, we will present the implementation of this ESD waveform sensor to perform a set of measurements into a 5 IO structure, and one core function. The chip is mounted into a CQFP 120 pin package and into its final printed circuit board (PCB) configuration. The measurements show that the impact of the parasitic elements of the package and PCB will influence the on-chip propagation and triggering delays. The objectives of these measurements are to get on-chip waveforms of ESD induced noises. In the last section, the device under test is stressed using a Very Fast Transmission Line Pulse (VF-TLP) generator. Some results will be presented and discussed, disclosing the complexity of analyzing ESD related failures.

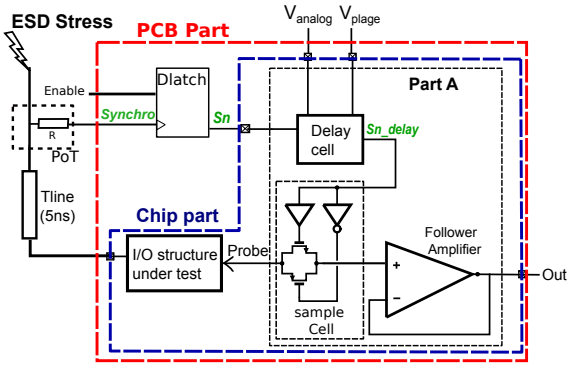

Figure 1: Schematic diagram of the measurement setup including ESD injection, PCB basic signals and on-chip sample and hold technique.

2. Measurement Technique and implementation

By implementing a sampling technique into the chip we are able to get benefit from the technology performances, and to have a very high measurement bandwidth. This could be useful to see the on-chip triggering of the ESD protections and the noise induced at each tested point. The on-chip sensor we published in 2000 [6,7] is not able to handle such stress and some dedicated attenuation probes have to be designed to catch only a part of the signal with sufficient measurement bandwidth range. Part 1 of this section will describe the principle of the on-chip "sample and hold" technique, with the dedicated voltage sensor we developed. In part 2, the implementation of the sensor to characterize ESD noise induced in a CMOS 65nm technology is describe.

1.1. Sampling technique

The schematic diagram of the "sample and hold" measurement is reported in figure 1 (part A). The device is composed of 3 main blocks: A "**delay cell**", a "**sample cell**" and a "**follower amplifier**" to drive the sampled signal out of the chip. The voltage range limitation of the sample cell is between 0V and 2.5V, i.e. the maximum voltage allowed by the technology. Few pico-seconds before the triggering of the voltage protections, the on-chip voltage can increase to a level more than twice the one the technology can handle. Therefore, a dedicated effort was carried out to develop probes with sufficient bandwidth and attenuation. The probes are different depending on the voltage measurement to be performed. The required attenuation range was optimized via simulations.

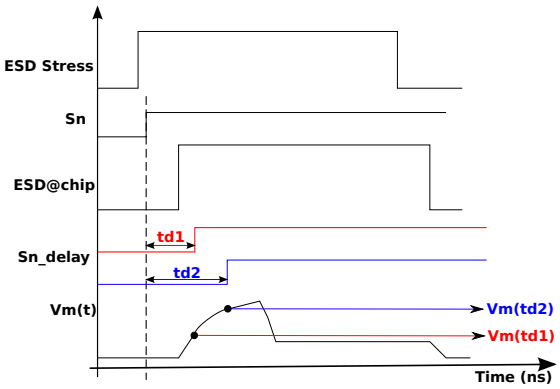

Figure 2: Waveform reconstruction of the sampling Circuit.

The sampling sensor works as follows: an ESD stress is generated and is split in two parts. Using a Pick of Tee (PoT), a small part (1V to 2V) of the ESD is directly used to generate the sampling circuit synchronization via a Dlatch circuit. Additional signal, not reported on fig.1, allows the reset of the Dlatch between each sample. The latch generates the Sn signal, between 0V and 1.2V, which is directly used to synchronize the sampling sensor on the ESD stress. The major part of the ESD stress (ESD@chip; Fig. 2) is applied to the IO structure under test after a small delay introduced by a coaxial cable, Tline. Approximately 5ns are necessary to drive the Sn signal from the input pin to the on-chip sensors plus 2ns for the Dlatch response. to get the necessary delay, a 5ns cable is inserted between the PoT and the chip injection. We can adjust the beginning of the sample using an additional on-chip delay cell.

The sensor probe samples the signal *Vm(t)*. From the synchronization signal *Sn*, a controlled delay (*td1*; fig. 2) is introduced to generate the *Sn-delay* signal, which controls the "**sample and hold**" block. The sample value, *Vm(td1)*, is stored into the input capacitance of

the follower amplifier and externally driven out of the chip. For each new *Sn* signal, the delay is increased and a new value of "*td2*" delay is sampled (*Vm(td2)*). The full waveform is externally reconstructed using mathematical fitting from measurements on a calibration structure.

The delay cell, based on a voltage control oscillator (VCO), has been fully described in [1] and is controlled by two analog signals, "Vplage" and "Vanalog". The figure 3 reports the electrical schematic of the main transistors involved into the delay control. By increasing "Vanalog", we extend the sampling delay following a linear curve as reported in figure 4. "Vplage" acts as a scalable factor like the timebase button of an oscilloscope. For Vplage = 0.7V, the time resolution is 10ps/10mV (100Ghz equivalent BW), with a time range of observation around 2ns. The maximum measurement range, 50ns, is obtained for Vplage = 0.3V, which is close to the threshold voltage of the NMOS transistor, with a BW of 4GHz. It makes clear that the control voltages have to be adjusted with care, and the layout of the delay cell have to include internal capacitances, shielding and a lot of substrate contacts to avoid any analog fluctuation during the measurement.

The sampling cell is a transmission gate (Tgate - Fig 1) realized by one Nmos and one Pmos transistor with minimum gate length and width. Compensated buffers allow controlling a cut-off with a small offset. To perform signal integrity measurements the sampling cell is directly connected to the node through a small wire introducing only few femto-Farad to ground. For ESD measurement, this is not possible. To perform high voltage measurement without destroying the MOS input transistor of the amplifier we decided to get benefit from capacitance coupling properties.

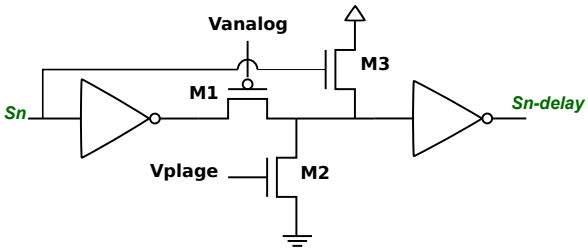

Figure 3: Circuit diagram of the delay cell

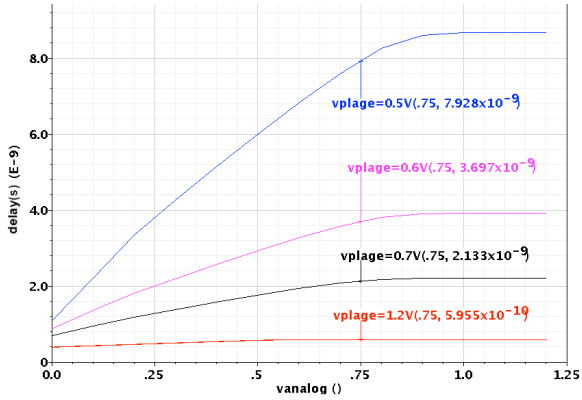

Figure 4: Variation of the delay depending on Vplage and Vanalog.

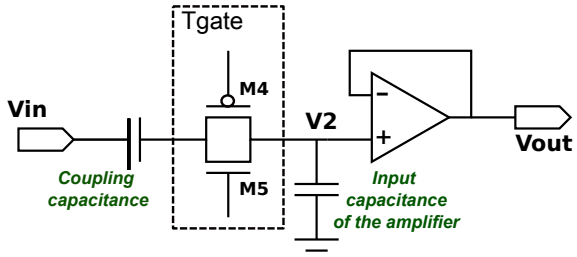

Figure 5: Schematic of the transmission gate with a coupling capacitance of 2fF to measure high voltages.

A small part of the line exposed to the ESD is coupled to the probe through an equivalent capacitance of a few femto-Farad. The equivalent schematic (see Fig. 5) of the final equivalent probe is composed of a coupling capacitance, the equivalent on-resistance of the MOS M4, M5 of Tgate and the input capacitance of the follower amplifier. The coupling capacitance is realized using metal layers. By adjusting the dimensions, we define the coupling capacitance and its value adjustment allows easily tuning the attenuation level. Table 1 gives the simulated and measured attenuations values for the probes we have connected to the power supply bus of the test chip.

Table 1: Simulated and measured voltage attenuation of the probes versus coupling capacitance.

Bus (coupling Capacitance)	*Measured Gain (dB)*	*Simulated Gain (dB)*
VDD (9.2fF)	*-11,5*	*-9*
GND (9.2fF)	*-11,5*	*-9*
VDDE (0.565fF)	*-30*	*-26,5*
Boost (0.577fF)	*-29,5*	*-26,3*
GNDE (2.5fF)	*-17*	*-15*
Trigger (2fF)	*-21*	*-18*

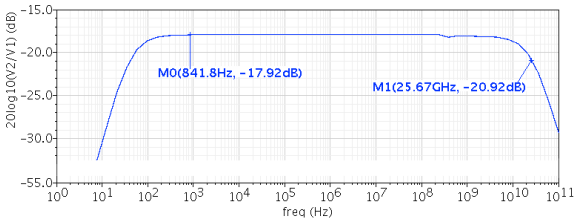

Figure 6: Transfer function of the probe with a 2.5fF coupling capacitance (simulated).

To get the measured gain, we performed the on-chip measurement of a well-defined 1V pulse directly injected on the buses and extract the gain. The transfer function with 18dB voltage attenuation is obtained for a measurement bandwidth around 21Ghz for a coupling capacitance of 2fF as reported in figure 6.

The silicon surface consumed for the full sensor is around 770µm^2. Its layout is presented on Figure 7.

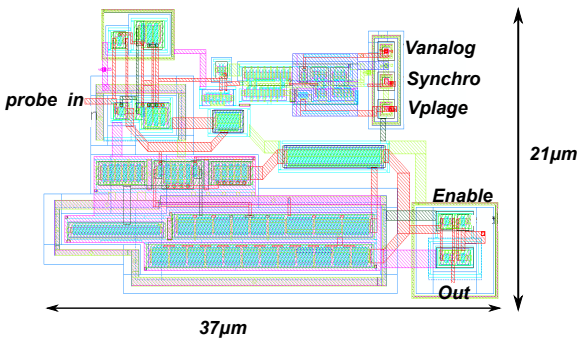

Figure 7: Layout of the sampling sensor

1.2. Calibration of the measurement system

The exact values of the delay introduced by the delay cell and the of DC offset of the voltage follower amplifier need to be known for the implemented on-chip sampling technique to be fully operational. Since these values may vary from chip to chip, a calibration step must be implemented. Some additional circuits are added to the chip to accomplish this task. A computer-based data acquisition system is used to drive these circuits, acquire their responses and in-house software has been developed to compute the two data mentioned above, besides its oscilloscope driving capabilities. The two calibration setups are described below.

T o acquire the delay introduced by the programmable delay cell, a ring oscillator has been designed making a closed-loop chain with 21 inverters and the programmable delay cell. The output is driven out of the chip via a frequency divider. The program is able to sweep the two analog voltages *Vanalog* and *Vplage* to change the oscillation frequency. The results are reported on figure 4. From these curves, a polynomial fit reconstructs the time dependency. This calibration technique is simple and accurate thanks to its small jitter. For the highest oscillation, frequency the measured jitter is around 1MHz that corresponds to a 2ps variation, which is acceptable regarding the targeted resolution.

A second calibration circuit has been designed to evaluate the DC offset introduced by the voltage follower amplifier and the dynamic offset coming from various effects at the sampling switch level (charge injection, clock feedthrough, etc...) [13]. We directly sample the analog signal on and external pad. This allows extracting the static and quasi-static offset. As expected, the transmission gate introduces a negligible offset. The follower amplifier is perfectly linear from voltages 20mV to 2.4V when it is supplied in the range 0 - 2.5V. The introduced dynamic offset introduce is around 50mV and mainly constant over the observable range. It is subtracted to the measurement by software.

1.3. Implementation into the chip

The structure under test (stressed by ESD) is composed of two power supplies, 1.2V(VDD and GND) and 2.5V(VDDE and GNDE) and one digital input. The ESD strategy provided by the silicon founder is reported in figure 8. The bus ring under study is composed of these two power supplies and two signals to trigger the ESD protection structures, *Trigger* and *Boost*. These six voltages are measured synchronously with probes using various coupling capacitances (as reported in table 1) and driven out on six analog pads. *Boost* is obtained after a simple diode (connected between the pad and the boost signal going to the trigger block), and *Trigger* activates all the clamps between VDDE and GNDE. When a stress occurs between VDD and GND, a local trigger is generated to activate local clamps. The objective is to detect the over-voltages, generated before the triggering of the ESD protections, inside the chip core, and to understand the complex current paths under system level condition, taking into account the parasitic elements of the board that can influence the internal behavior of the protections [2][3]. Substrate voltage fluctuations are computed at 10µm and 20µm from the I/O ring when the ESD is evacuated by the on-chip protections. For embedded application exposed to ESD, ESD-induced noises could introduce failures into the core chip. These measurements aim at characterizing the substrate noise level during an ESD. In a same way we perform the measurement of the magnetic field induced into the core at 10µm and

20µm from the I/O ring using a 20µm square loop connected to the ground through 5Ω. A Total of 10 sensors have been deployed around this 5 I/O structure. To control the measurement and for the calibration structures, 15 additional I/Os were used (4 for sensor supply, 6 for synchronic outputs, 5 for analog and synchronization control signals). Four I/Os were dedicated to calibration structure. This technique requires a significant amount of surface silicon and is not useful for final application chip. It is mostly dedicated to new product development and technology optimization

2. Measurement results

A 20V VF-TLP (300ps rise time – 5ns duration) is first injected between VDDE and GNDE. Figure 9 reports the six voltages synchronously measured by the sensor.

Figure 10 gives the equivalent protection scheme provided by the founder involved into the stress. The schematic also includes the inductances of the package (Lpack) and PCB (Lpcb).

The VDDE voltage increases up to 5V followed by the Boost signal. At the same time the associated GNDE ground follows, and saturates at about 0.8V. A small capacitance between VDDE and GNDE called internal decoupling capacitance (Cint; fig.10) tends to pull up the ground voltage toward VDDE due to the instantaneous current it0 (reported in red in fig.10). GNDE ground of the chip is connected to ground through an equivalent impedance of 10nH (Lpcb). This means that the ESD current cannot be drained quickly by the global GNDE to the PCB, and as a result, GNDE potential increases.

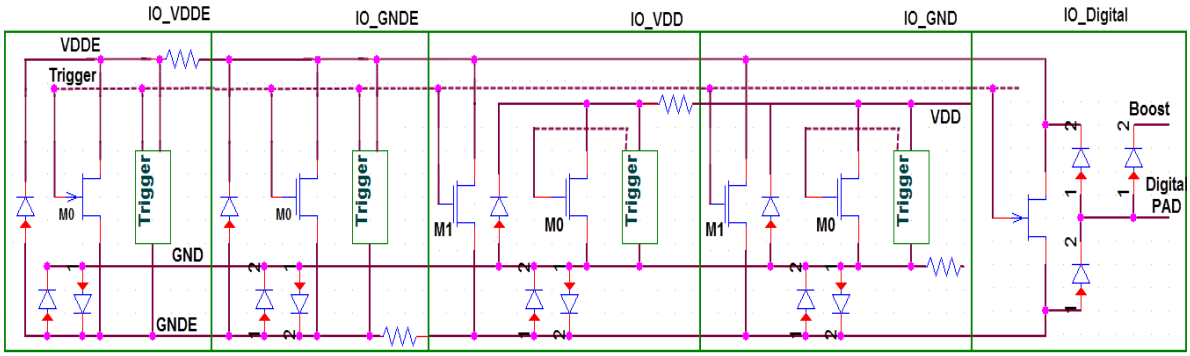

Figure 8: I/O structure under test and its ESD protection strategy.

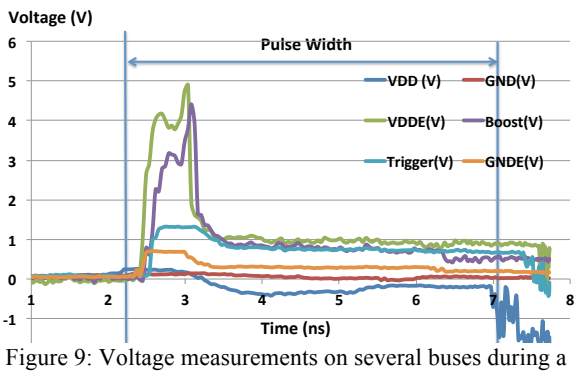

Figure 9: Voltage measurements on several buses during a 20V TLP injection between VDDE and GNDE.

The current tends to rise instantly to the GND rail through the protection diode D2 that provides a less inductive path, thus keeping GNDE voltage at 0.8V. The measurements show an overshoot before the triggering of the protections of 4.2V maximum. When the protection is fully on, the voltage between VDDE and GNDE is 0.65V, which is the snapback voltage, measured by quasi-static TLP. On-chip voltage measurements allow getting deeper insight into the analysis of the ESD protection triggering:

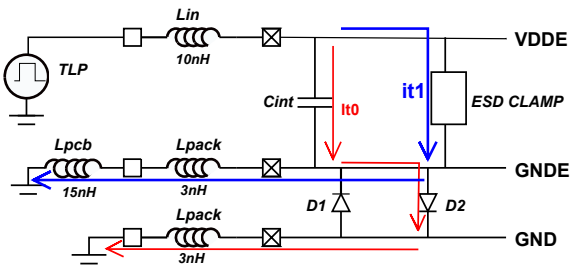

Figure 10: Equivalent electrical schematic of the elements while an ESD is injected between VDDE and GNDE.

- At time t=2.4ns VDDE starts to increase 250ps after the injection. This delay is due to the input inductance (Lin = 10nH) added between the TLP generator and the chip.
- The Boost signal follows VDDE with 100-150ps

delays. The shape of this signal is the same as the VDDE one but delayed and its voltage value is reduced by the triggering voltage of the Boost-diode.

- The Trigger signal that triggers the ESD protections (ESD clamp) rises up to 1.2V at t=2.6ns, around 200ps after the VDDE voltage.
- Between t= 3.05ns and t=3.2ns, VDDE voltage drops to 1.3V. This shows that 450ps are needed between the generation of trigger signal and the turn-on of the ESD structures.
- 150ps latter, the ESD protection structures are fully on and the voltage between VDDE and GNDE is around 0.7V. A TLP I/V characterization has been performed between VDDE and GNDE and showed that the ESD protection structure exhibits a strong snapback at 0.65V. The current follows the It1 path (fig. 10).

Such phenomena cannot be observed by classical TLP measurements. The on-chip technique allows measuring the over voltage before the triggering of the protections. The external inductances from the package and the PCB introduce delays that can cause the IC failure.

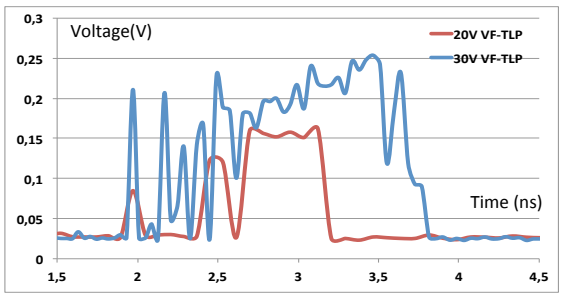

Figure 11: Substrate fluctuation at 10µm from the I/O Ring with 20V and 30V VF-TLP stress.

Figure 11 presents the on-chip measurement of substrate voltage fluctuation at 10µm from the ring while a 20V and 30V VF-TLP is injected between VDD and VSS. Even if the ESD stress if small, it induces 0.25V noise, not to far from the threshold voltage, Vt, of such technology, which is 0.3V. The substrate noise increases respectively to the amplitude of the stress, but it has twice duration with 30V.

Other results present the radiated field induced inside the core at 10µm. The field is measured using a magnetic probe of 20*10µm2 of metal 5 layer. A 5 Ω resistance drives the signal to the on-chip sensor. Measured field at 10µm from the ring is reported in figure 12 for 8V and 20V VF-TLP injected on VDD, and 20V VF-TLP injected in VDDE. 8V injection introduces a small voltage into this configuration. With 20V injection the noise induce is non negligible. Depending on the pad injection, the noise induce could be double. This is due to the position of the power rail on the ring: VDD rail is closed to the chip core.

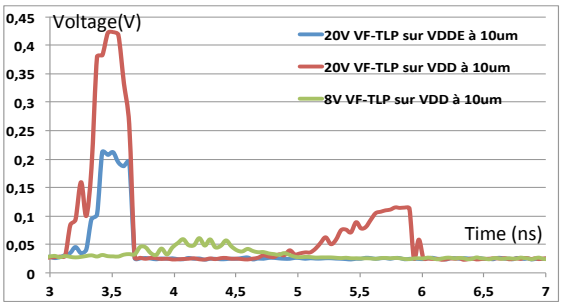

Figure 12: Induced Voltage from magnetic field at 10µm of the I/O Ring with 8V-20V and 30V VF-TLP stress.

4. Conclusion

One of the critical point to understand failure mechanism in ICs undergoing ESD system level stress is that the actual current paths or the shape of the signals inside a chip are not accessible. System condition is while an ESD can occurs on the final product and goes directly to the chip as defined by IEC 61000-4-2. The system can be powered or not. Into this study we didn't power the IC, but all the passives and parasitic elements of the package and PCB are taking into account.

Taking into account this consideration, we decided to develop on-chip measurement method based on sample and hold to observe the signal waveforms inside the chip. In this paper, details of the measurement system and probes allowing high bandwidth (20GHz) are presented as the calibration methodology.

The on-chip measurements of the ESD impact when the stress is injected into a 5 I/O structure give us good results and allow precisely extracting the delays in the triggering of the ESD protections. The analysis of substrate and field noise induced by an ESD stress is also detailed. We demonstrate that on-chip sampling technique can be very useful for on-chip characterization of ESD. It can give a lot of information concerning the various ESD propagation paths that directly impact on the final robustness of the product.

Acknowledgments

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