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Characterization of Changes in LDO Susceptibility After Electrical Stress

Jianfei Wu, Alexandre Boyer, Jiancheng Li, Sonia Ben Dhia, *Member, IEEE*, and Rongjun Shen

Abstract—The low dropout voltage regulator (LDO) is very sensitive to electromagnetic interference (EMI) coupled onto the power supply, with concomitant output voltage offset. Most electromagnetic compatibility analyses of the LDO do not account for the effects of ageing. However, device ageing can degrade the physical parameters of semiconductor devices and can worsen the effect of EMI. This paper analyses the drift in LDO immunity after accelerated ageing. A large number of measurements that show the variations in the test results for dc characteristic, impedance, and immunity reveal increasing susceptibility after electrical accelerated ageing.

Index Terms—Ageing, electromagnetic compatibility (EMC), electromagnetic interference (EMI), immunity drift, low dropout (LDO) voltage regulator, offset, susceptibility.

I. INTRODUCTION

IN recent years, with the ever-changing development of CMOS technology combined with the demand from the industry society [1], [2], IC designers have had to face tougher reliability problems [3] due to higher integration densities. Ensuring the electromagnetic compatibility (EMC) of such circuits is increasingly complex but a new and important challenge is to ensure EMC over the full service life of the product. Greater attention should be paid to electromagnetic robustness (EMR) [4], which aims to study and evaluate the impact of circuit ageing on EMC [5], [6]. For example, some recent experiments on a phase-locked loop [7] have shown drifts in immunity after accelerated stress.

Analog circuits such as LDO regulator are very susceptible to EMI transferred into their input terminals. The LDO voltage regulator is widely used in modern electrical systems with severe EMC problems. The performance of electronic devices is directly linked to the integrity of the power supply voltage. And the robustness to EMI is extremely important for long term electronic applications. Various papers have described the failure mechanisms of LDO regulators under conducted EMI. These failures are linked to the operational amplifier (op-amp) [8], [10]

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or bandgap circuit cell [9], [10]. Research focuses mainly on the analysis of EMC failure mechanisms and low-susceptibility design techniques, while little attention is given to the LDO's real-application environment and its effect on susceptibility.

This study describes an original study on the change in LDO susceptibility induced by electrical stress. In order to provide a better insight into the impact of intrinsic LDO circuit degradation, a novel ageing study methodology is proposed giving time-independent variations both on the functionality and the electromagnetic behavior of the LDO. Section II gives a general description of EMR issues and the methodology used to study the effects of LDO ageing on electromagnetic susceptibility. Section III presents the LDO test chip, measurement set-up, and conditions for accelerated ageing. Experimental results and an analysis about a likely origin of the decrease of susceptibility are presented and discussed in Section IV. Finally, Section V provides the conclusion and future work.

II. EMR ISSUES AND METHODOLOGY FOR THE STUDY OF LDO AGEING

A. General Ageing Issues on IC Susceptibility

The service life of ICs can generally be described in terms of a “bathtub” curve: infant mortality, normal life, and wear out. Survival of the fittest for newly fabricated ICs can eliminate the influence of infant mortality. After a long operational period of normal use, electronic devices begin to wear out on account of intrinsic degradation mechanisms such as electromigration [11], hot carrier injection (HCI) [12], negative bias temperature instability [13], time-dependent dielectric breakdown [14], etc.

Two questions arise when considering the impact of device degradation on robustness to EMI: whether ageing reduces the robustness to EMI, and the risk of the circuit no longer being compliant with the susceptibility level.

Fig. 1 illustrates the effect of IC ageing on susceptibility. For “fresh” components, the manufacturer provides the initial susceptibility level (ISL). ISL can be ensured after comparing with the customer's specified limit. After ageing, the final susceptibility level of the IC may change: what is expected is a general improvement in the immunity, giving a more robust IC. Otherwise, the safe margin may become an unsafe margin, and an unsafe margin may change to a high-risk margin, making immunity problems more likely. Hence, EMR issues should be considered during IC qualification.

B. LDO EMR Study Methodology

The principle of accelerated ageing is that of applying stress conditions to accelerate intrinsic degradation mechanisms. Susceptibility EMR characterization of a circuit consists in

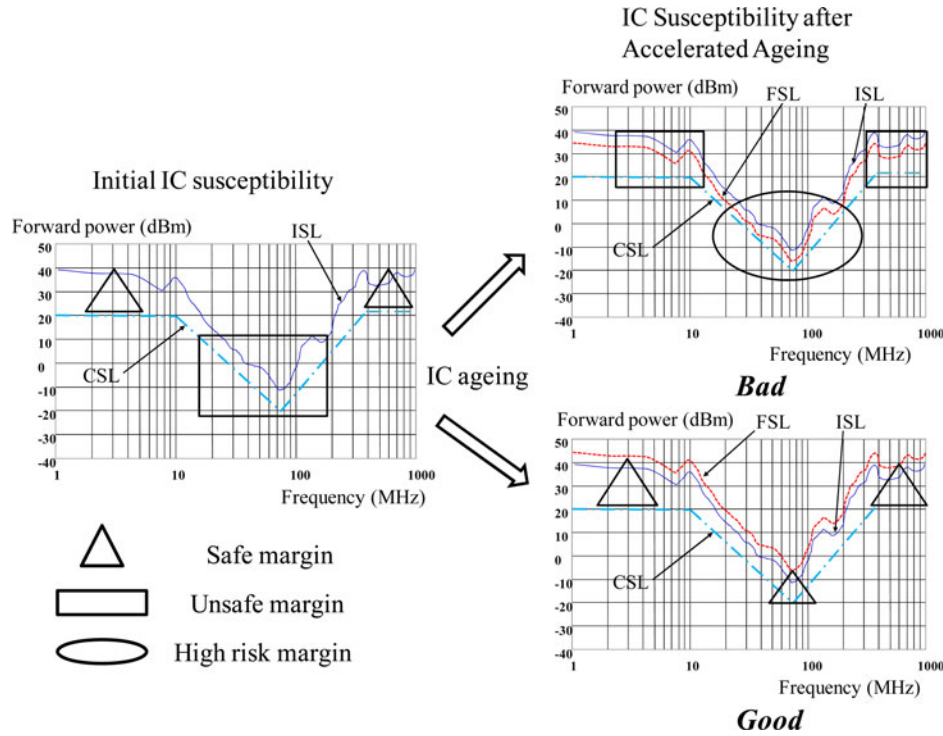


Fig. 1. Effect of IC component ageing on susceptibility.

measuring the change over time of its susceptibility to radio frequency interferences (RFI) before and after circuit ageing. To evaluate device lifetime and primary wear out mechanisms effectively, accelerated life tests are used. These consist in applying stress conditions to the device under test (DUT) (electrical overvoltage stress, high or low temperatures) in order to accelerate the rate of intrinsic damage and, thus, circuit ageing.

The aim of EMR characterization is the comparison of circuit susceptibility levels before and after the accelerated ageing process. Previous work [6], [7], [15] only focuses on two results of fresh and aged states and does not examine the variation in immunity during the ageing process. This paper presents an original methodology for the study of ageing as shown in Fig. 2, which presents our proposed experimental methodology for the study of drifts in immunity and electrical characteristics during the ageing stress cycle. The methodology is based on a measure-stress-measure test flow, which consists in applying electrical stress on LDO circuit and interrupts the stress during short period “*t*” for characteristic test purpose. The test time “*t*” (1 h) is very short compared with stress time “*T*” (1 day) to avoid recovery. After setting the ageing time to *n* multiples of *T*, the test data processing can give the susceptibility variations of the LDO with a time step *T*.

III. DUT AND TEST SETUP

A. Description of the DUT

The LDO regulator under test was implemented in a test chip designed with the Freescale CMOS 90-nm process and aims to provide a regulated power supply voltage to a small digital core.

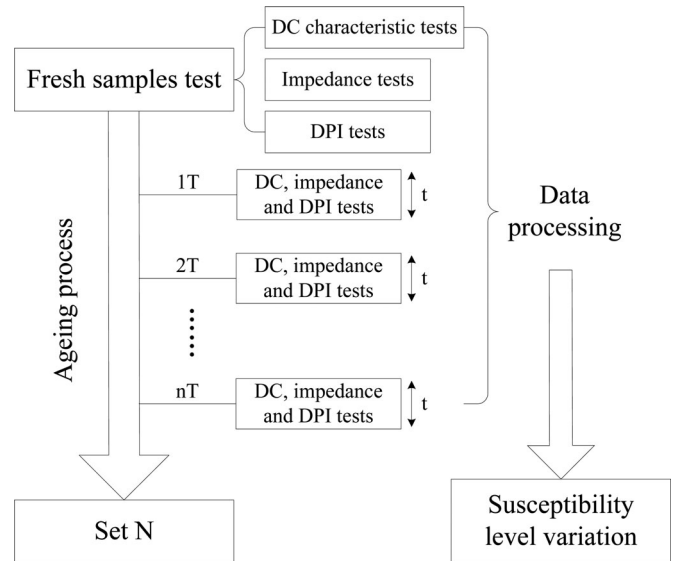


Fig. 2. Susceptibility EMR study methodology.

There are three regions for the LDO V_{IN}/V_{OUT} voltage characteristics: off, dropout, and regulation (see Fig. 3). Below $V_{D\text{dropout}}$, the output voltage falls rapidly with decreasing input voltages. Above $V_{D\text{dropout}}$, the LDO works in the regulation region with typical dc voltage $V_{IN(TYP)}$. In susceptibility tests, conducted EMI is applied to the power pin, causing two types of failure as illustrated in Fig. 3: failure type 1 is the residual harmonic noise coupled to V_{OUT} , while failure type 2 is an offset of the regulated voltage, induced by nonlinear operation of the device. The second type of failure is more harmful in real

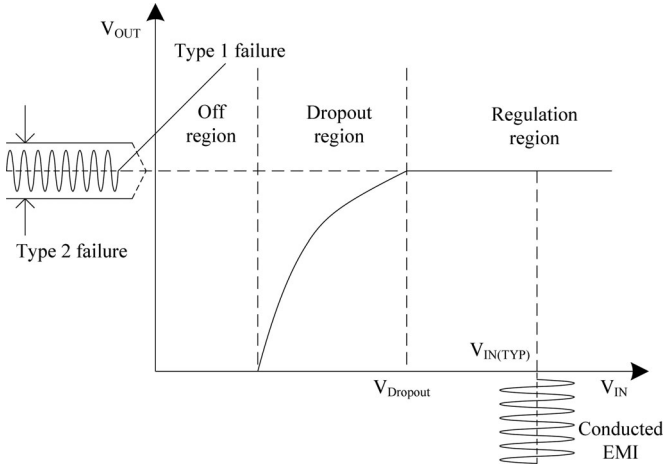


Fig. 3. Typical V_{IN}/V_{OUT} voltage characteristics of LDO under EMI.

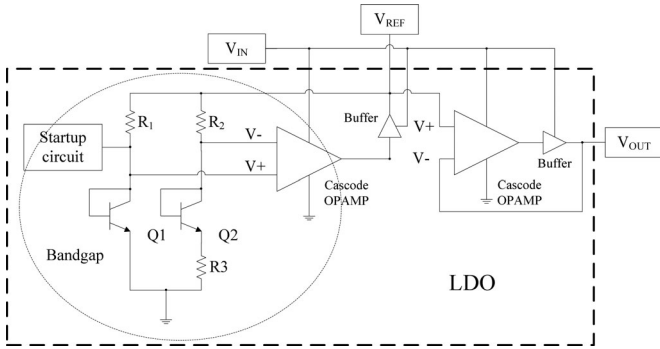


Fig. 4. LDO structure and general setup of input/output terminals [17].

applications since it cannot be filtered out. Hence, the following susceptibility tests are focused only on failure type 2.

Fig. 4 illustrates the internal structure of the LDO voltage regulator that contains a Kuijk bandgap [16] reference circuit and an output amplifier designed to work with a +3.3-V supply [17]. The nominal voltage of the bandgap reference voltage is +1.2 V and the gain of the output amplifier is 1. Bandgap reference circuit and regulator outputs are monitored through the terminals V_{REF} and V_{OUT} .

B. Accelerated Ageing Conditions

Electrical stress conditions (e.g., excess operating temperature or supply voltage) are applied to the DUT for a short period to accelerate the damage rate for the relevant wear out failure mechanisms. In this paper, the accelerated ageing condition is electrical stress, which is +5 V on the power supply V_{IN} (150% of the normal voltage of +3.3 V) [15]. Balancing the ageing time and effects, the chosen voltage +5 V is based on experiments done on single MOS devices to measure the degradations induced by dc stress. The ageing is applied until the DUT fails. Circuit tests were carried out every day ($T = 1$ day). All the tests were performed at ambient temperature. After seven days, the component had failed; hence, the ageing and testing last for the complete degradation of the LDO right up to an unrecoverable failure.

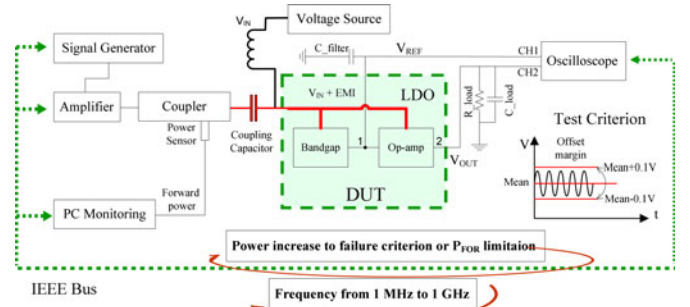


Fig. 5. DPI test bench for EMR study.

C. Conducted Susceptibility Test Setup

Measurements were carried out in accordance with IEC standard 62132-4: direct power injection (DPI) [18]. The test bench for the DPI measurements includes the board for the DUT, EMI generation, and injection path (signal generator, amplifier, coupler, and power sensor), dc voltage source, bias tees, and PC for bench control and DUT monitoring, as shown in Fig. 5.

Decoupling capacitors were removed from the power supply V_{IN} to ensure efficient coupling of EMI to the LDO input. In the test chip design, there is lack of on-chip load capacitor in op-amp which is crucial for output stability. A 47-nF capacitor (C_{filter}) is mounted to improve the output stability of the bandgap reference circuit. The regulated output V_{OUT} is loaded by a 330- Ω resistor (R_{load}) and a parallel 100-pF capacitor (C_{load}).

The dc offsets induced on both bandgap reference circuit and regulator outputs were monitored. A deviation of ± 0.1 V from the nominal output voltage V_{REF} and V_{OUT} is tolerated. As the nominal output voltage can change due to LDO ageing, the criterion is updated according to the new V_{REF} and V_{OUT} voltage to keep the same offset condition.

Other tests are also performed in parallel to the DPI tests. The dc characteristics of V_{OUT} (V_{IN}) and I_{IN} (V_{IN}) are monitored to analyze the degradation of the LDO. The impedance seen on the input pin is also measured by a vector network analyzer, as the susceptibility is directly influenced by the impedance of the DUT.

IV. MEASUREMENT RESULTS AND ANALYSIS

A. DC Characteristic Test Results

Fig. 6 illustrates the input I/V curve of the LDO after several stress periods. Compared with fresh and aged states, the off region shifts from 1.2 to 1.5 V and the dropout region shifts from 1.8 to 2.5 V. In the regulation region, the I_{IN} offset is about 0.4 mA (10% of the fresh value).

Comparing supply voltage V_{IN} and output voltage V_{OUT} of the regulator as shown in Fig. 7, the dropout and regulation regions of the regulator have the same offset tendency in the process of ageing for the same reason as that in the analysis of the drift in the input I/V curve. The dropout region extends 0.7 V into the regulation region. For the regulator, the significant

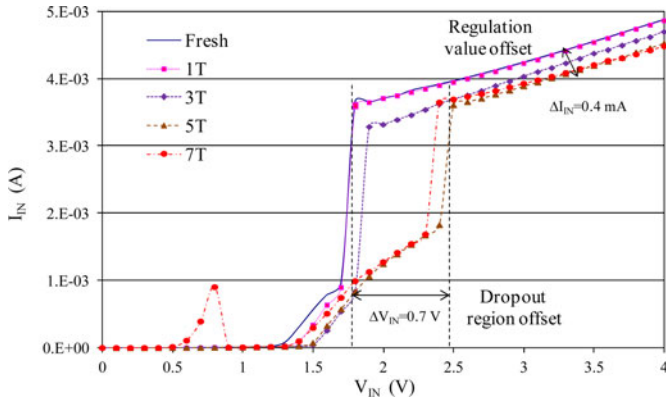


Fig. 6. Input I/V curve variation in ageing process.

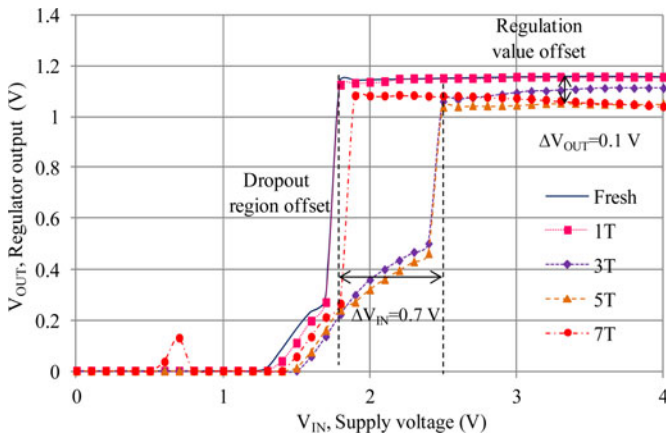


Fig. 7. Supply V_{IN} versus Output V_{OUT} of regulator in different stage of ageing process.

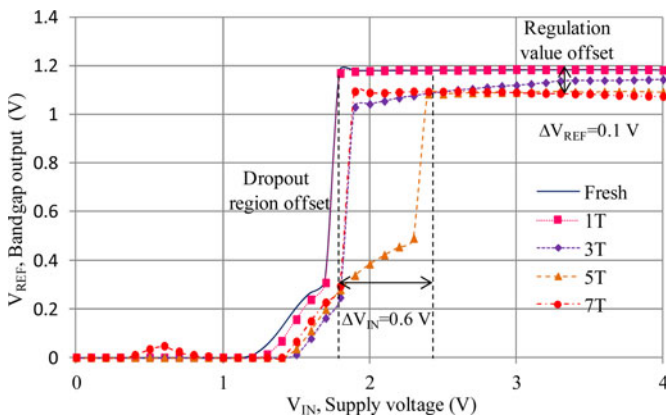


Fig. 8. Supply V_{IN} versus Output V_{REF} of bandgap reference in different stage of ageing process.

decrease of V_{OUT} is about 0.1 V compared with the fresh state in the regulation region.

The main reason is the shift of V_{REF} voltage (see Fig. 8) as there is only an op-amp follower structure between V_{REF} and V_{OUT} in LDO. Under an electrical stress of 5 V on the power supply, there is very little variation in V_{REF} , $V+$, and $V-$ in the bandgap reference circuit op-amp, which means that the voltages across R_1-R_3 , and $Q1$ and $Q2$ remain nearly

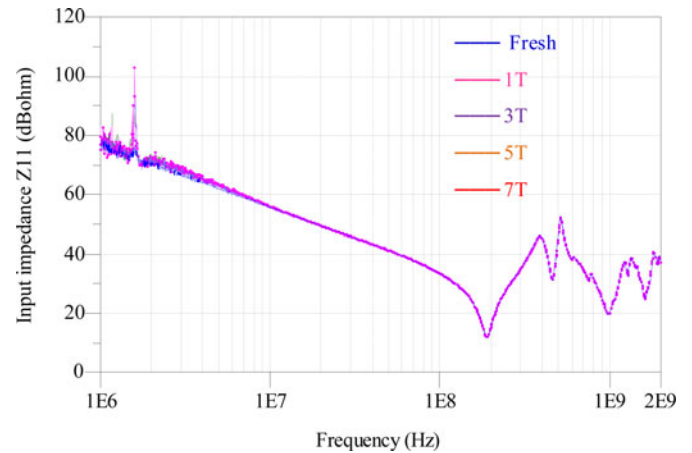


Fig. 9. Impedance comparison between fresh and ageing process.

constant and hence they are not stressed. Fig. 4 shows the two cascode op-amps and buffers with 5 V across them. The input offset voltage of the op-amp in bandgap reference circuit could be the source of the output voltage drift as the bandgap reference is equal to the sum of the theoretical bandgap reference voltage and the offset effect [17]. This offset comes from the mismatch of the transistor differential pair (difference of threshold voltage and mobility).

B. Impedance Test Results

Impedance measurement is carried by a vector network analyzer between power supply pin and ground pin of the LDO without bias voltage. The result in Fig. 9 shows that the impedance of the power distribution network of the LDO has not been affected by the ageing process.

C. Test Bench Repeatability

In order to characterize accurately the small variation in the test, the errors caused by measurement are minimized by observing suitable precautions in the experimental protocol and by verifying the long term stability of the measurement equipment. In order to verify the repeatability of the test bench, DPI tests are carried out four times on a given sample in a fresh state. As shown in Fig. 10, the average differences between DPI results are mostly negligible (the mean standard deviation is about 0.15 dBm). The DPI test bench offers a sufficient degree of repeatability.

D. Bandgap Reference and Regulator Susceptibility Drift

Bandgap reference circuit and regulator susceptibility variations are presented in three parts: forward power comparison at different frequencies with time, immunity level comparison with time step T in the frequency domain, and decreasing value comparison between fresh and aged $7T$ states.

Fig. 11 shows the susceptibility with changing at four arbitrarily selected frequency points. For the bandgap reference circuit, four frequency points of 30, 100, 199.5, and 501.2 MHz are chosen to compare the immunity from day one to seven.

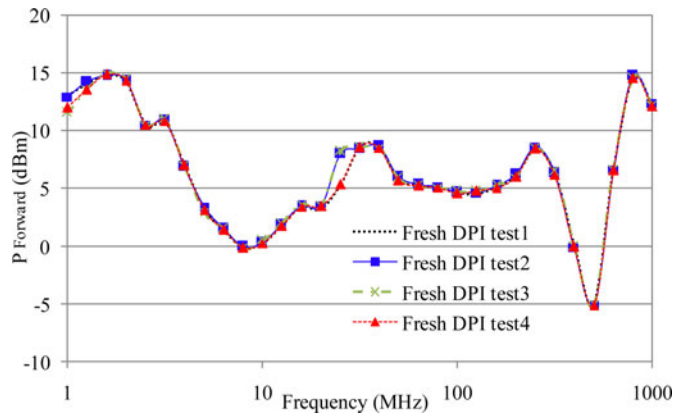


Fig. 10. Test bench repeatability tests of fresh sample.

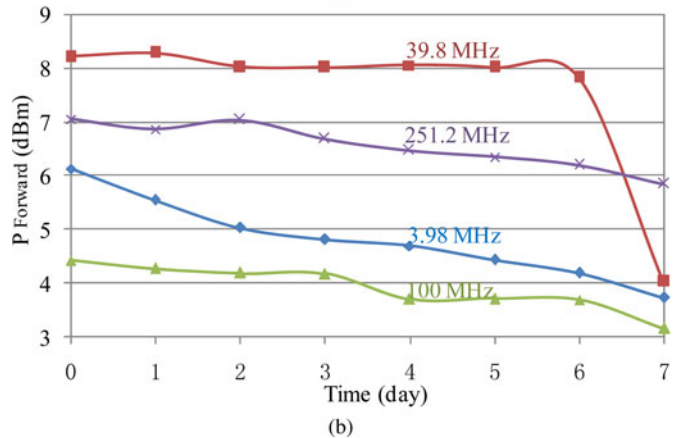
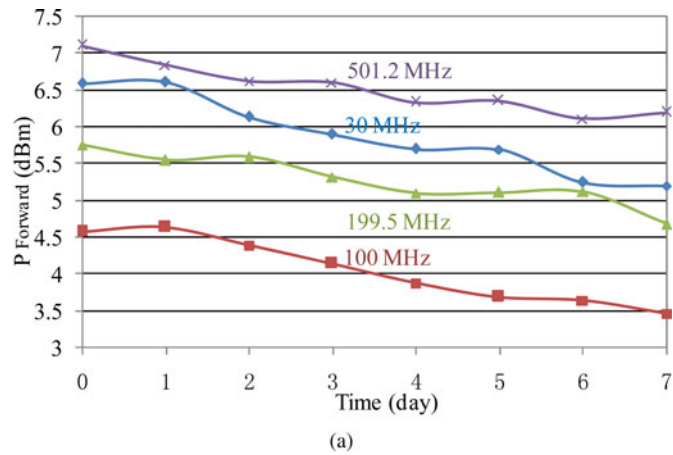


Fig. 11. Example at four frequencies with respect to ageing time of: (a) bandgap reference circuit and (b) regulator.

For the regulator, four frequency points of 3.98, 39.8, 100, and 251.2 MHz are chosen. There is a sharp drop in injected power from 8.0 (5 *T*) to 4.0 dBm (7*T*) at 39.8 MHz as the failure type changes from positive offset to negative offset. The results show that the immunity of the LDO and the bandgap reference circuit decreases continuously with stress time.

Fig. 12 shows, over a wide range, the reduction in the immunity of the bandgap reference circuit (the samples are broken when test Kuijk bandgap circuit below 30 MHz with no failure but over current even not reach the maximum power) and

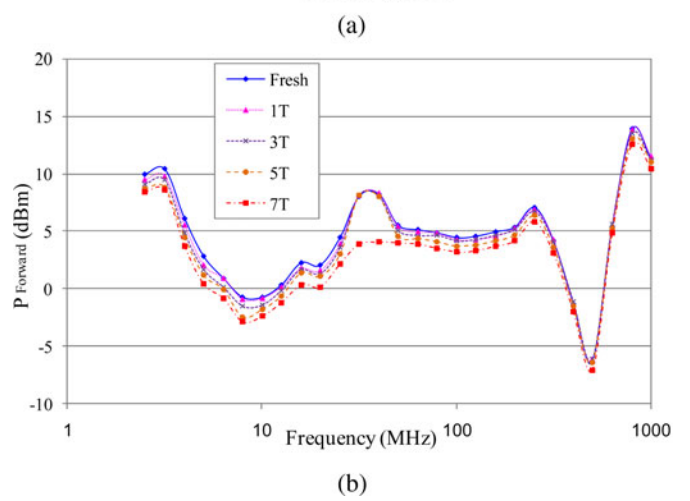
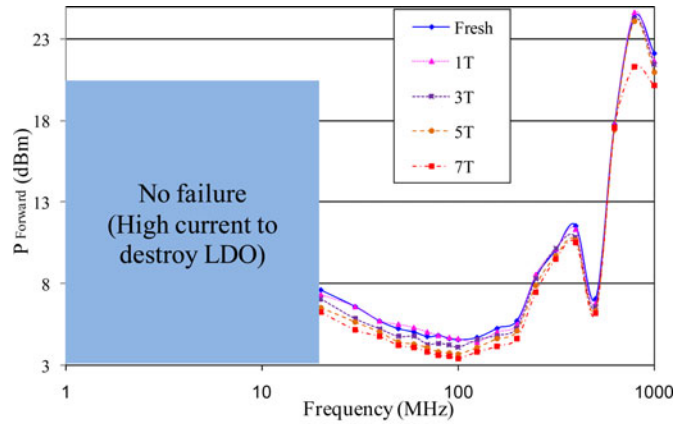


Fig. 12. DPI measurement results for: (a) bandgap reference circuit and (b) regulator in ageing process.

LDO to conducted EMI. The reduction of robustness to EMI is correlated with the degradation of the bandgap reference circuit and regulator characteristics revealed by the results in Figs. 6–8. As illustrated in Fig. 12(a) and (b), there is a sharp drop in power in the bandgap reference from 24.1 (5*T*) to 21.3 dBm (7*T*) at 794.3 MHz as the failure type changes from positive offset to negative offset. For regulator in frequency 30–40 MHz, the failure type changes from positive offset to negative offset after ageing. So the regulator output (two op-amp effects) has the sharp drop in these frequencies. But for frequencies around 800 MHz, the failure types are different: the failure on V_{REF} changes from positive offset to negative offset but the failure on V_{OUT} does not change after ageing.

The relative variations in the susceptibility levels for the bandgap reference circuit and regulator after seven days are presented in Fig. 13(a) and (b), respectively.

Fig. 13(a) shows the increase in susceptibility between 7*T* and Fresh for the bandgap reference circuit. The maximum Δ power is -50.6% at 794 MHz, where the failure type changes. The average Δ power over the whole frequency range is -22.5% .

Fig. 13(b) shows the increase in susceptibility between 7*T* and Fresh for the regulator. The average Δ power over the whole frequency range is -29.3% . After comparing the DPI results between aged and fresh states, the decrease in susceptibility

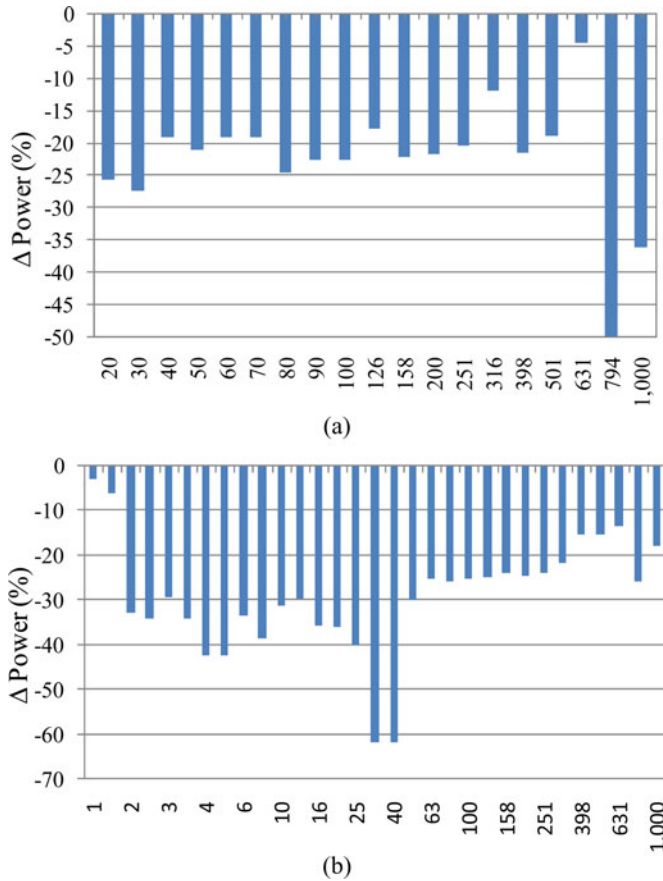


Fig. 13. Susceptibility level increases between 7T and Fresh for: (a) bandgap reference circuit and (b) regulator.

level indicates the frequency dependence of the ageing effects. Below 2 MHz, the offset is not obvious as the output op-amp works in feedback mode, where EMI is eliminated and is less affected by the electrical ageing condition. Moreover, the unstable test results in this frequency range are due to degradation of measurement accuracy by the noise floor of the power sensor. Δ power seems to be independent of frequency up to about 400 MHz except at 31.6 and 39.8 MHz, where the maximum Δ power is -61.7% due to the changeover of failure types.

E. Susceptibility Drift Mechanism Analysis Part E

This part reuses known works about immunity of bandgap and op-amp to propose a hypothesis about the origin of the susceptibility level shift. Numerous publications such as [8]–[10] have highlighted the fundamental role of op-amp differential input in the mechanism of generation the dc offset in presence of EMI. The degradation of susceptibility of the regulator is certainly linked to a change of the characteristics of op-amp differential inputs induced by the electrical stress.

There are two folded cascode op-amps in regulator circuit. A simplified equivalent circuit of the differential input is depicted in Fig. 14. In order to make sure that the voltage fluctuations are enough small to prevent any switching off of differential pair of the transistors, we consider a case of weak non linearity of the differential pair.

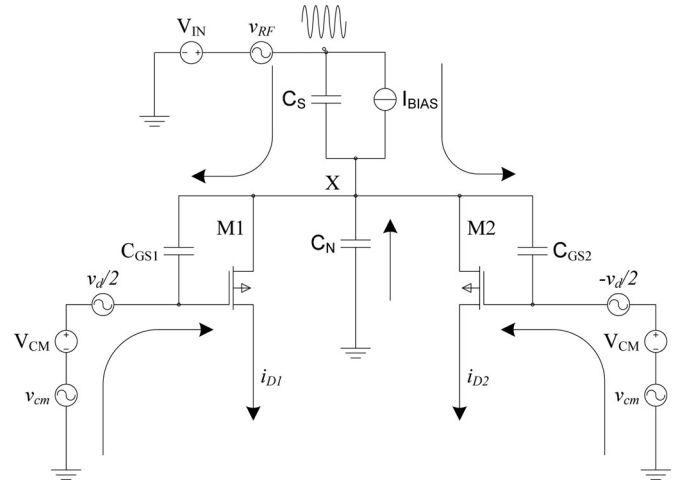


Fig. 14. Input PMOS differential pair under interference from power pin and differential pair inputs [9].

For the op-amp in bandgap, there are three paths for disturbance coupling: one from V_{IN} to the common node “X” of P-type metal-oxide-semiconductor (PMOS) differential pair by parasitic capacitors C_S (C_S represents the parasitic capacitance between V_{IN} and X) and C_{GS} (gate-to-source capacitance of M1 and M2); one from the output to the inverting and noninverting inputs by feedback circuit and C_N (C_N represents the parasitic capacitance between “X” and substrate) which offers the possible path for disturbance coupling from substrate [9]. For the op-amp in the regulator output, the first path is the same from V_{IN} . The noninverting input has the disturbance from the bandgap output; inverting input has the noise from op-amp output by the follower structure.

The output offset voltage is calculated in the presence of an RF signal (v_{RF}) with differential (v_d) and common-mode (v_{cm} and V_{CM}) components as depicted in Fig. 14. M1 and M2 are in saturation region and with the same size (suppose $W = W_1 = W_2, L = L_1 = L_2$). The differential drain current of M1 and M2 is Δi_D , which is established as follows:

$$\begin{aligned} \Delta i_D &= \frac{\mu_p C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 - \frac{\mu_p C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 \\ &= \mu_p C_{ox} \frac{W}{L} v_d (v_{cm} - v_x) + v_d g_m \end{aligned} \quad (1)$$

where v_x is the voltage at the common-source node of the differential pair. Suppose $C_{GS} = C_{GS1} = C_{GS2}, C_T = C_S + C_N$ and $g_m = g_{m1} = g_{m2}$

$$v_x = \frac{s(2C_{GS}) + 2g_m}{s(2C_{GS} + C_T) + 2g_m} v_{cm} + \frac{sC_S}{s(2C_{GS} + C_T) + 2g_m} v_{RF}. \quad (2)$$

So

$$\begin{aligned} \Delta i_D(s) &= v_d(s) g_m + \mu_p C_{ox} \frac{W}{L} v_d(s) Y(s) \\ &\quad \times \{C_T v_{cm}(s) - C_S v_{RF}(s)\} \end{aligned} \quad (3)$$

where

$$Y(s) = \frac{s}{s(2C_{GS} + C_T) + 2g_m} \quad (4)$$

$$|g_m| = \sqrt{I_{BIAS} \mu_p C_{ox} \frac{W}{L}}. \quad (5)$$

The differential pair output current average dc offset $\Delta i_{D|avg}$ can be used to calculate the op-amp inputs voltage offset $\Delta V_{IN|diff}$ using the transconductance amplification g_m of the differential pair stage [9]

$$\Delta V_{IN|diff} = -\frac{\Delta i_{D|avg}}{g_m} \quad (6)$$

$$|\Delta V_{IN|diff}| = \left| \frac{\mu_p C_{ox} W}{2L} v_{d,pk} \frac{\omega}{g_m \sqrt{4g_m^2 + \omega^2} (2C_{GS} + C_T)^2} A \right| \quad (7)$$

where

$$A = C_T v_{cm,pk} \cos(\text{Ph}(\phi_{d-cm}) + \text{Ph}(Y(j\omega))) - C_S v_{RF,pk} \cos(\text{Ph}(\phi_{d-RF}) + \text{Ph}(Y(j\omega))). \quad (8)$$

Under ageing condition, over voltage stress is implemented on the bias current PMOS transistor (large V_{DS} , which can accelerate degradation mechanism such as HCI). Degradation mechanism such as HCI leads to a main reduction of mobility and increase of threshold voltage [15], [19], [20] which induces the decreasing of I_{BIAS} , the same with $|g_m|$ from (5). So the $\Delta i_{D|avg}$ is inverse to I_{BIAS} , the $\Delta i_{D|avg}$ will increase if I_{BIAS} decreases. Finally, the $\Delta V_{IN|diff}$ increases as it is in direct ratio to $\Delta i_{D|avg}$. As there is negative feedback on both op-amps and as they are stable, the feedback forces the differential current to cancel. So an offset is created on the output voltage. The immunity level decreases, which is match with the measurement results in ageing process.

To find the origin of the immunity degradation, the best solution is prediction by modeling and simulation. In [19]–[22], the authors presented the methodology of study ageing effects based on CAD simulations and modifications of MOS device parameters extracted from measurements. The modification of MOS transistor parameters, such as threshold voltage and mobility, may affect the immunity of LDO circuit. The perspective work will include SPICE simulations to validate the proposed demonstration aforesaid.

V. CONCLUSION AND FURTHER WORK

The aim of this paper is to clarify experimentally the immunity level variation in a circuit designed in CMOS 90-nm technology. Ageing induced by electrical stress has a significant influence on the electrical characteristics of an LDO as shown in the dc measurement results. The immunity level of the LDO and bandgap reference circuit decreases continuously with device ageing. Despite this degradation, the circuit remains operational but becomes less robust to EMI conducted via its power supply rail. This implies that certain margin for LDO susceptibility should be provided by manufacturers for some

specific applications. The aforesaid ageing study methodology can also be applied to other IC devices to assess the appropriate margin to compensate for the drift in immunity level.

The progressive drift in immunity level of up to 30% is correlated with the degradation of the LDO, it identifies the origin of the progressive reduction in level of immunity as wear out mechanisms due to electrical stress. However, evaluating the variation in immunity level by accelerated ageing conditions is costly in time and effort. An attractive solution is an approach based on modeling and simulation, as shown in [19]–[22]. With the susceptibility drift mechanism study, the immunity decreasing in ageing process is explained by mathematical analytical analysis of the op-amp input PMOS differential pair. In ageing process, the bias current decreasing is mainly responsible for the immunity decreasing.

Further study will focus on ageing-related variation in MOS transistor parameters to clarify the origins of LDO immunity variations (such as HCI degradation mechanisms in NMOS) and give an accurate prediction model of service life susceptibility for LDOs. Further work will use this methodology on LDOs with different architectures (other bandgap reference circuit types, other structures for the feedback circuit) to validate whether there will be degradation in the susceptibility.

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