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Experimental Investigations into the Effects of Electrical Stress on Electromagnetic Emission from Integrated Circuits

Alexandre Boyer, Sonia Ben Dhia, *Member, IEEE*, Binhong Li, Néstor Berbel, and Raul Fernandez-Garcia, *Member, IEEE*

Abstract—Recent studies have shown that the aging of integrated circuits may modify electromagnetic emission significantly. This paper reports on an experiment to elucidate the origins of emission level changes in a test chip using 90-nm CMOS technology. Circuit analysis, combined with electromagnetic emission and on-chip power supply voltage bounce measurements made during the application of electric stress, have identified the role of intrinsic wear-out mechanisms, which contribute to a progressive change in the transient current produced by the circuit.

Index Terms—Aging effects, electromagnetic emission, integrated circuits, semiconductor device reliability.

I. INTRODUCTION

RECENTLY, many publications have predicted a decrease in the lifetimes of new CMOS technology devices down to few years [1]. Technology scaling and the introduction of new materials in CMOS processes required for higher levels of integration and improving integrated circuit (IC) performance lead, as expected, to the occurrence of hard or soft failures and wear-out mechanisms (e.g., hot carrier injection (HCI), negative bias instability, electromigration, etc.) [2], [3]. This trend is a key issue in ensuring the long-term reliability and robustness of professional electronic products [4].

The drift in electrical characteristics of semiconductor devices has direct consequences on electromagnetic emission (EME) because of the unpredictable time-dependent variability of the emission level. It is well known that differences between components due to unavoidable process variations are a major source of variability of EME [5], [6]. Recently, some publications have shown that accelerated aging tests such as high or low

temperature operating life, thermal cycling, or electrical over-stress lead to a significant variation in EME produced by power supply units [7], high side switch devices [8] or I/O buffers [9]. However, no publication has yet demonstrated that the wear-out mechanisms during accelerated lifetime tests are responsible for the drift in EME level; hence, the real effect of IC aging on EME remains unclear.

This paper intends to clarify the effect of IC aging on EME experimentally, and to correlate the change in emission level with IC intrinsic degradation mechanisms. A test chip designed using Freescale 90-nm CMOS technology was developed to characterize both the wear-out mechanisms induced by electrical stresses and the changes over time, together with stress levels of power integrity and conducted emission of some basic blocks (digital cores and I/O buffer). Several digital cores with various types of on-chip capacitance were duplicated in order to evaluate the influence of electrical stress. The first section of this paper presents an experimental characterization of degradation mechanisms induced by electrical stress on the MOS devices. Efficient stress conditions for the accelerated aging of the device can be deduced. The second section describes the test chip and the experimental setup for characterizing the change in EME and power integrity during stress periods. The third and fourth sections present the experimental results of electrical stress effects on EME of the output buffer and digital core structures, respectively. Finally, there is a comparison of emission levels measured on the digital cores with different on-chip capacitor technologies.

II. CHARACTERIZATION OF DEGRADATION MECHANISMS IN 90-NM CMOS TECHNOLOGY

A. CMOS Transistor Degradation Mechanisms

During their lifetime, CMOS transistors are affected by intrinsic failure mechanisms such as time-dependent dielectric breakdown, negative bias temperature instability (NBTI), or HCI [10], mainly brought on by harsh environmental conditions such as high or low temperatures and electrical overstress. Table I summarizes the main failure mechanisms which may affect MOSFET transistors. The most common intrinsic failures of CMOS circuits induce charge trapping and breakdown in the gate oxide layer. The failure origins and their models have been studied for years and active research is still on-going [11]. Among these mechanisms, HCI and NBTI are the major

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TABLE I
COMMON CMOS TRANSISTOR INTRINSIC FAILURE MECHANISMS AND MODES

Failure mechanism	Cause of failure	Failure modes	Acceleration factor
Time dependent dielectric breakdown (TDDB)	Cracks and holes in gate oxide.	Gate leakage.	High temp. Electrical field.
Hot carrier injection (HCI)	Trapped carrier in gate oxide due to the effect of ionization of channel carriers near the drain region.	Threshold voltage shift and mobility degradation. Serious issue in short channel NMOS transistor.	Low temp. High drain-source voltage. Radiation exposure.
Negative Bias Temperature Instability (NBTI)	Formation of fixed-oxide charge in PMOS gate oxide.	Threshold drift with partial recovery phenomenon. Serious issue in thin oxide PMOS transistor.	High temp. High negative gate voltage.

TABLE II
STRESS CONDITIONS

Accelerated wear-out mechanism	Transistor characteristics	Drain-source voltage V_{ds}	Gate-source voltage V_{gs}
Hot carrier injection (HCI)	Thin oxide NMOS Width = 10 μm Length = 0.1 μm	High V_{ds}	V_{gs} condition to obtain maximum substrate current
	Thick oxide NMOS Width = 10 μm Length = 0.38 μm		
Negative Bias Temperature Instability (NBTI)	Thin oxide PMOS Width = 10 μm Length = 0.1 μm	$V_{ds} = -50 \text{ mV}$	High negative V_{gs}
	Thick oxide PMOS Width = 10 μm Length = 0.38 μm		

contributors to the degradation of device performance in advanced CMOS technologies.

The degree of degradation of a device, and hence its lifetime, depends on the level of stress and its duration. Applying a high level stress (e.g., high temperature or high voltage) for a short period accelerates the damage rate for the relevant wear-out failure mechanisms. This principle is commonly used in accelerated life tests to extrapolate semiconductor device lifetimes, or in screening tests.

B. Characterization of Failure Mechanisms

A dedicated test chip was developed to characterize the failure mechanisms using Freescale 90-nm CMOS technology. It contains MOS devices with various geometrical and gate options (thin and thick oxide options, with nominal operating voltages of 1.2 and 3.3 V, respectively). The transistor terminals (gate, drain, source, bulk) were accessed with dc probes. $I_{ds}(V_{gs}; V_{ds})$ transistor characteristics were measured with a Keithley 2601-A source meter and a data acquisition board after several periods of electrical stress. The stress conditions for the tested MOS transistors are given in Table II. The tests aimed to characterize NBTI in PMOS, and HCI in NMOS devices specifically. The NBTI characterization was based on fast ΔI_D measurement to

TABLE III
CHARACTERIZATION OF HCI IMPACT ON THIN AND THICK OXIDE NMOS TRANSISTORS

Transistor type	Stress conditions	ΔI_{dsat}	ΔV_{th}	ΔG_m
Thin oxide NMOS	After 2000 s @ 3 V	- 40 %	+ 25 %	- 20 %
	After 500 s @ 4 V	- 75 %	+ 40 %	- 40 %
Thick oxide NMOS	After 2000 s @ 5 V	- 7 %	+ 5 %	- 5 %
	After 1000 s @ 7 V	- 20 %	+ 25 %	- 10 %

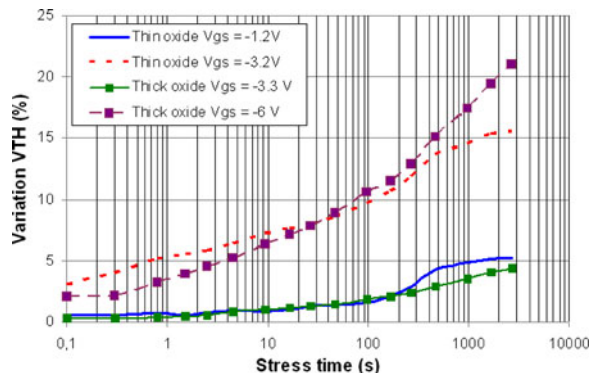


Fig. 1. Characterization of NBTI impact on thin and thick oxide PMOS transistors.

reduce both the measurement time and the recovery effect during device monitoring [12]. More details about the measurement setup and results can be found in [13] and [14]. Temperature is also a well-known accelerating factor in IC failure mechanisms, as shown in Table I. However, to simplify the setup, this factor is not considered in our experiments. All the tests were performed at ambient temperature.

The saturation current I_{dsat} is strongly affected depending on the stress voltage and duration due to both threshold voltage V_{th} and transconductance G_m changes. The relative change in I_{dsat} , V_{th} and G_m of thin and thick oxide NMOS transistors after two types of HCI acceleration stress are summarized in Table III.

Fig. 1 shows the effect of NBTI stress on thin and thick oxide PMOS transistors. Depending on the duration of the stress voltage, the negative bias condition also brings about a significant reduction in saturation current due to an increase in the threshold voltage of the transistor; this follows a power law dependence with stress time.

The experimental characterizations show that HCI and NBTI effects occur in NMOS and PMOS devices, respectively, when electrical stresses are applied. The degradation rate increases with the stress voltage. Above 4 V for thin-oxide devices and 7 V for thick-oxide transistors, sudden hard failures occur rapidly due to oxide breakdown. Efficient electrical stress conditions can be deduced from these experiments to accelerate the aging of ICs designed using this technology: from 3 to 4 V for thin-oxide transistors, and from 6 to 7 V for thick-oxide transistors.

TABLE IV
OPTIONS OF THE FOUR CORES

Core number	On-chip capacitor type	Core capacitance (without/with supply)		Voltage bounce
Core 1	None (reference)	18 pF	25 pF	59 mV
Core 2	Metal-metal	99 pF	104 pF	27 mV
Core 3	P-type MOS	90 pF	60 pF	40 mV
Core 4	N-type MOS	100 pF	128 pF	26 mV

TABLE V
TESTS AFTER STRESS INTERVAL

Tested block	On-chip capacitor type
Output buffer	Conducted emission (1 Ω method)
	I(V) of pull-up and pull-down devices
	Output waveform
Digital core	Conducted emission (1 Ω method)
	Power supply voltage bounce (on-chip sensor)
	Signal propagation delay

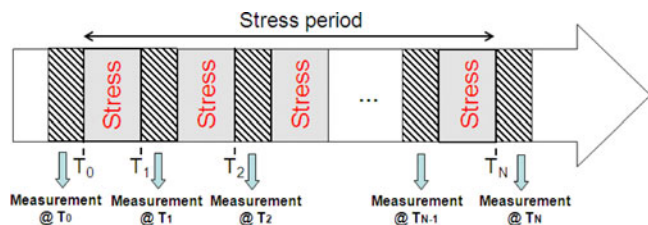


Fig. 2. Principle of characterization of aging effect on EME: measurement-stress-measurement flow.

III. SETUP FOR CHARACTERIZING THE AGING EFFECT ON IC ELECTROMAGNETIC EMISSION

A. Test Chip Presentation

A dedicated test chip was designed using Freescale 90-nm CMOS technology for IC emission and susceptibility modeling, and for characterizing the effect of aging on the EMC of ICs. The test chip includes various basic blocks, such as digital cores, I/O, voltage regulator, ring oscillator, and differential amplifiers. The blocks are isolated from each other by separating the power supply rails. The chip is mounted in a LQFP64 package. A test board with socket was developed to mount the various tested samples. The same test board was used for all the tests. The experiment focused on two noisy structures, i.e., which produce significant amounts of voltage bounce and conducted emission: a digital output buffer and a digital core. This digital core is a basic 100-stage shift register duplicated four times in the chip: the first is the reference core; the three others have additional on-chip decoupling capacitors implemented in three different types: metal-insulator-metal, and MOS capacitor with either N- or P-well. The options are summarized in Table IV. The values of the core capacitance were extracted from impedance measurements made by a vector network analyzer. As MOS capacitors depend on voltage, they are measured with and without a dc power supply applied to the cores.

On-chip voltage sensors were placed along the power supply rails of each core to monitor the voltage bounce waveform in the time domain. The principle and implementation in the test chip are explained in [15] and [16]. The peak-to-peak voltage bounces measured on the power supply rail of each core are shown in Table IV.

B. Description of the Experimental Setup

The experiment was based on a measurement–stress–measurement flow, which consists in applying electrical stress to the circuit under test while interrupting the stress regularly over short periods for characterization purposes (Fig. 2). The stress

conditions, duration, and measurement intervals are defined before the test. With this procedure, the gradual change in circuit characteristics can be monitored. The output buffer is supplied at a nominal 3.3 V; the stress voltage applied to its power supply ranges from 6 to 7 V. The nominal power supply voltage of the cores is 1.2 V. The stress voltage applied to its power supply ranges from 3 to 4 V. The stress duration depends on the stress voltage. It is adjusted so as to observe gradual changes over a reasonable time interval, without inducing excessively rapid hard failures. The characterization time has to be minimized to prevent complete recovery. However, it cannot be reduced to less than 15 min so partial recovery is likely, especially for NBTI induced failures.

Several tests, as described in Table V, are performed after each stress interval to measure the conducted emission and the degree of degradation of the tested structure. The conducted emission measurements are based on IEC61967-4 Standard—1 Ω method [17], which is devoted to characterization of the RF current generated by IC switching activity. The repeatability of the different tests was evaluated beforehand and remained within an acceptable range. Although the input of the on-chip voltage sensor is stressed, any drift of its response is compensated by a recalibration process performed after each stress interval. Electrical stress has no significant impact on sensor performance up to 4 V. When the stress voltage exceeds 4 V, the voltage measured by the sensor tends to become noisy. Therefore, on-chip voltage fluctuation measurements are not performed after stressing at 4 V.

IV. CHANGE IN OUTPUT BUFFER CONDUCTED EMISSION

A. Effect of Electrical Stress on the Output Buffer

Applying an electrical stress to the power supply of the output buffer can degrade the NMOS pull-down (PD) and PMOS pull-up (PU) devices. Individual $I(V)$ characterizations are performed after each stress interval to evaluate the effect on their saturation current. As degradations of PD and PU devices can have a direct impact on the rise and fall times of the output signal, these are also measured after each stress interval.

6.5- and 7-V electrical stresses were applied to two different samples. Both stress conditions induced a change of saturation current of PU and PD devices, as shown in Fig. 3. The saturation current reduction rate depends on the stress amplitude. A 7-V stress applied for 30 min has the same effect as a 6.5-V stress applied for 4 h. Only the PD device is affected by the electrical stress, which accelerates HCI in the NMOS transistors of

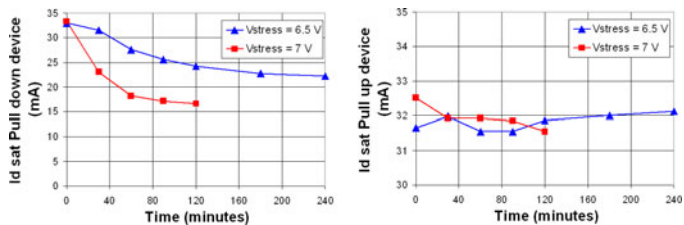


Fig. 3. Change in saturation current of PD (left) and PU (right) devices vs. stress time

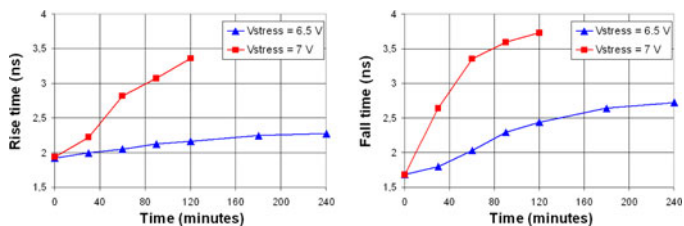


Fig. 4. Change in rise (left) and fall times (right) of the output buffer versus stress time

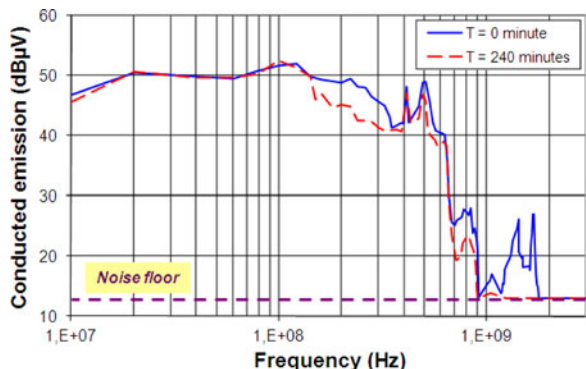


Fig. 5. Change in conducted emission of the output buffer after 6.5-V electrical stress over 240 min.

the PD device. No NBTI effect observed because of the long characterization time and the rapid recovery time for NBTI.

The rise and fall times of the signal delivered by the output buffer increase while the saturation current of the PD device decreases (Fig. 4). The asymmetric degradation of PU and PD devices results in a larger increase in the fall time.

B. Change in Conducted Emission Level

The conducted emission of the output buffer was monitored after each stress interval. Figs. 5 and 6 show the changes in conducted emission spectra for both stress conditions. To facilitate the comparison of emission spectrum levels at various stress times, only the spectrum envelopes have been plotted.

The electrical stress induces a wide range reduction in the emission level, especially at high frequencies except for the first eight spectral harmonics (up to 80 MHz), the amplitudes of all even or odd harmonics change after the stress. The high-frequency content above 600 MHz disappears completely after the stress period. The reduction in the emission spectrum envelope can be as much as 20 dB. Resonances at 100 and 400 MHz are also attenuated.

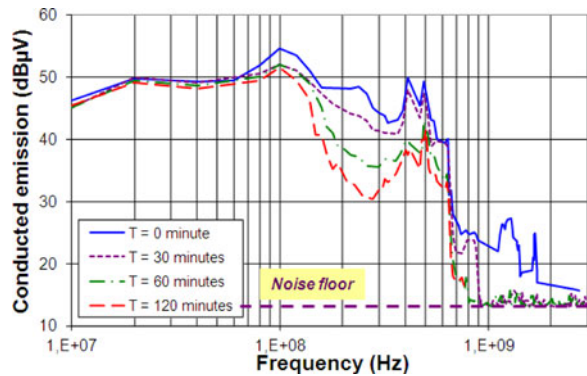


Fig. 6. Change in conducted emission of the output buffer after 7-V electrical stress over 120 min.

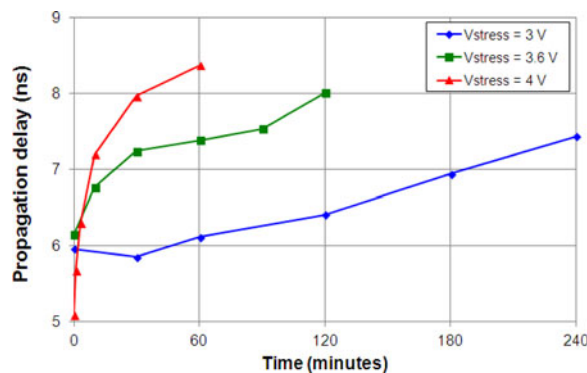


Fig. 7. Change in propagation delay of core 1 for different stress conditions.

The change in the level of the emission spectrum is a function of the stress voltage and the stress duration. Fig. 6 shows that the emission level falls steadily with stress time. As with $I(V)$ and switching time measurements, the effect of a 7-V stress applied for 30 min is the same as a 6.5-V stress applied for 4 h. The fall in emission level is a consequence of the fall in the drive current and the switching time of the output buffer due to HCI in the PD device.

V. CHANGE IN DIGITAL CORE CONDUCTED EMISSION

A. Effect of Electrical Stress on Digital Core

Three different electrical stress conditions were applied to the power supply pin of core 1: 3, 3.6, and 4 V. After applying the stress, the three tested samples remained operational. Their quiescent current remained constant, so no failures occurred during the stress period. However, their timing characteristics were strongly degraded. Fig. 7 shows the change in propagation delay of binary data between two stages of core 1 after each stress interval for the different stress conditions. The delay increased from 25% to 65% depending on the stress voltage and its duration. The electrical stress applied to the core power supply accelerates wear-out mechanisms such as HCI and/or NBTI, which increase the propagation delay of each gate of the core.

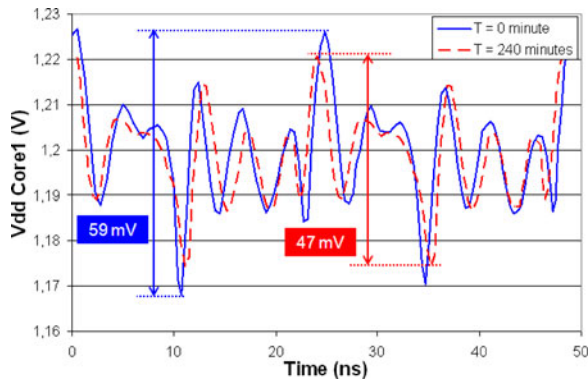


Fig. 8. Change in core 1 power supply voltage bounce after 3-V electrical stress over 240 min.

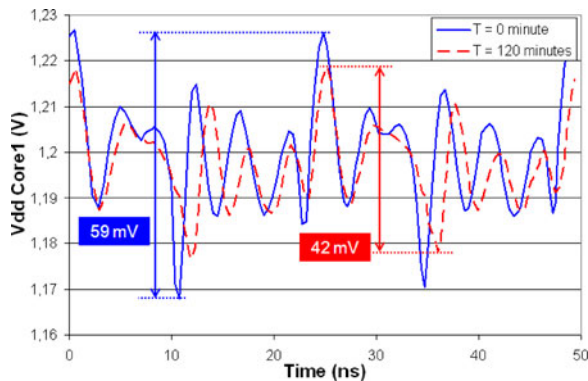


Fig. 9. Change in core 1 power supply voltage bounce after 3.6-V electrical stress over 120 min.

B. Change in Digital Core Power Integrity

Figs. 8 and 9 show the power supply voltage bounce as measured by the on-chip sensor before and after application of 3- and 3.6-V stresses. The voltage fluctuations are linked to the 40-MHz clock switching which synchronizes the operation of the core. At each clock pulse edge, a rapid peak voltage appears due to the switching of circuit gates, followed by an oscillation with a pseudo-period of 4.2 ns. This oscillation is linked to the excitation of the chip-package resonance, which is associated with the core equivalent capacitance and parasitic inductances distributed along the power supply and ground pins of the core.

A reduction of between -20% and -30% of the peak-to-peak amplitude was observed depending on the stress voltage and duration. The waveform of the signal was also modified. The first peak was less steep. The period of the resonance oscillation did not change. Its amplitude was reduced, but it was still damped at the same rate. The excitation current of the circuit resonance was reduced. Impedance measurements carried out with a vector network analyzer between the power supply and ground pin of core 1 confirmed that the impedance of the power distribution network (PDN) of the core was not modified by the stress. Neither the equivalent capacitance of the core, nor the inductance and resistance associated with its PDN were affected by the electrical stress.

The reduction in power supply voltage bounce is linked to the change in transient current produced by the core activity.

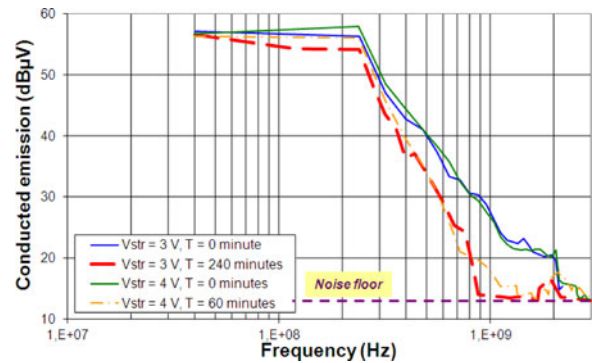


Fig. 10. Conducted emission of the core 1 before and after 3- and 4-V electrical stress.

Wear-out mechanisms accelerated by electrical stress reduced the transient current amplitude and caused temporal spreading due to the increase of gate switching time.

C. Change in Conducted Emission

Conducted emission in the digital core 1 was monitored after each stress interval for the different stress conditions. Fig. 10 shows the emission spectrum envelopes measured before and after stress periods at 3 and 4 V. Electrical stress induces a wide range reduction in emission level, especially above 200 MHz. The measured reduction was as much as 15 dB at 1 GHz. The harmonic content above 1 GHz was below the noise floor of the spectrum analyzer. As observed during on-chip measurement (Figs. 8 and 9), the amplitude of the spectral peak at the chip-package resonance frequency (240 MHz) was reduced by 2 dB.

This measurement confirms the same conclusion as was drawn for the power supply voltage bounce change after stress. Both the amplitude and the high frequency spectral content of the transient current produced by the digital core were reduced, due to the wear-out mechanisms accelerated by the electrical stress.

D. Comparison of the Electrical Stress Effects Between the Four Cores

Whatever the type of capacitor implemented, the electrical stress affected the timing performance of the digital core. The propagation delay changed identically in the four cores. Thus, the same degradation mechanisms occur.

As measured in core 1, the waveform of the power supply voltage bounces measured on each core altered after electrical stress, but not identically. Fig. 11 shows the change in the peak-to-peak amplitude of the voltage bounce measured on the power supply of the four cores with the on-chip sensors. Except for core 4, the peak-to-peak amplitude of the voltage bounce measured on the power supply of each core was reduced. The voltage bounce for core 1 was reduced by 20 to 30% depending on the amplitude and duration of the stress. Cores 2 and 3 show a reduction of about 10 to 15%.

The voltage bounce measured on the core 3 power supply shows a 140-MHz oscillation, due to its chip-package primary resonance. After stress, the damping of the oscillation did not

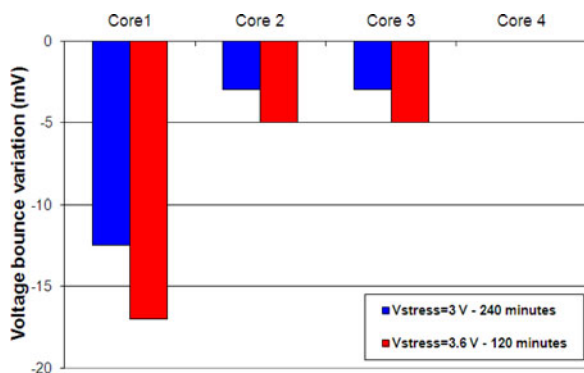


Fig. 11. Change after two types of stress in the peak-to-peak amplitude of the voltage bounce measured on the power supply of the four cores.

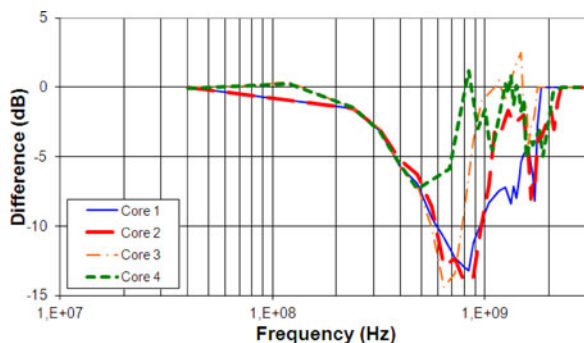


Fig. 12. Change in conducted emission of the four cores after a 3.6-V stress over 120 min.

change. Moreover, impedance measurement carried out with a vector network analyzer between the power supply and ground pin of core 3 showed that the on-chip capacitance of cores 2, 3, and 4 were not modified by the electrical stress.

The change in conducted emission of cores 2 to 4 was also characterized. The change in their emission spectra is identical to that of core 1. The variation in the spectrum envelope after 120 min at the 3.6-V stress is shown in Fig. 12. The conducted emission level tends to decrease above 200 MHz whatever the type of decoupling capacitor. The reduction becomes more significant at high frequency because of the increase in the propagation delay for each gate of the core. The reduction seems to be less above 800 MHz because the emission level is below the noise floor after stress, except for core 4.

These results demonstrate that the electrical stress does not degrade the on-chip capacitors, and hence their decoupling efficiency.

VI. CONCLUSION

Recent studies have shown that the aging of integrated circuits may modify electromagnetic emission significantly. This paper reports on an experiment to elucidate the origins of changes in emission level in a circuit designed using 90-nm CMOS technology. Electrical stresses applied to an output buffer and a digital core strongly reduced the conducted emission, especially the high-frequency spectral content, and improved the power integrity. Analysis of device degradation identified the wear-out

mechanisms activated by stress, such as HCI and NBTI as the cause of the gradual reduction in emission level. These degradation mechanisms reduce the current drive and the switching time of MOS devices. The PDN of the digital core was not altered by the internal aging process. From a modeling point of view, the prediction of the changes in integrated circuit emissions relies on correctly estimating the transient current amplitude reduction and spread in the time domain.

Although the results presented in this paper show a decrease in emission at circuit level, aging is an additional source of variability for emission level with circuit process dispersion or temperature. Moreover, aging does not reduce EMC issues for integrated circuits. They can become less robust to electromagnetic interference, as shown by several recent publications [18], [19]. Similar experimental work should be carried out to clarify this question. Finally, the results presented in this paper confirm that the gradual changes in circuit electromagnetic “signature” associated with conducted or radiated emission can provide a simple indication as to the state of its internal aging.

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