Fabrication of high-density Si and SixGe1–x nanowire arrays based on the single step plasma etching process

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Dense arrays of silicon and silicon germanium nanowires are fabricated using a top–down approach, which exploits the excellent patterning capabilities of inductively coupled plasmas. Using standard deep UV lithography on a previously deposited silicon oxide hard mask, silicon nanowires with straight and smooth sidewalls and a high aspect ratio greater than 60:1 can be obtained with $SF_6/O_2/HBr/SiF_4$ plasma chemistries. The best results are obtained using Cl_2/N_2 high-density plasmas to pattern $Si_{0.5}Ge_{0.5}$ nanowires with an aspect ratio of 10:1. © *2013 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4812792]

I. INTRODUCTION

Because of the promising properties of nanowires (NWs), the last few years have seen much attention focused on their research. Silicon NWs are increasingly important in emerging technologies such as biochemical sensors,[1] photovoltaic devices,[2] and optical waveguides,[3] and the high carrier mobility of silicon germanium NWs[4] makes them promising candidates for 3D integration and gate-all-around MOSFETs.[5] There are two approaches toward NW fabrication that can be considered. First, the "bottom-up" growth technique creates NWs with high density and almost unlimited size, and can be achieved at a very low cost.[6] This technique, however, suffers from contamination issues from the metal catalyst required for directing the growth. Also, with this technique, the position and growth direction of the NWs are difficult to control precisely. The second NW growth approach, the "top–down" fabrication process, directly uses standard lithography and etching technologies. The NWs fabricated using these conventional technologies are contaminant free and exhibit superior properties,[7] a high process reproducibility and well controlled positions and diameters. Different patterning technologies have been reported in the literature for the fabrication of high-aspect-ratio silicon NWs. After Si etching, some approaches use a metal hard mask combined with a lift-off step,[8,9] while other studies used the popular Bosch™ process for the etching of silicon NWs.[10]

This paper focuses on the plasma etching of Si and Si_xGe_{1-x}. Typical complementary metal–oxide–semiconductor (CMOS) compatible process steps are carried out using deep UV (DUV) lithography with SiO_2 hard mask patterning and subsequent Si/Si_xGe_{1-x} etching via inductively coupled plasma (ICP) reactors. Special attention is given to the development of processes minimizing the NW sidewall roughness, which can induce diffusion and carrier mobility issues. For this reason also, processes with multiple etching/polymer deposition cycles, such as the Bosch process, cannot be used due to the generation of sidewall scalloping.[11,12]

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II. TOP–DOWN APPROACH FOR NW FABRICATION

To create the NWs, we employed 200 mm-wide silicon and silicon germanium layers grown by epitaxy (2 μm thick). Hard mask formation was subsequently performed by depositing a 500 nm resist layer on top of 50 nm of a bottom antireflective coating (BARC) spin coated on 500 nm of SiO_2 deposited by plasma-enhanced chemical vapor deposition (CVD). The photoresist (PR) template was defined using a 248 nm DUV exposure (ASM300 Stepper) and consisted of PR dots with 250 nm diameters and spacings, which covered the entire 200 mm wafer. The BARC and SiO_2 hard mask opening was etched using a 200 mm magnetically enhanced reactive ion etching plasma etch chamber (Emax™ from Applied Materials®). The plasma chemistry used for the hard mask opening was a highly PR-selective mixture of $CF_4/CH_2F_2/N_2$ gases. Finally, following the Si or SiGe plasma main etch step, the SiO_2 hard mask was removed with 49% hydrofluoric acid (HF).

A. Si NW etching

After the SiO_2 hard mask opening is created, the 200 mm wafers are cleaved into 4 × 4 cm^2 samples and then patched onto 300 mm SiO_2 substrates prior to the Si NW main etching. The thermal contact between the samples and the 300 mm carrier substrate is provided with thermal Fomblin® oil and Kapton parts, thereby ensuring that the wafer temperature during plasma processing is well controlled.

The Si NW etch development is performed in a 300 mm ICP source chamber (DPS AdvantEdge™ platform from Applied Materials). The plasma is maintained using two radio-frequency (rf) planar spiral coils held at 13.56 MHz to improve the ion flux uniformity. The temperatures of the anodized aluminum walls and the electrostatic chuck are maintained at 80 and 65 °C, respectively.

The chemistry selected for silicon NW etching is a mixture of $SF_6/O_2/HBr/SiF_4$. The fluorine sources, SF_6 and SiF_4, are commonly used for fast chemical etching of silicon, though lateral etching by fluorine radicals can be problematic

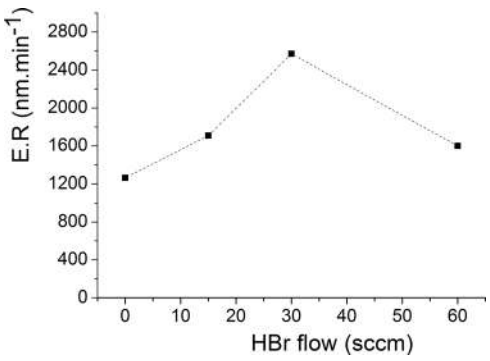

FIG. 1. Graph of the SiO_2 etch rates as function of the HBr flow. The etching conditions are a 30 sccm SF_6 flow; a 60 sccm O2flow; 0–60 sccm HBr flow; rf bias power of 1000 W; rf source power of 150 W; and a pressure of 25 mTorr. A peak in the etch rates is reached for a 30 sccm HBr flow.

and must be inhibited by the formation of a passivating layer as the etching proceeds. The role of O_2 is crucial to generate a thin protective layer of SiO_xF_y on the NW sidewalls,[13–18] thereby increasing the selectivity with the hard mask (in SiO_2) by reducing the SiO_2 etching. Because of the O_2 in the plasma gas phase, a thin SiO_xF_y layer is formed at the bottom of the Si NWs during the etching process; the layer is then chemically sputtered. This sputtering leads to the formation of a passivation layer via line-of-sight deposition of the heavy SiO_xBr_y etch by-products. In most cases, bromine is not detected on the sidewall surfaces since it is substituted by the oxygen present in the plasma gas phase. In agreement with the results seen by Gomez *et al.*,[19] our studies show that the vertical silicon etch rate increases with the addition of HBr in the plasma gas phase, as well as the selectivity to the SiO_2 hard mask. As shown in Fig. 1, this observation is true only with an HBr flow up to 30 sccm in the gas mixture, above which the silicon etch rate decreases. This is because SF_6 and SiF_4 are diluted if the HBr flow is increased, leading to a lower F concentration in the plasma. Also, the formation of HF causes a decrease in the F concentration when the HBr flow is increased. Finally, the role of SiF_4 has been discussed in previous papers and seems to both improve the silicon sidewall passivation and reinforce the etch selectivity with the silicon oxide hard mask.[20]

Optimized process conditions in terms of the etch rate, mask selectivity, and anisotropy are found using an rf source

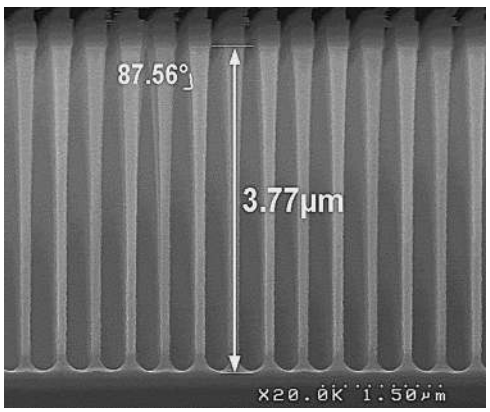

FIG. 2. SEM micrographs of Si NWs etched with run 1 conditions.

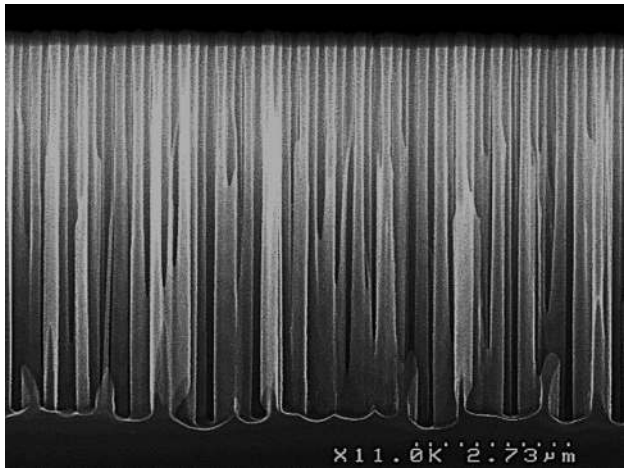

FIG. 3. SEM micrographs of Si NWs etched with run 2 conditions.

power of 1500 W and an rf bias power of 200 W, and by using a total pressure of 25 mTorr in the plasma chamber. In order to prevent process drift, all experiments are conducted with the chamber walls coated with a 50 nm-thick SiO_xF_y layer, which is formed by etching silicon or SiO_2 substrates in SiF_4/O_2 plasma.

Optimization of the NW etching process as a function of gas phase chemistry, as mentioned previously, is accomplished using various mixtures of SiF_4, HBr, SF_6, and O_2. Figures 2–4 show the different Si NW profiles after etching with different gas phase chemistries, as summarized in Table I. In the first run (Fig. 2), the high F:O ratio leads to severe roughness and an undercut, and an increased etch time would generate a catastrophic drop of the NWs. On the contrary, in the second run (Fig. 3), the lowered F:O ratio (via reduced SF_6 and SiF_4 flows) generates significant micromasking. This demonstrates that the bottom fluorine-rich oxidized silicon layer through which the etching proceeds is too thick, leading to the micromasking. These experiments show that the process window is very narrow and extremely sensitive to the F:O ratio. Indeed, the process can be switched from an undercut to micromasking by decreasing the fluorine source

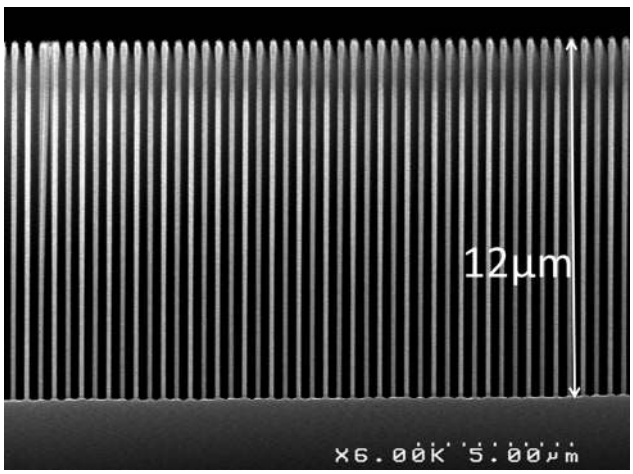

FIG. 4. SEM micrographs of Si NWs etched with run 3 conditions. The diameter of the NWs is 200 nm and the length is 12 μm.

TABLE I. Summary of experimental gas flow in the $SF_6/O_2/HBr/SiF_4$ chemistry.

	SF_6 (sccm)	O_2 (sccm)	HBr (sccm)	SiF_4 (sccm)	Time (s)	Height (μm)	Angle (degree)
Run 1	32	45	30	30	100	3.8	87.56
Run 2	28	45	30	15	200	5.3	–
Run 3	28	45	60	20	500	12	90

(SF_6 or SiF_4 flow) by only a few sccm. The best process is found in the third run (Fig. 4) with a perfect trade-off between lateral etching and sidewall passivation without the formation of micromasking on the silicon surface. Using these conditions, very straight 12 μm-tall NWs can be grown over the 16 cm^2 wafer area. The aspect ratio of these 200 nm diameter NWs is, therefore, about 60:1, which is the same order of magnitude achieved with the Bosch plasma etch process but without sidewall scalloping. Figure 5 shows the NW arrays after the hard mask removal using a 49% HF dip, which shows the tendency of the NWs to collapse and stick together due to capillary forces. The use of a vapor phase HF, which is operated at a pressure point without condensation, would be more appropriate for samples such as these and should prevent NW collapse. Nevertheless, high-magnification SEM images of the NW sidewalls show that even when scalloping is avoided, a non-negligible roughness is present (Fig. 6). This roughness can still be detrimental to the electrical functioning of devices such as NW transistors and photovoltaic cells.

1. Silicon NW sidewall roughness control

The silicon sidewall roughening that occurs as a result of fluorine/oxygen-based etching chemistries is attributed to the irregular passivating oxide layer formed on the silicon sidewalls. In some locations along the sidewalls, fluorine radicals can punch through the passivating layer and etch silicon laterally, and in other locations where the oxide layer is sufficiently thick the sidewall is well protected. Finally, the micropitting of the passivation layer shows that the etch process cannot generate a thin, uniform, and well-controlled passivation layer around the silicon sidewalls. One possible explanation involves ions that arrive at a grazing angle on the silicon sidewalls because of slight bending of the ion trajectory due to charging on the oxide hard mask. These grazing-angle ions can locally punch through the passivation layer in the thin regions of SiO_2. Since the top part of the NWs is often seen to be more acutely damaged [Fig. 6(a)], ion-induced pitting of the passivation layer at the top of the NWs, where local charging is the most likely, seems plausible.

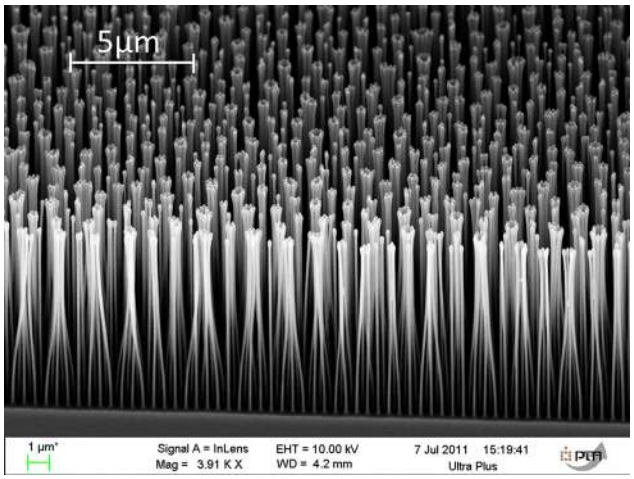

FIG. 5. (Color online) SEM image of the Si NW array after HF dip.

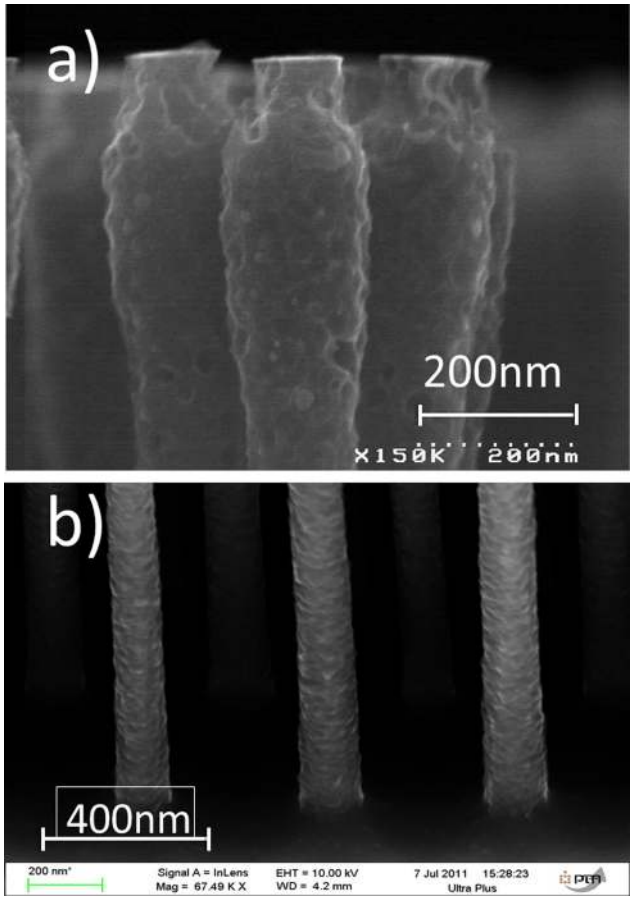

FIG. 6. (Color online) SEM image of the Si NW sidewall roughness after $SF_6/0_2/HBr/SiF_4$ etching. (a) Top of the NWs (after HF dip). (b) Bottom of the NWs (after HF dip).

We now consider two methods to decrease the sidewall roughness. The first was developed by Dornel *et al.*,[21] who annealed the sample at temperatures above 800 °C in an H_2 atmosphere, and observed that the surface was smoothed by the surface diffusion of silicon atoms on the sidewalls. For our samples, we perform a 5 min annealing at atmospheric pressure in a vertical CVD furnace at 1000 °C, which reaches full temperature in 8 min. The H_2 flow is fixed at 1.6 L/min during the entire process. We cured the previously observed sample containing 12 μm-long NWs using the method indicated above, and the results are shown in the SEM images in Fig. 7. The NW sidewalls are seen to be completely smoothed even at the NW tops, which had been more severely damaged after the plasma etching. Although this technique is suitable for some applications, the high annealing temperatures necessary are prohibited in CMOS technology.

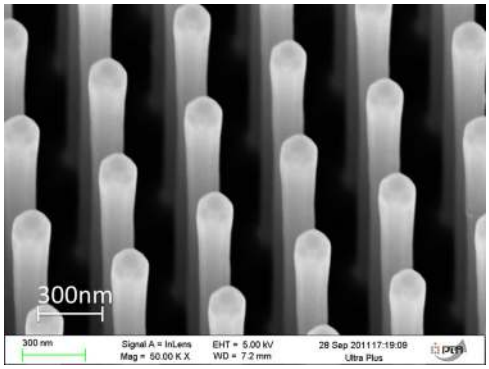

FIG. 7. (Color online) Si NW sidewall roughness after curing with 800 °C H_2 annealing.

The second method to reduce roughness uses a completely different approach. In an attempt to prevent the initial sidewall pitting, the NWs are etched using a chemistry that is less aggressive (i.e., fluorine-free chemistry). Chlorine plasma is a suitable candidate because chlorine radicals are considered less aggressive toward the passivation layer formed on the NW sidewalls. Also, with this new chemistry, the sidewall passivation will occur by N_2 addition rather than O_2. This leads to the formation of SiN_xCl_y as the passivation layer, which is more efficient as a barrier for Cl radicals on the sidewalls. Another benefit of this new chemistry is that the SiN_x passivating layers formed in Cl_2/N_2 etching plasmas are thinner than the SiO_xCl_y layers generated with the typical Cl_2/O_2 chemistry used for silicon etching.[22] Therefore, the Cl_2/N_2 plasmas are more adapted to prevent the tapered profiles that can occur with thick passivating layers. Using this new chemistry, 1.5 μm-tall NWs with 150 nm diameters are achieved, as shown in Fig. 8(a). Because the selectivity with respect to the mask is lower in chlorine-based chemistries than in $SF_6/O_2/HBr/SiF_4$, NWs with maximum aspect ratios of only 10 are produced. Nevertheless, the roughness for these NWs is nearly invisible in high-magnification SEM images of the sidewalls, confirming that the SiN_xCl_y passivation layer is quite robust with respect to reactive chlorine radicals [Fig. 8(b)].

B. SiGe NW etching

We prepared a 2 μm-thick layer of $Si_{0.5}Ge_{0.5}$ using reduced pressure CVD epitaxy (AMAT^{TM} Centura 5200 EPI) on 20 mm Si(100) wafers. After producing the hard mask opening in a capacitively coupled plasma reactor (AMAT Emax), the wafers were cleaved into 2 × 2 cm^2 samples and patched onto 300 mm Si substrates prior to SiGe NW etching in the 300 mm AMAT DPS2 ICP chamber.

The fluorine/oxygen-based chemistries previously used for Si NW etching are not suitable for SiGe layers (50% germane). In fact, the high volatility of germanium oxide products means that the passivation layer is created only via silicon etch products. The subsequent redeposition and oxidation of the Si etch by-products on the sidewalls, where no germanium products are involved in the passivation layer formation, creates a passivation layer which becomes too thin to prevent aggressive fluorine radical reactions.[23]

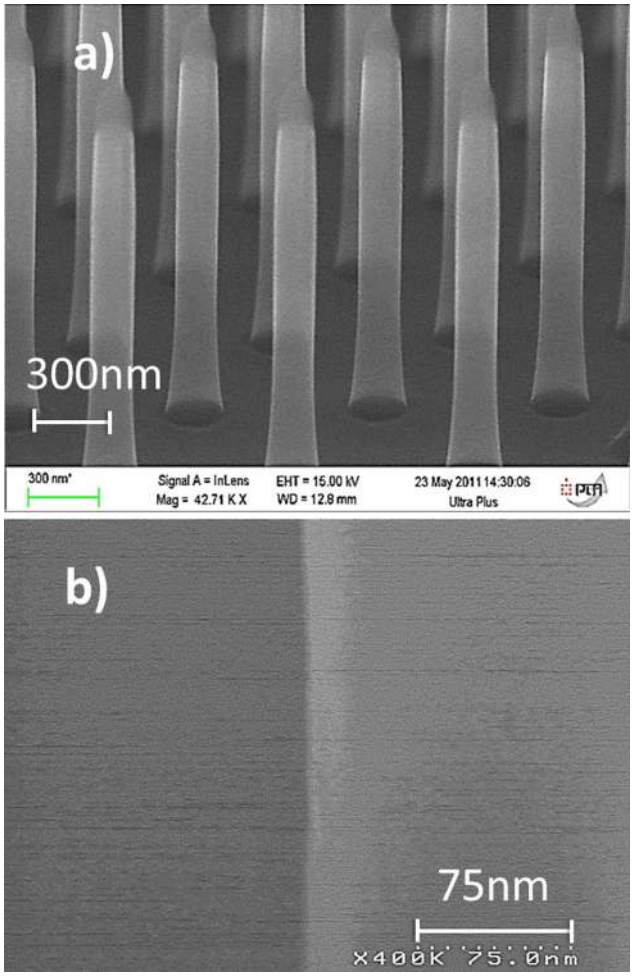

FIG. 8. (Color online) (a) SEM micrographs of Si NWs obtained via Cl2/N2 etching. The diameter is 150 nm, and the length is 1.5 μm. (b) SEM high-magnification view of the NW sidewall showing the low roughness of these NWs.

Because the sidewalls are not well protected against the fluorine chemical etching, the vertical and lateral etch rates are roughly the same, which quickly leads to mask lift-off. In a study by Joubert *et al.*,[24] it was pointed out that germanium nitride etch products are formed on germanium surfaces during the Cl_2/N_2 etch process and are chemically sputtered away in the plasma gas phase. These etch products are

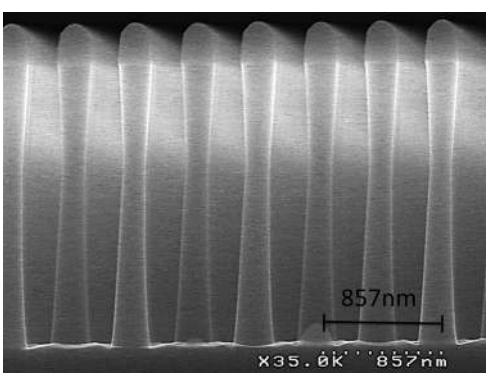

FIG. 9. SEM view of 250 nm-diameter and 2 μm-long SiGe NWs after Cl_2/N_2 etching. The "bowing effect" can be seen on the sidewalls.

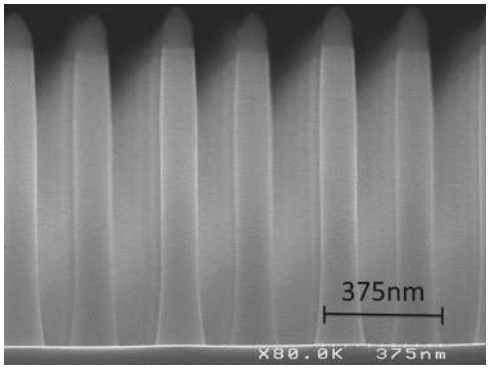

FIG. 10. SEM view of 90 nm-diameter and 1 μm-long SiGe NWs after Cl_2/N_2 etching. No bowing can be observed on the sidewalls.

re-deposited on the feature sidewalls, generating a thin GeN_x passivating layer (<7 nm).

Using this chemistry, $Si_{0.5}Ge_{0.5}$ NWs with 250 nm diameters were patterned using the following plasma conditions: A 160 sccm Cl_2 flow, a 40 sccm N_2 flow, an rf source power of 200 W, an rf bias power of 200 W, a pressure of 5 mTorr, and a growth duration of 300 s. Under these conditions, 2 μm-long SiGe NWs were obtained, as shown in Fig. 9. Following the same chemistry used for etching the Si NWs, the sidewall roughness is quite low but the etched profiles are slightly bowed. We attribute the bowing to SiO_2 hard mask charging. Unlike ions, plasma electrons have an isotropic angular distribution and negative charging can build up on the sidewalls of an insulating mask. This, in turn, can lead to ion deflection on the etched sidewalls.

In order to decrease the electrical field, the oxide hard mask volume is reduced by about ten times. This is achieved by using the previously described resist template and performing a resist pattern trimming with HBr/O_2 plasma. After the hard mask opening, the pattern diameter is 90 nm. This new layout is used to etch SiGe NWs for 130 s with the same plasma conditions used previously (see Fig. 10). The 1 μm-long NWs thus acquired have straight profiles, low roughness, and an aspect ratio of 10:1. However, successfully use of this process requires an etching time of less than 130 s to avoid hard mask faceting transfer in the SiGe patterns.

III. SUMMARY AND CONCLUSION

A technique suitable for the mass production of high-aspect-ratio Si and SiGe NWs is presented. The purpose of this research is to develop a benchmark technique to investigate the properties of NW-based devices, where special attention is given to fabrication technologies compatible with standard industrial microelectronics processes. For this reason, DUV lithography, silicon oxide hard mask, and single step ICP plasma etching are used. We show that high-density silicon NWs with an aspect ratio of >60:1 can be achieved using a continuous $SF_6/O_2/HBr/SiF_4$ plasma etching process. The remaining sidewall roughness due to the fluorine/oxygen-based plasma etching mechanism can be smoothed by annealing at 1000 °C in an H_2 atmosphere. For applications where high temperatures are prohibited, we develop a Cl_2/N_2 plasma chemistry, which enables us to obtain Si NWs with an aspect ratio of 10:1 and very low sidewall roughness. The same gas mixture can also be used to etch high-density $Si_{0.5}Ge_{0.5}$ NWs because the Cl_2/N_2 chemistries allow a passivation layer to be formed based on silicon and germanium products. The sidewall bowing issues that accompany this process are overcome by reducing the aspect ratio of the hard mask and the total etched depth.

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